Sliding Mode Observation of Capacitor Voltage in Multilevel Power Converters

Masoud Almaleki, M.Sc., B.Sc.

Submitted to the University of Nottingham for the degree of Doctor of Philosophy,

September 2010

Abstract

Smart power supply grids may be required to link future energy production and consumers. Multilevel converters are a building block for smart grids. There are several structures of multilevel converters, for example the Neutral Point Clamped (NPC), the Flying Capacitor Circuit and the Cascaded H-Bridge (CHB) converter. The modular structure of the CHB multilevel converter makes it one of the best options for smart grids. Using modular converter structures reduces production and maintenance costs.

Implementation of efficient and fast controllers for multilevel converters requires accurate measurement of the voltages and currents for the system feedback loops. Knowledge of the DC link voltages is necessary to construct voltage control loops. In a typical CHB multilevel converter there are many DC links which means that a lot of voltage transducers maybe required. Voltage transducers at medium voltage are not easy to implement and add to system cost.

This thesis presents an efficient way to observe the DC link voltages and hence eliminate the cost associated with voltage transducers. A “Sliding Mode Observer (SMO) using the Equivalent Control Method” has been chosen because of its robustness against system uncertainties. Simulation and practical work has been performed on a three-phase, three-cell multilevel converter to validate the use of this observer.

Acknowledgements

I would like to express my sincere thanks to my supervisors, Prof. Pat Wheeler and Prof. Jon Clare for all their guidance, continuous support and patience throughout my study.

I would also like to thank my PhD examiners Professor Tim Green and Professor Greg Asher for their time and valuable comments on my thesis.

Thanks are also due to my colleagues in the PEMC group for their help and support. I would especially like to thank Dr. Alan Watson for his helps with practical issues of the project.

Thanks also go to my dear sister, her husband and my lovely niece, Kiana, for their help and being supportive.

Finally, I want to thank my dearest mother who has always been enriching my life with her love and support. Thank you mother for everything.

Nottingham, 2010

Masoud Alamleki

Contents

Chapter 1

Introduction

Today's electric power generation systems convert about 33 percent of fuel energy into electricity [1]. The other 67 percent is dissipated as heat without recovery. Eight percent of this power is dissipated in the transmission lines. Twenty percent of the generation capacity is only for peak load demand, which is only five percent of the time [1].

Hydro, thermal and nuclear power generation are three major types currently being used. Hydro power plants have no pollution during operation but they cause significant environmental and often societal impacts during construction. Possible locations for hydro power plants depend on river locations. Significant construction and operational cost, as well as high pollution mean that thermal power plants are becoming a major problem. Nuclear power plants with existing technology are soon to be retired and they are not currently being replaced at a significant rate [2].

Environmental concerns mandate that thermal and nuclear power plants must be located far away from cities. This requires the construction of large, complex and expensive power transmission lines that causes ecological and environmental problems [2]. Construction of

hydro, thermal and nuclear power plants are time consuming and very expensive. In today's competitive energy market only a few corporations are capable of spending such an amount of money with pay-back period measured in decades.

Most of fossil fuels are located in limited areas on earth. Extraction and transportation of fossil fuels to other areas is costly and polluting. The depletion of fossil fuel stocks threatens the security and sustainability of future electric energy.

Commercial, environmental and security problems are primary drivers for the growth of distributed generation (DG). Any electric power production technology that is integrated within distribution network can be classified as DG. DG units can either be grid connected or independent of the grid. DG can be categorized into nonrenewable and renewable types. Internal combustion engines, combined cycle engines, combustion turbines, micro turbines and fuel cells are all nonrenewable forms of DG production technologies.

Solar, wind, geothermal and ocean are all renewable forms of DG production technologies. Renewable energy sources are inexhaustible, nonpolluting, diverse in resources and available almost everywhere so they may be the best option for a secure and sustainable energy supply infrastructure. Construction of renewable DG units is fast and cheap compared to central power plants and this choice limits the green house gas (GHG) emissions. The use of local renewable energy sources also eliminates the need for construction of new transmission circuits and large central power plants in some cases. This is not always the case as for large offshore wind farms, it is necessary to have long transmission lines.

DG is a cost effective way to improve the power quality and the reliability of power network. DG can be distributed around distribution network and failure of one unit therefore has limited impact on whole system. However there are still some economical and technical challenges in the integration of DG with distribution power network. Electricity from renewable sources is still generally more expensive than energy from fossil fuel sources, but it may be less expensive if we consider the environmental costs, health costs and energy security costs.

The electric energy produced by renewable sources often fluctuates, which can have a bad effect on grid. Therefore there is a need for additional power electronic based interfaces to enable connection. Optimal location of DG units in existing distribution networks is another important issue for active network design. Stability studies were not usually considered in design of existing passive distribution networks because they will remain stable under most conditions assuming that the transmission network is stable [2][3][4][5].

Figure 1.1 shows a diagram of an existing power system. Power flow is unidirectional from source to consumer. In an active network the power flow could be bi-directional. Figure 1.2 shows a possible structure for a future active network. In such a network new integrated active management (AM) schemes, as well as new distribution and protection technologies, are required.

System monitoring, communications and data management will play an important role in future grids. Power electronic converters using fast semiconductor switches and high speed real time controllers are capable of implementing integrated, advanced and complex control algorithms making them a good choice for deployment in a modern distribution system [6][7][8].

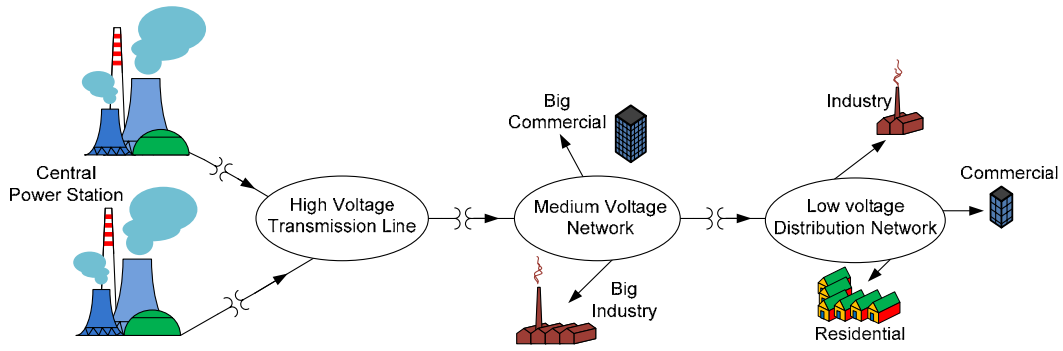


Figure 1.1: Existing passive electric power system with unidirectional power flow

The majority of power system problems occur in the distribution network, so it is necessary to make distribution networks smart to achieve a secure electricity supply [9].

One project leading towards the realization of a power electronic based substation is UNIFLEX-PM (Advanced Power Converters for ***Univ***ersal and ***Flex***ible ***P***ower ***M***anagement in future electricity network) [10].

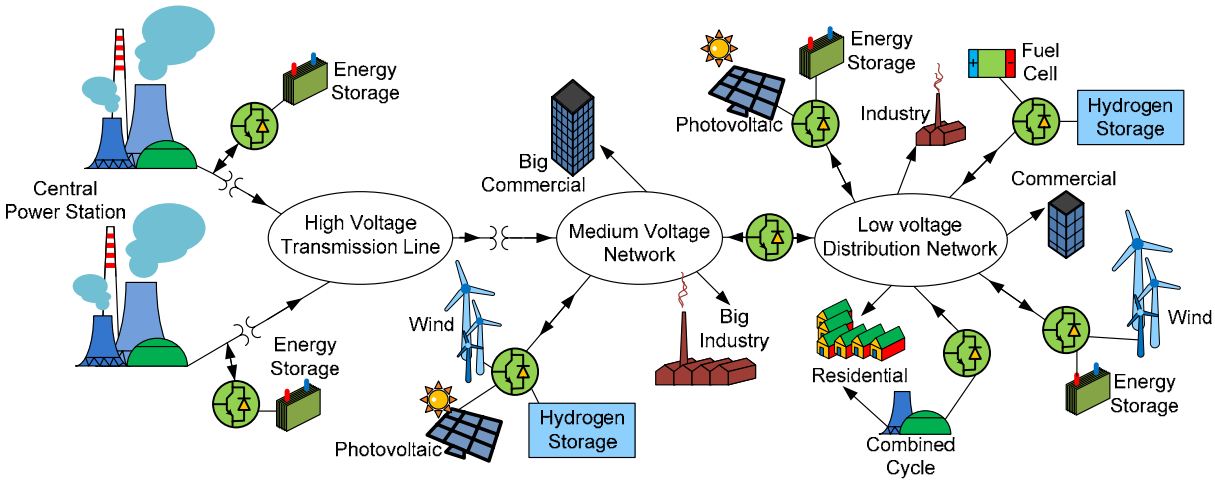
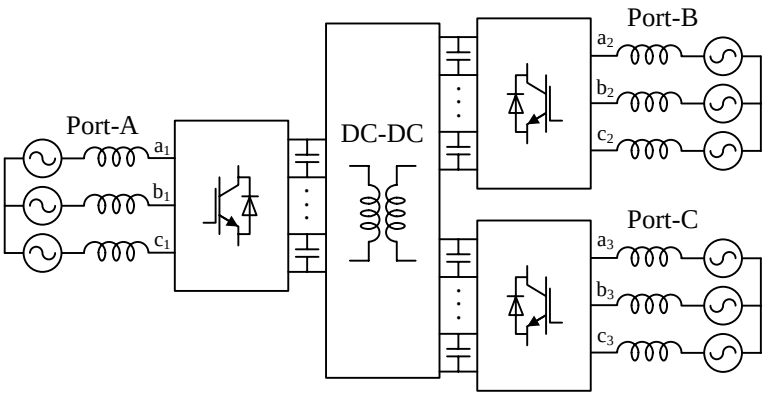


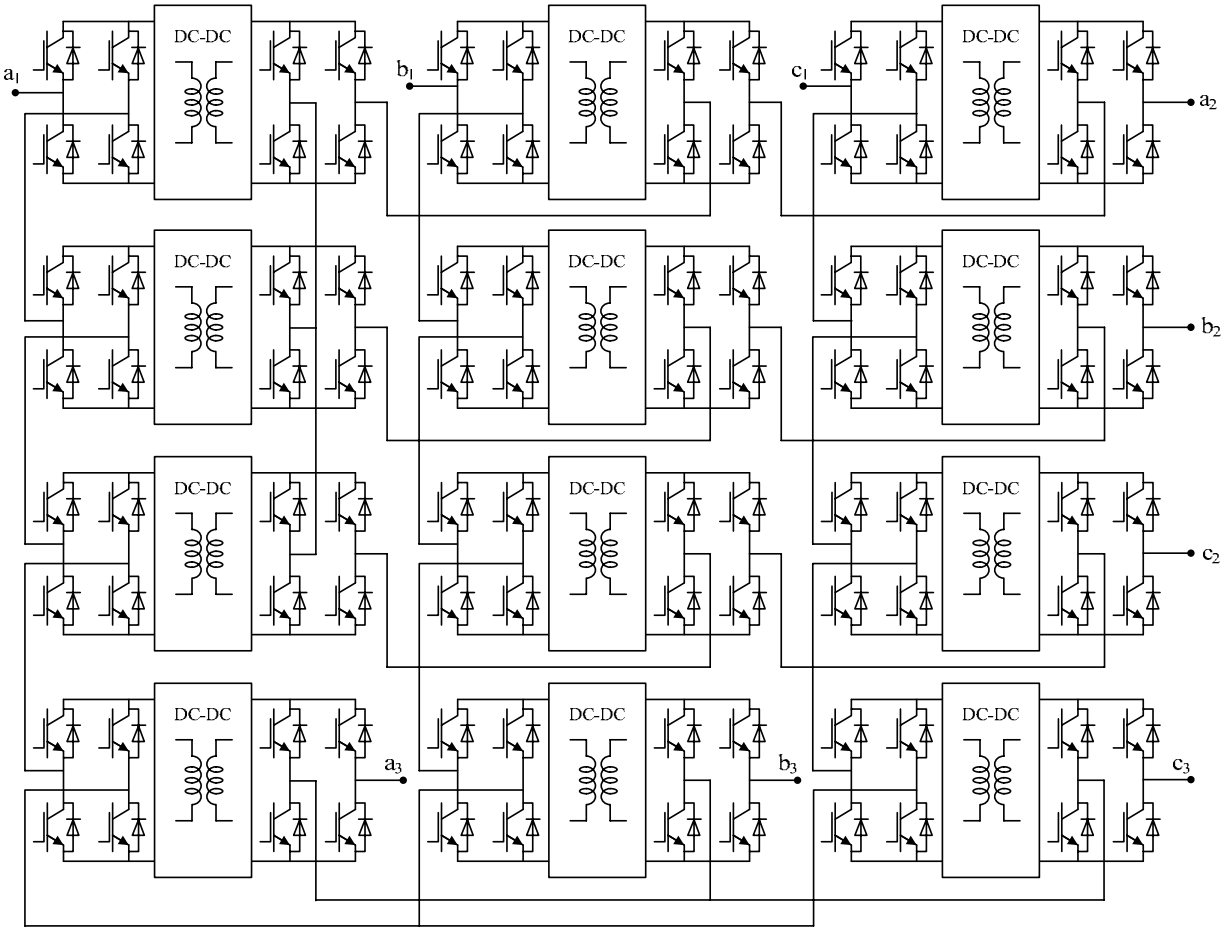
Figure 1.2: Next generation active network structure

The strategic objective of UNIFLEX-PM is to help to secure clean, economic and sustainable electrical energy. One of the suggested topologies for the UNIFLEX-PM concept is shown in figure 1.3. The objective of the multi-cellular, multilevel power converter is to develop advanced power conversion technique to meet future needs of electricity networks.

The power converter also can assist in the optimized connection of distributed energy sources, integration and management of energy storage, optimized utilization of the transmission and distribution infrastructure, maintaining a high quality of supply and coordinated control across the network. The main characteristics that make this topology a unique choice for power system applications is the modular structure and the interleaved connection between phases at the different ports.



(a): Grid connection of three-port Uniflex-PM converter



(b): Converter topology

Figure 1.3: The 3-port UNIFLEX-PM converter

By having an interleaved connection between phases, this converter is able to operate under unbalanced conditions on one port while maintaining balance on the other ports. There are 12 AC-DC-DC-AC modules in the example three-phase three-port structure shown in figure 1.3. The DC-DC converters provide galvanic isolation through a medium frequency transformer. The structure of a DC-DC converter is shown in figure 1.4.

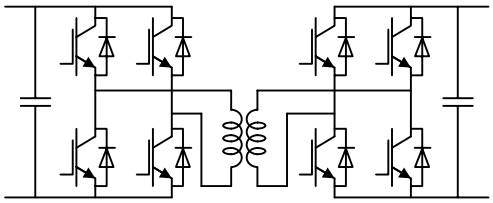


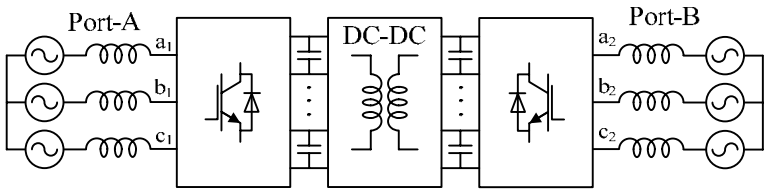
Figure 1.4: The DC-DC converter module

The 3-port power converter structure in figure1.3 could be capable of providing the following functions in a power network [11]:

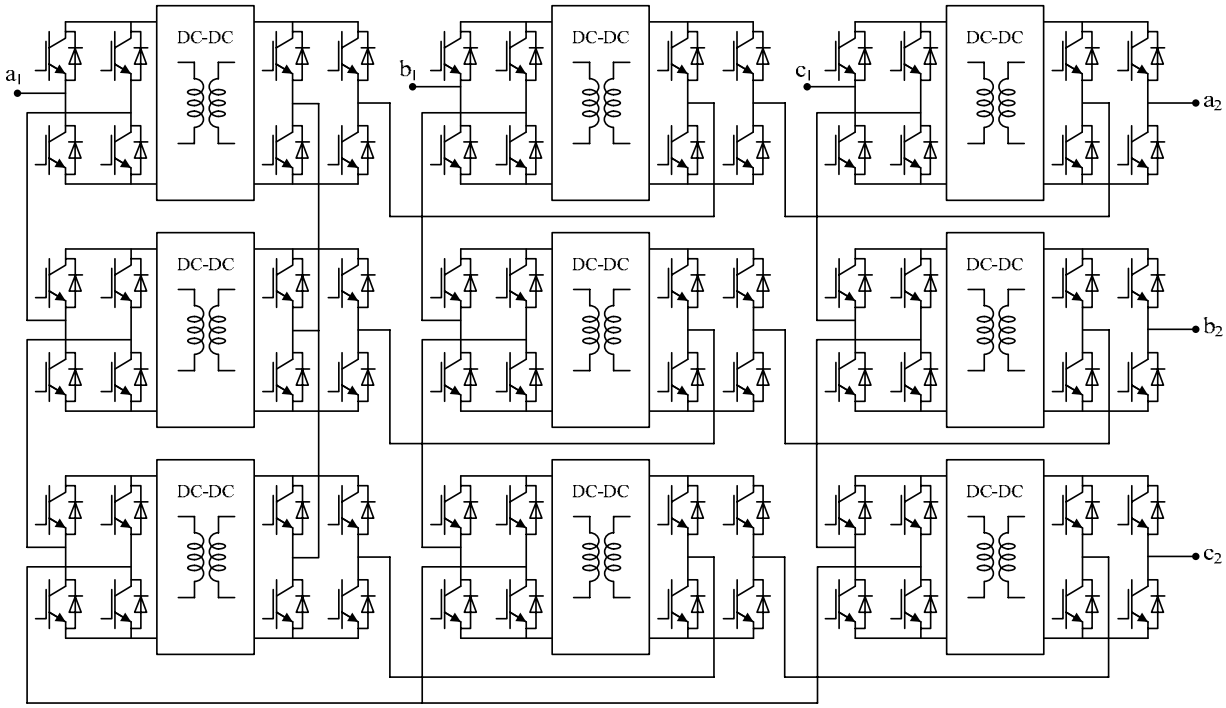
- Voltage ratio adjustment
- Frequency changing
- Phase changing
- Asymmetric load current cancellation
- Voltage asymmetry cancellation
- Reactive power control
- Active power control
- Harmonic cancellation
- UPFC like functionality

To achieve any of these functions, a number of control loops are required. These control loops include a current control loop, voltage control loop and capacitor balance loop implemented at port-A, a current control loop implemented at port-B and a current control loop at port-C. To implement the voltage control and capacitor balance loops a knowledge of all DC link voltages are necessary. At port-A in figure1.3 there are 12 capacitors, so 12 voltage transducers are required. Voltage transducers at medium voltage ratings are not easily to

implement and they can be expensive. This thesis presents an observation method for measuring the capacitor voltages to eliminate the need for DC link voltage measurements.



(a) The grid connection



(b) The two-port power converter topology

Figure 1.5: The two-port UNIFLEX-PM converter

1.1 Thesis Objectives

The main objective of this thesis is to choose and practically implement an efficient and robust dc-link voltage observer for the two-port power converter. Several observers including Luenberger Observer, Standard Kalman Filter (SKF), Extended Kalman Filter (EKF), Sliding Mode observer (SMO) and Sliding mode observer using the equivalent control method have been considered to be used in the two-port power converter. The main contribution of this thesis is to address the challenges of the capacitor voltage observation in the two-port power converter that are:

- Complex structure of the power converter doesn't allow having exact mathematical model of the system hence an approximated model of system has been used to construct the observer equations.

- The magnetizing and core loss currents in the medium frequency transformers of the DC-DC converters introduce error in the output current measurements.

- In practical cases the capacitance value are different from the nominal value and there is always uncertainty in capacitance.

- The system observability depends on the power converter switching states. The dc-link voltages are observable during a very small fraction of a switching period. The duration of observable states decreases as the number of cascaded H-bridges increases.

Therefore it is necessary to use an observer which is robust to uncertainties in the system model and parameter as well as measurement error. Several papers have been published in the field of dc-link voltage observation in multilevel power converters. An example of the dc-link voltage observation in a multicell power converter has been presented in [68]. The structure of a multicell power converter isn't complex and an exact mathematical model of the system can be used to develop the observer equations. Also there is no transformer in the structure of a multicell inverter to have magnetizing and core loss currents. Therefore in a multicell power converter there is no uncertainty in system model or parameters.

In order to select and implement an efficient observer for power converter, the performance of each type of observer in presence of uncertainty in the system model or parameters should be studied. The Luenberger observer isn't robust to uncertainty in the system model or parameters. The Kalman filter robustness to parameter uncertainty depends on the accurate value of the process and the measurement noise covariance matrices. Incorrect covariance matrices will reduce the robustness to parameter uncertainty and external noise [69]. The practical implementation of Extended Kalman Filter (EKF) involves significant numerical complexity [69]. The traditional sliding mode observer has no robustness to uncertainty in system parameters. The SMO using the equivalent control method is robust against some uncertainty in system model or parameters and it is easy to implement.

In [68] a traditional sliding mode observer has been used for dc-link voltage observation in a multicell inverter as there is no uncertainty in system model or parameters. Obviously traditional SMO would not be a good choice for the two-port power converter. In this thesis a "Sliding Mode Observer (SMO) via Equivalent Control Method" has been chosen and implemented on a two-port configuration, shown in figure 1.5. The selected observer generates precise observer results in presence of model uncertainty introduced by DC-DC converters.

The circuit in figure 1.5 is a subset of the full UNIFLEX-PM topology and has been chosen to demonstrate the functionality of the observer and this will be justified in chapters two and five.

1.2 Thesis plan

Chapter two presents the complete converter design and simulation results. Implementation of voltage and current control loops, as well as the design of the capacitor voltage balancer, is described in this section. The converter modulation technique is also presented. The design of the DC-DC converter and control is explained. Finally simulation results are presented.

Chapter three presents a theoretical study on sliding mode observers. The sliding mode observer via equivalent control method is introduced. A comparison is made between sliding

mode observers using *sgn()* and *sat()* functions. A stability study is presented on the observer in sliding mode and finally simulation results are presented for the observer operation.

Chapter four presents the simulation results of sliding mode observer applied to the UNIFLEX-PM power converter. The converter observable states are considered and presented based on converter switching states. The effect of DC-DC converters on system and observer equations is examined. Sliding mode observer equations for the two port converter is developed and simulation results are presented.

Chapter five describes the experimental power converter and associated control platform. Details of the H-bridge power circuit cards and selected IGBT devices are presented. Design of the high frequency analog controller card for DC-DC converter is also described. Details of the optical interface card used between FPGA and H-bridge cards, as well as voltage and current transducers are presented. The structure of the control platform including the DSP, FPGA and HPI-daughtercard are described. The implementation of the controller and observer equation on DSP and FPGA are presented. Finally the practical results of converter including converter voltage and current as well as dc-link voltages across DC-DC converters are presented.

Chapter six presents the experimental implementation of the sliding mode observer on power converter. Finally the practical results of power converter DC voltage observation are presented.

Chapter seven presents a conclusion for whole project including the observer design and implementation.

Chapter 2

Converter Design and Simulation

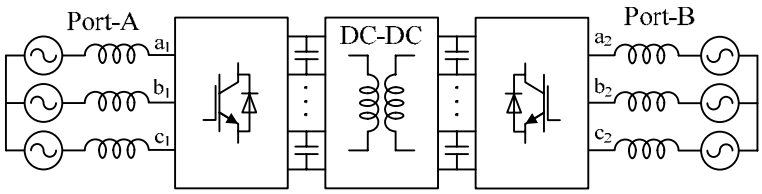
2.1. Introduction

This chapter presents the design and simulation of the converter and associated control for the two-port power converter. The converter modelling and the implementation of the control loops are described. A controller is used to control both active and reactive power flow at the ports of the power converter. PI regulators are used in voltage and current control loops, as well in the control of the capacitor voltage balancers. DQ transformations are used to decouple the system equations. The converter is modulated using a Phase Shifted Cascaded PWM technique. A brief introduction for the DC-DC converter and associated control is also presented. Finally, simulation results for the complete converter are presented.

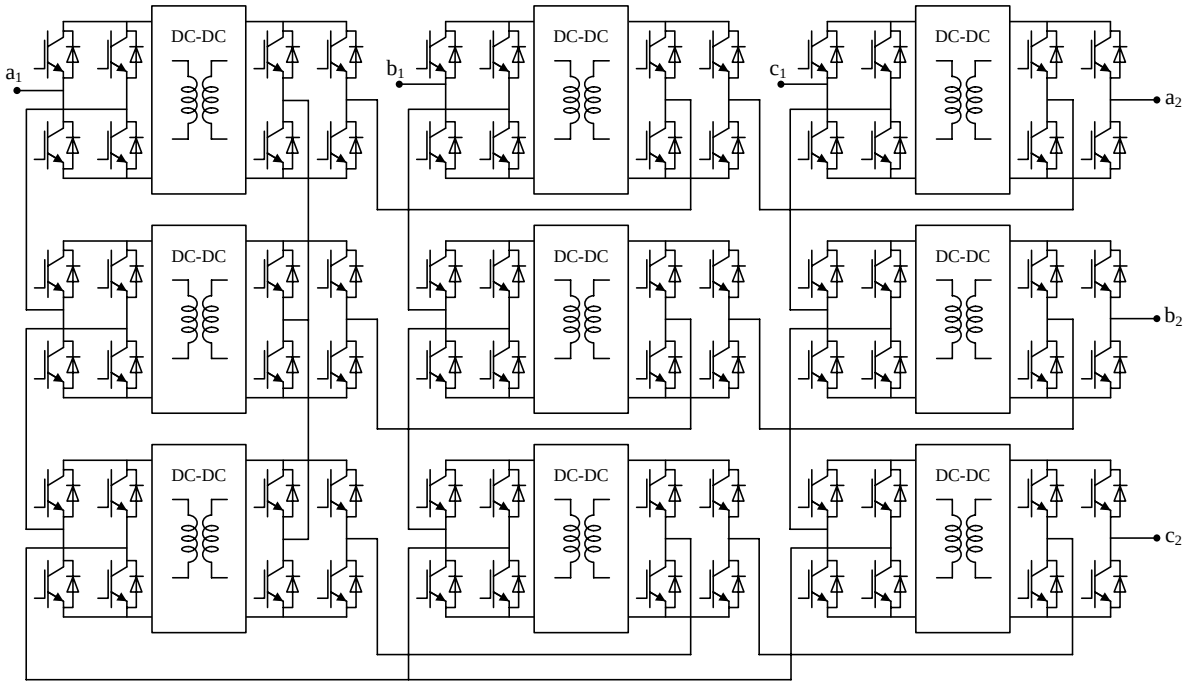
2.2. Power converter structure

The structure of the two-port power converter is shown in figure 2.1. The main characteristic of this power converter is the modular structure and the interleaved connection between

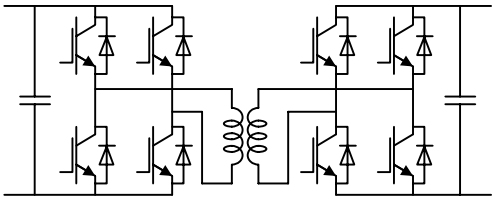
phases at the different ports. Maintenance and control of modular structure is relatively easy, fast and cost effective. Also, by having an interleaved connection between phases, this converter is able to operate under unbalanced conditions on one port while maintaining balance on the other ports.



(a) The power converter diagram.



b) The two-port power converter topology.



(c) The DC-DC converter topology.

Figure 2.1: The 2-port power converter

Out of the main multilevel power converter structures (Diode-Clamped Inverter, Capacitor-Clamped inverter, Cascaded H-Bridge Inverter and M2C), are the M2C and cascaded H-bridge multilevel converter that have a modular structure [12][13][14][15][64][65][66][67].

2.3. H-Bridge converter

The H-bridge converter topology is shown in figure 2.2. The power flow in an H-bridge converter is bi-directional and the H-bridge converter can be used as both ac-to-dc rectifier and dc-to-ac inverter.

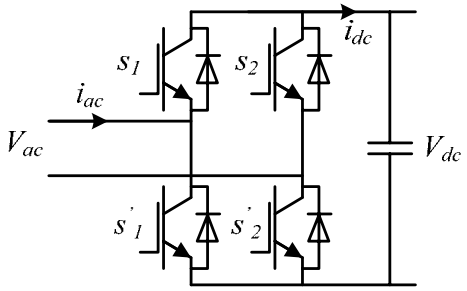


Figure 2.2: The H-Bridge converter

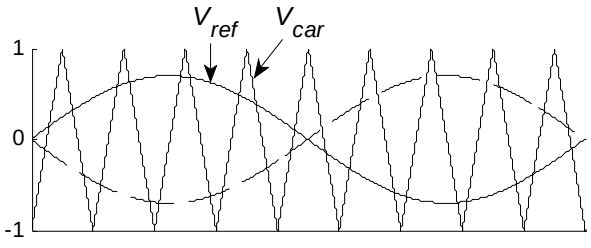
Pulse width modulation (PWM) is one of the most widely used strategies for controlling the AC output of power converters [16]. Both the amplitude and the frequency of AC output can be controlled by PWM technique. The basic naturally sampled PWM technique is based on comparing a reference signal V_{ref} with a triangular waveform V_{car}, which is also known as carrier waveform. The PWM strategy with a unipolar voltage switching technique [16][17] is selected as modulation technique for the H-bridge converter in this work. The PWM technique is shown in figure 2.3. Consider the following reference signal:

$$V_{ref} = M \sin(\omega t - \theta) \tag{2.1}$$

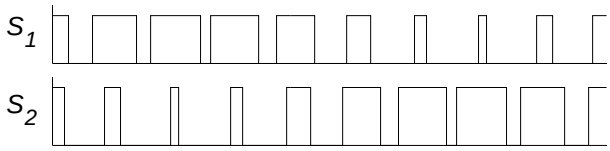
Where $0 < M < 1$. The switches are controlled by following rule:

s_1	s'_1	
ON	*OFF*	$V_{ref} > V_{car}$
OFF	*ON*	$V_{ref} < V_{car}$

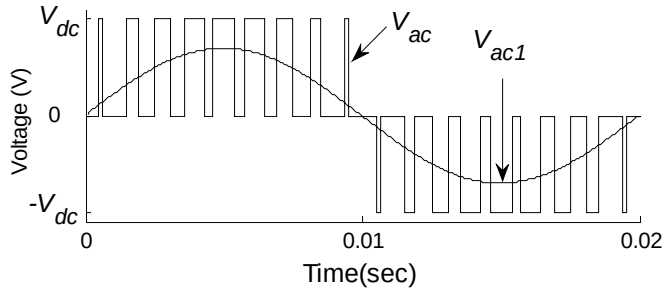
s_2	s'_2	
ON	*OFF*	$-V_{ref} > V_{car}$
OFF	*ON*	$-V_{ref} < V_{car}$



(a) Carrier and reference signals.



(b) Gate signals for switches S_1 and S_2.



(c) H-bridge output voltage V_{ac} and its fundamental component V_{ac1}

Figure 2.3: The unipolar voltage switching PWM technique for an H-bridge module.

The amplitude modulation ratio or modulation index is defined as the peak value of V_{ref} divided by the peak value of the V_{car}. If the peak value of V_{car} is set to 1 then:

$$\text{Modulation Index } = \frac{M}{1} = M \tag{2.2}$$

Where M is the peak value of V_{ref}. Figure 2.3 (c) shows the V_{ac} waveform and its fundamental-frequency component V_{ac1}. The relation between fundamental-frequency component V_{ac1} and dc-link voltage V_{dc} is:

$$V_{ac1} = V_{ref} \times V_{dc} = M.V_{dc} \sin(\omega t - \theta) \tag{2.3}$$

equation 2.3 described the relation between the AC and DC side voltages. In order to find the relation between the AC and DC sides currents it is assumed that the AC side current is sinusoidal:

$$i_{ac} = I_m \sin(\omega t) \tag{2.4}$$

Figure 2.4 presents the AC current i_{ac} and the DC current i_{dc}.

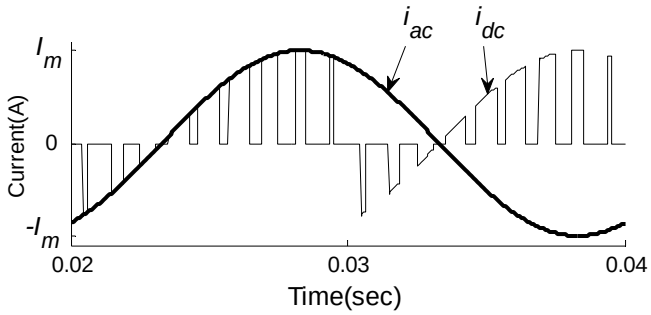


Figure 2.4: The i_{ac} and i_{dc} current waveforms.

The input power into an ideal, lossless converter is equal to the output power, therefore:

$$V_{dc} \times i_{dc} = V_{ac} \times i_{ac} \tag{2.5}$$

In order to simplify the calculations, all the harmonic components of i_{dc} and V_{ac} are neglected. V_{ac1} is the fundamental-frequency component of ac voltage V_{ac}. Combining equations 2.3 and 2.4 with equation 2.5 gives:

$$\begin{aligned} V_{dc} \times i_{dc1} &= V_{ac1} \times i_{ac} \\ &= M.V_{dc} \sin(\omega t - \theta) \times I_m \sin(\omega t) \\ &= \frac{M.V_{dc}.I_m}{2} \times (\cos\theta - \cos(2\omega t - \theta)) \end{aligned} \tag{2.6}$$

i_{dc1} is the dc current i_{dc} without harmonics and can be calculated as:

$$i_{dc1} = \frac{M.I_m}{2} \times (\cos\theta - \cos(2\omega t - \theta)) \tag{2.7}$$

The average model of H-bridge converter has been constructed using equations 2.1 to 2.7 and is shown in figure 2.5.

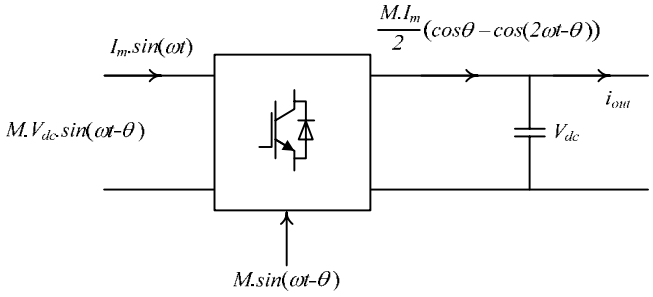
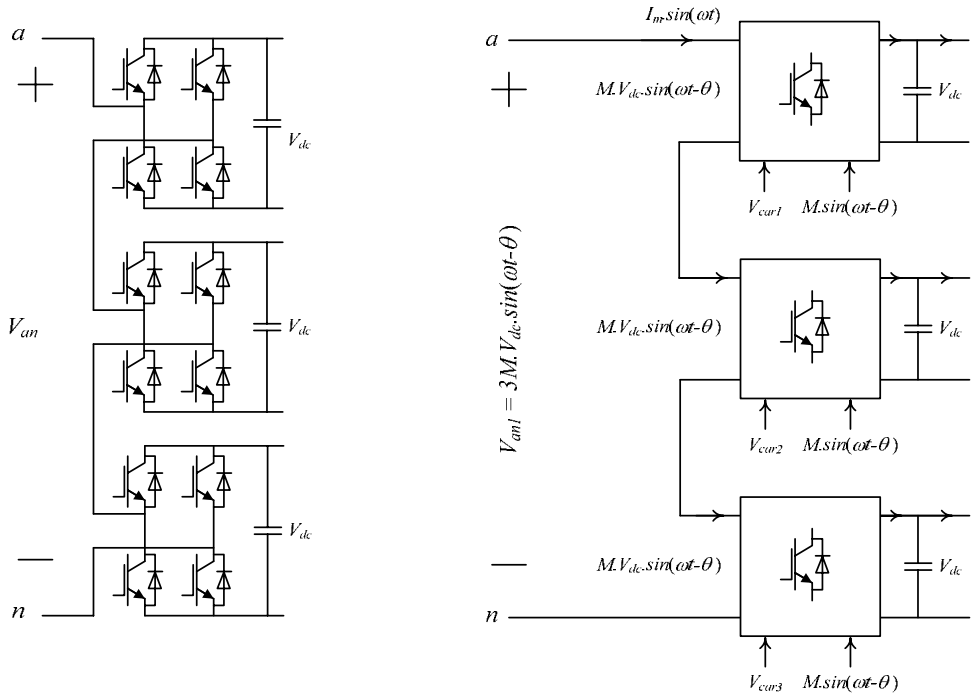


Figure 2.5: The average model of H-bridge converter.

The ac voltage and dc current are controlled by modulation index. The dc current has an average value and a sinusoidal component with double line frequency. The ac voltage fundamental component is equal to reference modulation signal multiplied by dc-link voltage.

2.4. Phase-Shifted Cascaded PWM

The phase-shifted cascaded PWM (PSCPWM) technique is one of modulation strategies used for cascaded multilevel converters. The multilevel cascaded H-bridge converter comprises of a series of connected single H-bridge converters. The PWM modulation technique for a single H-bridge converter is explained in the previous section. In the PSCPWM technique the same reference signal is applied to all the H-bridges and the carrier signal of each H-bridge is phase shifted by π/N where N is the number of cascaded H-bridges in the chain. It has been shown that optimum harmonic cancellation in the generated waveform can be achieved by phase shifting carrier signals by π/N radians [16]. The structure of a three cascaded H-brides is shown in figure 2.6(a) and the average model is shown in figure 2.6(b).



(a) Three cascaded H-bridges (b) Average model of CHB

Figure 2.6: The cascaded H-bridge converter structure

The multilevel converter ac voltage is equal to sum of ac voltage produced by each H-bridge. Figure 2.7 presents the output AC voltage and the carrier signals for three cascaded H-bridge converter which phase shifted by $\pi/3$ radians.

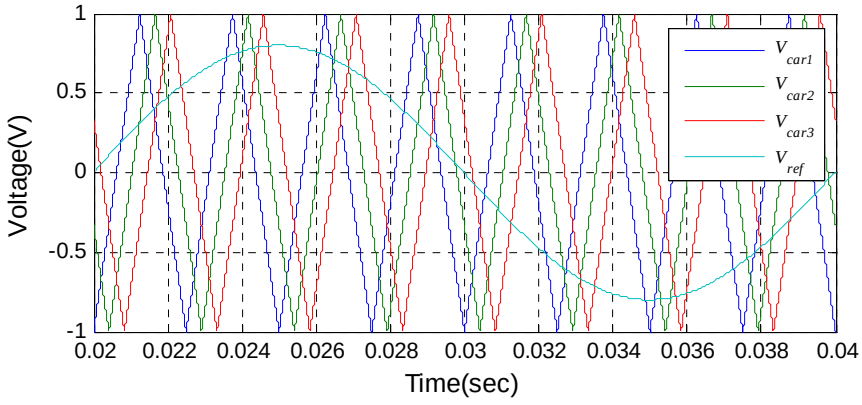


Figure 2.7: The phase shifted cascaded PWM technique for multilevel converters

The output ac voltage V_{an} can be a 7-level voltage and the fundamental component is:

$$V_{an1} = 3M.V_{dc}\sin(\omega t - \theta) \tag{2.8}$$

Where V_{dc} is the DC-link voltage and $M.\sin(\omega t - \theta)$ is the modulation reference signal. In an N cascaded H-bridges, the AC voltage levels can be up to $(2N + 1)$ levels depending on the modulation index M. Figure 2.8 shows the output ac voltage variation with modulation index.

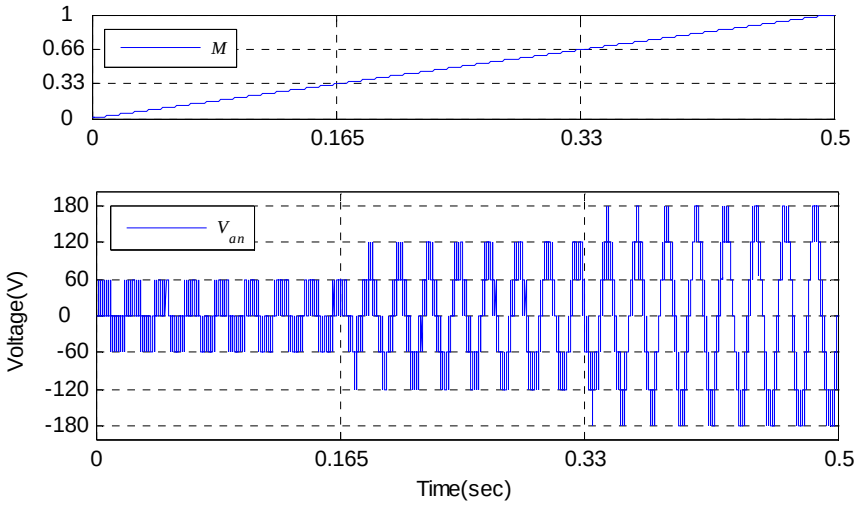


Figure 2.8: The ac voltage variation in PSCPWM technique with Modulation index

In a three cascaded H-bridges the ac voltage is three level for $0 < M < 0.33$, five level for $0.33 < M < 0.66$ and seven level for $0.66 < M < 1$.

2.5. Converter modeling and design

In this section the important equation for converter design has been derived. The prototype converter design and details are presented in chapter 5. It is assumed that the system operates under unity power factor condition. System rated power and voltage are two important factors in converter design. The grid connection of 2-port converter at port-A is shown in figure 2.9. The system rated power is $P = 1kW$ and the supply voltage peak value is $V_m = 100V$. The supply frequency is $50Hz$. The rated line current peak value I_m can be calculated as:

$$I_m = \frac{2P}{3V_m} = \frac{2 \times 1000}{3 \times 100} = 6.7A \tag{2.9}$$

The first step is to calculate the DC-link voltages. The relation between total dc-link voltage and source voltage is [17]:

$$total(V_{dc}) > \sqrt{2}\, V_m \tag{2.10}$$

There are three dc-link voltages in each phase, therefore:

$$V_{dc} > \frac{\sqrt{2}\, V_m}{3} \tag{2.11}$$

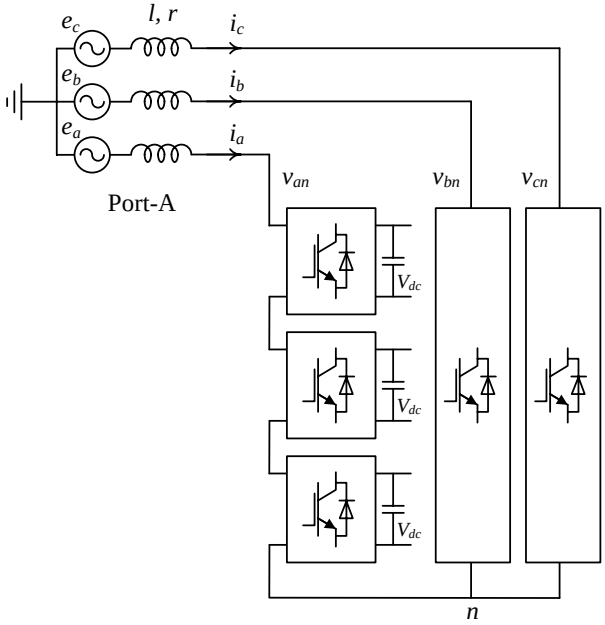


Figure 2.9: The grid connection of 2-port converter at port-A

The dc-link voltage V_{dc} is set to $60V$. Consider the phase-A voltage and current as:

$$e_a = V_m \sin(\omega t) \tag{2.12}$$

$$i_a = I_m \sin(\omega t) \tag{2.13}$$

$$V_{an} = 3M.V_{dc} \sin(\omega t - \theta) \tag{2.14}$$

Where V_m is the supply peak amplitude, I_m is the line current peak amplitude, V_{dc} is the DC-link voltage and M is the modulation index. Therefore the phasor-diagram of system operating under unity power factor condition will be:

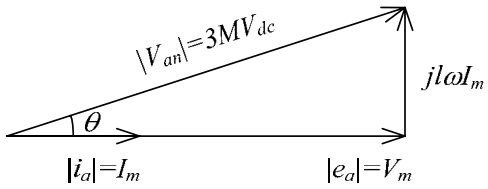


Figure 2.10: Phase-A phasor-diagram of power converter

The relation between the peak values of the source voltage, line current and converter voltage is:

$$(V_m)^2 + (l\omega I_m)^2 = (3MV_{dc})^2 \tag{2.15}$$

Where ω is the supply angular frequency. The linear range for M in PSCPWM technique is $0 < M < 1$ however the minimum operating M for this example occurs when line current is zero.

$$M_{min} = \frac{V_m}{3V_{dc}} = \frac{100}{3 \times 60} = 0.55 \tag{2.16}$$

The maximum modulation index is 1 and it is desirable to place the nominal modulation index in the middle, therefore the nominal modulation index can be taken as $M = 0.77$. The line inductance for this operating point can be calculates as:

$$l = \frac{\sqrt{(3MV_{dc})^2 - (V_m)^2}}{\omega I_m} = \frac{\sqrt{(3 \times 0.77 \times 60)^2 - (100)^2}}{100\pi \times 6.7} = 45.6mH \tag{2.17}$$

The available line inductance in the lab is $11mH$ and also it is large enough to filter the line current harmonics. The nominal modulation index for a $11mH$ inductance can be calculated as:

$$M = \frac{\sqrt{(V_m)^2 + (l\omega I_m)^2}}{3V_{dc}} = \frac{\sqrt{(100)^2 + (0.011 \times 100\pi \times 6.7)^2}}{3 \times 60} = 0.57 \tag{2.18}$$

The dc-link capacitance is designed in such a way to result in a reasonable DC-link voltage ripple. The dc-link input current is given in equation 2.7. It is assumed that the output current i_{out} is a constant dc current. During steady state the average value of input current will be

equal to output current and the sinusoidal component of input current causes capacitor voltage ripple. The capacitor equation during steady-state is:

$$c\frac{dV_{dc}}{dt} = \frac{M.I_m}{2}\cos(2\omega t - \theta) \tag{2.19}$$

The peak value of capacitor voltage ripple can be calculated as:

$$(\Delta V_{dc})_{peak} = \frac{M.I_m}{4c\omega} \tag{2.20}$$

For this example a $1000\mu f$ capacitor at nominal operating condition will give a $3V$ peak capacitor voltage ripple.

$$(\Delta V_{dc})_{peak} = \frac{0.57 \times 6.7}{4 \times 0.001 \times 100\pi} = 3V \tag{2.21}$$

$$\%(\Delta V_{dc})_{peak} = \frac{(\Delta V_{dc})_{peak}}{V_{dc}} = \frac{3}{60} = 5\% \tag{2.22}$$

The dc-link voltage ripple is 5% and is less than maximum limit.

2.6. Control loops modeling and design

The power converter diagram considered in this investigation and associated controllers at each port are shown in figure 2.11. Active and reactive power flow controllers can be used for each port of power converter and can be operate independently.

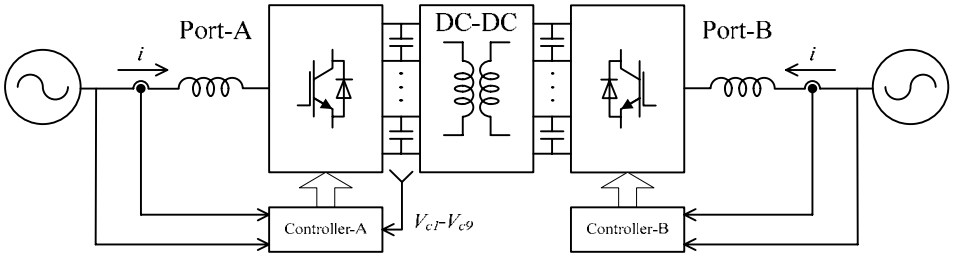


Figure 2.11: The power converter diagram with grid connection.

The active and reactive power flow can be controlled by controlling the line currents. The line current can be controlled by converter voltages. Therefore the current control loop should generate references for converter voltages. The diagram of current controller is shown in figure 2.12.

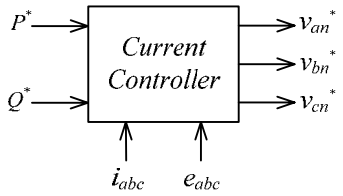


Figure 2.12: Current controller

The demanded active and reactive powers are the reference values for current controller. The supply voltage and line current are the feedback signals. The current controller output is the references for converter voltages. Based on the reference converter voltages the PSCPWM generates reference modulating signals for H-bridges. The current controller design process is described in detail in section 2.6.1.

The objective of active power flow controller at port-A is to maintain dc voltages of all the capacitors at a specified, fixed value. The dc-link voltages are controlled by active power flow between supply and converter. Therefore voltage controller should generate reference for active power in order to maintain average dc-link voltages at a reference value. Figure 2.13 shows the diagram of voltage controller.

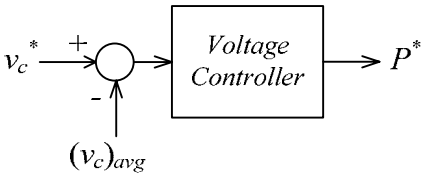


Figure 2.13: Voltage controller

The voltage controller output is the reference for port-A active power. The design details are explained in section 2.6.2.

The dc-link voltage of each H-bridge in multilevel converter would diverge under any unbalance conditions in network. In order to equalize all dc-link voltages a capacitor voltage balancer can be used at port-A. As explained in section 2.3, each individual capacitor voltage can be controlled by the average value of current flowing into the capacitor. The dc current in each H-bridge converter is described by equation 2.7. The average value of dc current is proportional to the modulation index and line current amplitude. The capacitor voltage balancer generates modified modulation index for each H-bridge converter. Figure 2.14 shows the capacitor voltage balancer.

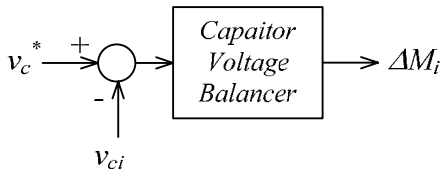


Figure 2.14: Capacitor voltage balancer

The controller at port-A comprises of a voltage control loop, a current control loop and a capacitor voltage balancer. At port-B there is only a current control loop to deliver the demanded active and reactive power to the network. Figure 2.15 shows the port-A controller structure.

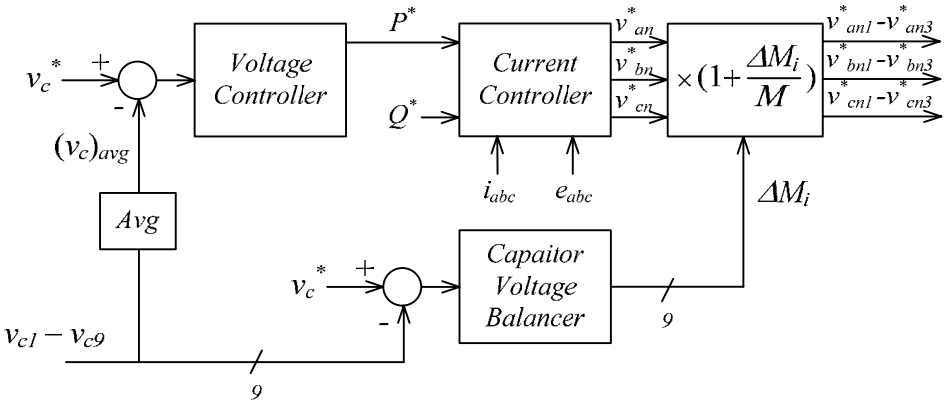


Figure 2.15: Port-A controller.

Signals $v^*_{an1}-v^*_{an3}$, $v^*_{bn1}-v^*_{bn3}$ and $v^*_{cn1}-v^*_{cn3}$ are used by PSCPWM to generated reference modulating signals for three H-bridges in phase-A, phase-B and phase-C respectively. Three mathematical models are developed for current control loop, voltage

control loop and capacitor voltage balancer. PI regulators are used in the control loops and are tuned using the MATLAB sisotool GUI [18]. The modelling and design of each controller is described in the following sections.

2.6.1. The current control loop

The objective of the current control loop is to set the amplitude and phase of three-phase line currents to reference values. The current control loop should generate references for v_{an}, v_{bn} and v_{cn} in order to achieve these desired line currents. A mathematical model of the circuit in figure 2.9 is used to design the current loop. The voltage equations for the three-phase system are:

$$[e]_{abc} = (r + l\,s)[i]_{abc} + [v]_{abc} + [v_n] \tag{2.23}$$

With:

$$[e]_{abc} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad [v]_{abc} = \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad [i]_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad [v_n] = \begin{bmatrix} v_n \\ v_n \\ v_n \end{bmatrix} \tag{2.24}$$

Where r is the line resistance. If the three-phase supply is balanced and free from harmonic then the voltage of point n will be:

$$v_n = \frac{-(v_{an} + v_{bn} + v_{cn})}{3} \tag{2.25}$$

Replacing the v_n in equation 2.23 will result in following equation in matrix form:

$$[e]_{abc} = (r + l\,s)[i]_{abc} + [B][v]_{abc} \tag{2.26}$$

Where:

$$[B] = \begin{bmatrix} \frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{2}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{-1}{3} & \frac{2}{3} \end{bmatrix} \tag{2.27}$$

Equation 2.26 contains ac variables that are not decoupled. It is much easier to analyze a decoupled system with dc variables. Applying $\alpha\beta$ and dq transformations to equation 2.26 will result in a decoupled system equation with dc variables [19][20]. The $\alpha\beta$ and dq transformations are explained below [21][22][23]. Consider a balanced three-phase voltage source defined by:

$$e_a = V_m \cos(\omega_e t) \qquad (2.28-a)$$

$$e_b = V_m \cos(\omega_e t - 120^\circ) \qquad (2.28-b)$$

$$e_c = V_m \cos(\omega_e t - 240^\circ) \qquad (2.28-c)$$

Where ω_e is the supply angular frequency. These voltage waveforms can be transformed into $\alpha-\beta$ coordinates as follows [21]:

$$\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}$$

$$= \sqrt{\frac{3}{2}} \begin{bmatrix} V_m \cos(\omega_e t) \\ V_m \sin(\omega_e t) \end{bmatrix} \qquad (2.29)$$

These voltages can be defined in a new reference frame which is rotating at the same speed as the AC supply frequency. Figure 2.16 shows the $\alpha-\beta$ voltages in this rotating reference frame.

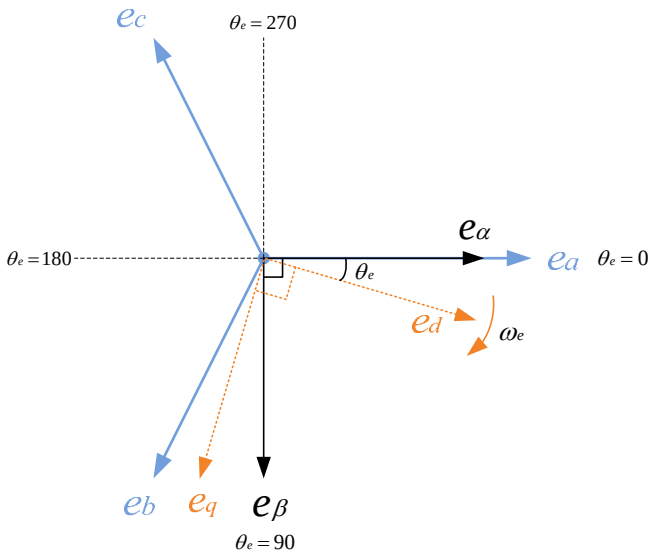


Figure 2.16: Stationary and rotating reference frames

The instantaneous angle between rotating voltages and α axis is:

$$\begin{aligned}\theta_e &= \tan^{-1}\left(\frac{e_\beta}{e_\alpha}\right)\\ &= \tan^{-1}\left(\frac{\sin(\omega_e t)}{\cos(\omega_e t)}\right)\\ &= \tan^{-1}(\tan(\omega_e t))\\ &= \omega_e t\end{aligned} \tag{2.30}$$

The projection of e_α, e_β onto the rotating reference frame will result in new imaginary variables e_d, e_q. The relation between $[e]_{abc}$ and $[e]_{dq0}$ coordinates is:

$$[e]_{dq0} = T[e]_{abc} = \begin{bmatrix}\sqrt{3/2}\,V_m\\ 0\\ 0\end{bmatrix} \tag{2.31}$$

Where

$$T = (T^{-1})^T = \sqrt{\frac{2}{3}} \times \begin{bmatrix}\cos\theta_e & \cos\left(\theta_e - \frac{2\pi}{3}\right) & \cos\left(\theta_e + \frac{2\pi}{3}\right)\\ \sin\theta_e & \sin\left(\theta_e - \frac{2\pi}{3}\right) & \sin\left(\theta_e + \frac{2\pi}{3}\right)\\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2}\end{bmatrix} \tag{2.32}$$

The three phase currents can be transformed to rotating reference frame.

$$[i]_{dq0} = T[i]_{abc} \tag{2.33}$$

Application of dq transformation from equation 2.26, results in equation 2.34.

$$T^{-1}[e]_{dq0} = (r + l\,s)T^{-1}[i]_{dq0} + [B]T^{-1}[v]_{dq0} \tag{2.34}$$

The simplified form of equation 2.34 in the dq rotating reference frame is presented in equations 2.35 and 2.36.

$$e_d = v_d + r.i_d + l\frac{d}{dt}i_d + l.\omega_e.i_q \tag{2.35}$$

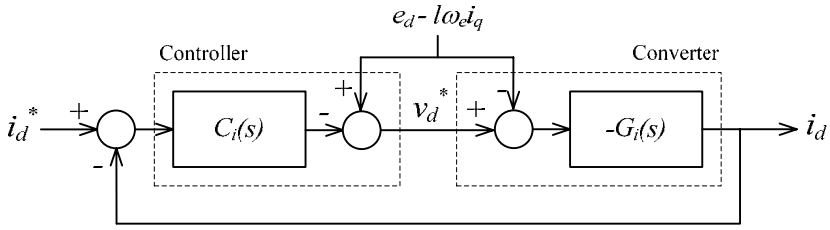
$$0 = v_q + r.i_q + l\frac{d}{dt}i_q - l.\omega_e.i_d \tag{2.36}$$

The i_d and i_q are decoupled and can be controlled independently. Rearranging the above equations results in:

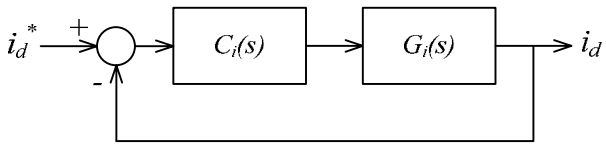
$$i_d = \frac{v_d - \left(e_d - l.\omega_e.i_q\right)}{-(r + ls)} \tag{2.37}$$

$$i_q = \frac{v_q - \left(e_q + l.\omega_e.i_d\right)}{-(r + ls)} \tag{2.38}$$

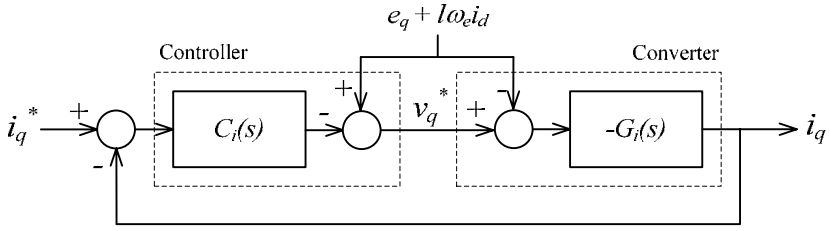
The current control loop should generate reference for v_d and v_q in order to control i_d and i_q to the desired value.



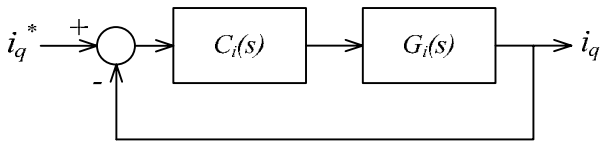
(a): The i_d control loop



(b): The simplified i_d control loop



(c) The i_q control loop



(d) The simplified i_q control loop

Figure 2.17: Current control loops

The plant dynamic $G_i(s)$ for current control loop is:

$$G_i(s) = \frac{1}{(ls + r)} \tag{2.39}$$

The current control loops are shown in figure 2.17. The plant $G_i(s)$ can be controlled by a PI controller. The root locus design method can be used to design the PI controller [24]. The maximum speed of current control loop is limited because of line inductor saturation. The speed of inductor current change depends on the voltage across the inductor. A fast current control loop, applies a big voltage on inductor, which may saturates the line inductor. Therefore a bandwidth of $95Hz$ is chosen for closed loop current control system to avoid any possible saturation of inductor. The current controller has been designed for an example circuit shown in figure 2.9 with the following parameters:

The peak supply voltage	V_m	$100V$
The peak line current	I_m	$6.7A$
The DC link voltage	V_{dc}	$60V$
The supply frequency	f	$50Hz$
The line resistance	r	0.5Ω
The line inductance	l	$11mH$
The DC-link capacitance	C	$1000\mu F$

Table 2.1: system parameters

The plant dynamics is:

$$G_i(s) = \frac{1}{(0.011s + 0.5)} \tag{2.40}$$

The designed PI controller transfer function is:

$$C_i(s) = 1160\left(\frac{0.0037s + 1}{s}\right) \tag{2.41}$$

Figure 2.18 presents the root locus, bode plots and step response for current control loop.

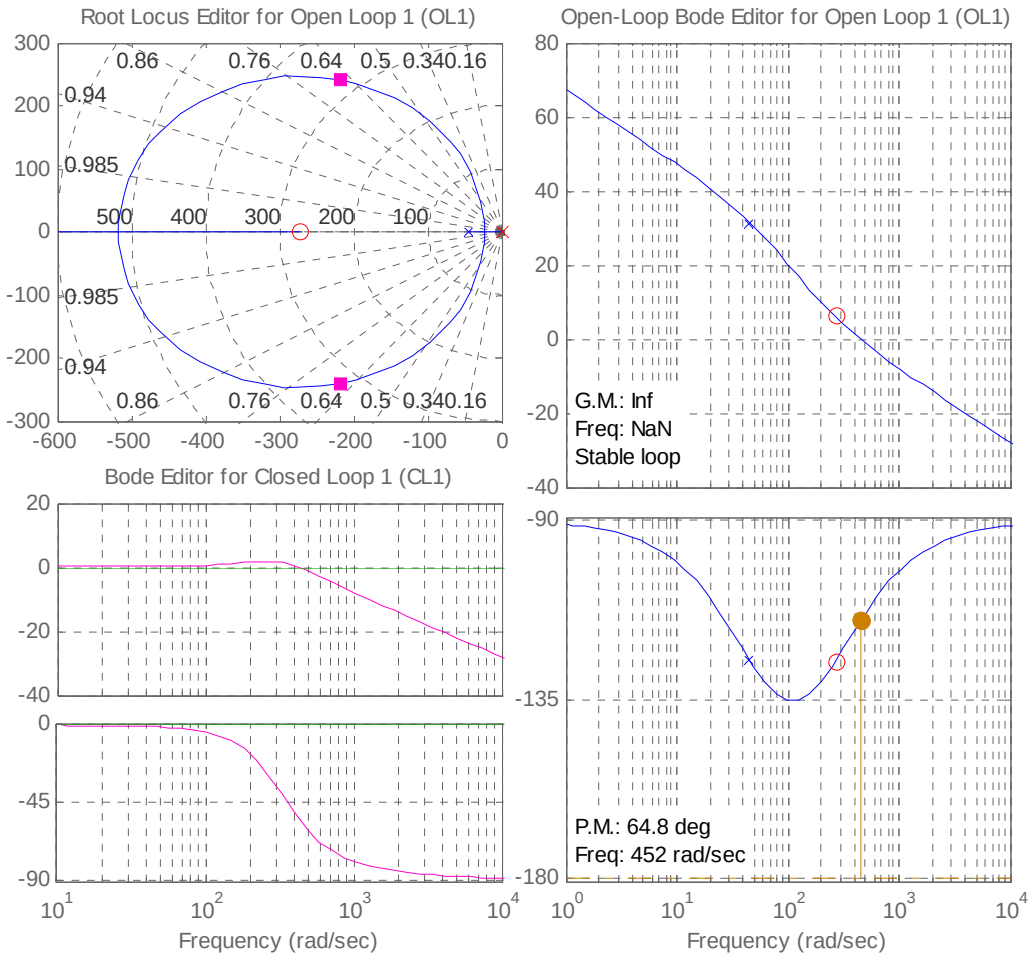


Figure 2.18(a): The root locus, bode plots for the current control loop

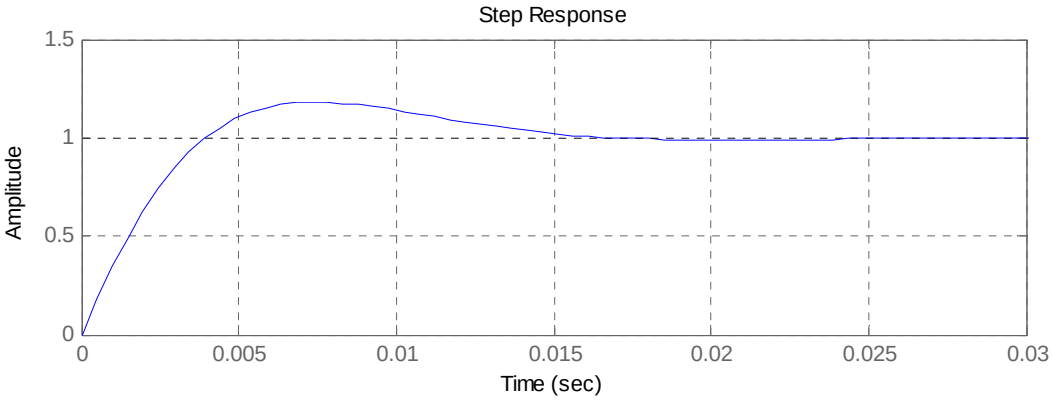
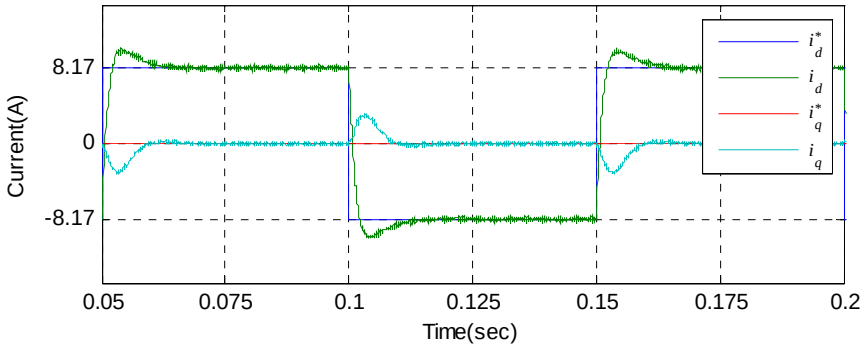
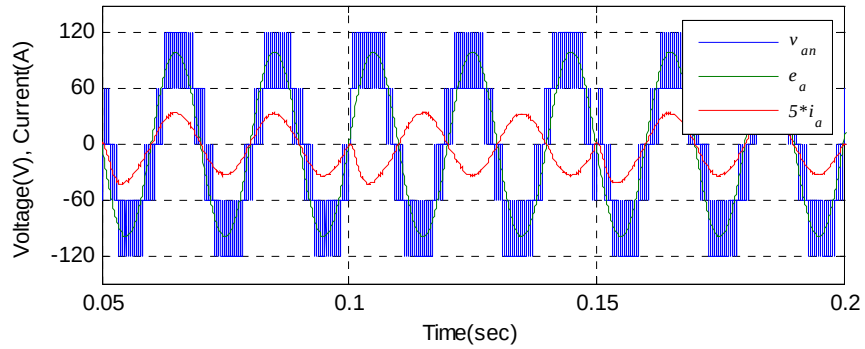


Figure 2.18(b): The step response for the current control loop

The poles of the closed-loop system are located at $-217 \pm i241$ and have a natural frequency equal to $325\ rad/s$. The damping ratio is set to be $\zeta = 0.67$. The open loop phase margin is 64.8° and gain margin is infinite. The simulation results of current control loops are presented in figure 2.19.



(a) The i_d, i_d^* and i_q, i_q^*.



(b) Supply voltage e_a, line current i_a and converter voltage v_{an}.

Figure 2.19: Current control loop simulation results.

It is assumed that the dc-links are connected to constant dc voltage source. The reference and actual values of i_d and i_q currents are shown in figure 2.19(a) and supply voltage and current and converter voltage are shown in figure 2.19(b). The Active power flow direction has been changed at $t = 50ms$, $t = 100ms$ and $t = 150ms$. During $50ms < t < 100ms$ the line current and supply voltage are in phase and power flow is from supply to converter and during $100ms < t < 150ms$ the power flow is from converter to supply. The simulation results confirm that the current control loop is stable in both direction of active power flow. Currents i_d and i_q can be controlled independently. The time for full current reversal is as expected and is equal to settling-time of closed-loop step-response.

2.6.2. The voltage control loop

The objective of the voltage control loop is to control the amplitude of the average of the DC link voltages. A net active power flow into the power converter will charge the capacitors. The voltage control loop should generate a reference for the active power in order to achieve the desired average of the converter dc-link voltages. The simplified circuit of the 2-port converter shown in figure 2.20 is used to design the voltage control loop. The load that is delivered to port-B is modelled as a resistor R.

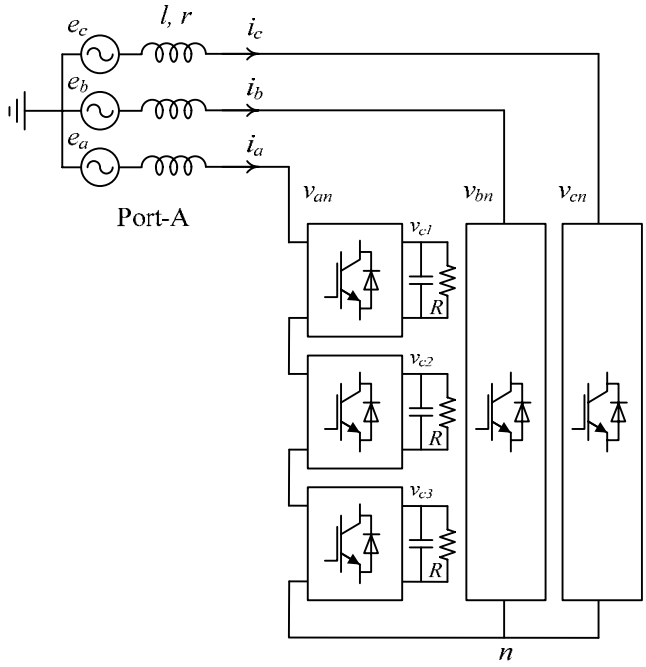


Figure 2.20: The simplified model of grid connection of 2-port converter at port-A

As shown in figure 2.1(b) there is nine modules in the 2-port converter. Assuming that all the modules in the power converter are symmetrical and lossless, the net active power supplied to each module will be one-ninth of the total active converter input power as given in equation 2.42.

$$\frac{1}{9}P = v_c(t)i_c(t) + \frac{v_c^2(t)}{R} = v_c\left(Cs\boldsymbol{v_c} + \frac{\boldsymbol{v_c}}{R}\right) \tag{2.42}$$

Where $P = e_d.i_d$ is the active input power to the converter. Voltage e_d is constant and active power flow is controlled by i_d. Rearranging equation 2.42 results in:

$$\boldsymbol{v_c} = \frac{e_D}{9v_c\left(Cs + \frac{1}{R}\right)} i_D \tag{2.43}$$

The plant dynamics for voltage control loop is:

$$G_v(s) = \frac{e_D}{9v_c\left(Cs + \frac{1}{R}\right)} \tag{2.44}$$

The voltage controller output is a reference for current i_d. The nested structure of voltage and current control loops is shown in figure 2.21.

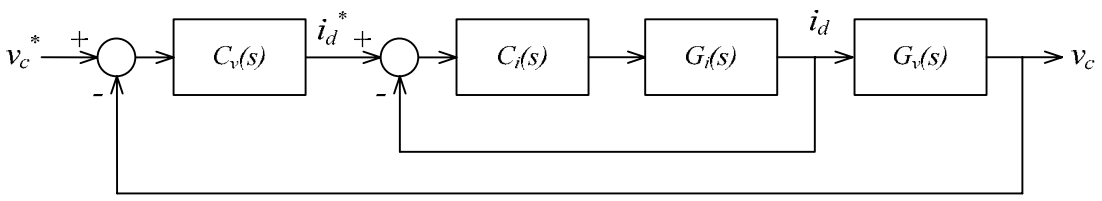


Figure 2.21: The nested control loop including voltage control loop and current control loop

If the voltage controller is significantly slower than current controller, therefore the speed of i_d^* changes is slow and i_d can track i_D^* very closely and it can be assumed that i_d is identical to i_d^*. Therefore the block diagram of figure 2.21 can be simplified to figure 2.22.

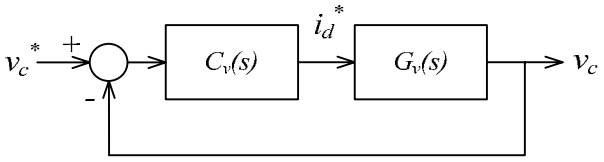


Figure 2.22: The voltage control loop

The maximum speed of voltage control loop is limited by line current rating. A fast voltage control loop imposes big line current. Also voltage control loop should be much slower than current control loop so the response of the nested loop to a step input be virtually identical to the voltage control loop response alone. For a current control loop with a bandwidth of $95Hz$ the voltage control loop bandwidth can be $6Hz$. The voltage controller has been designed for an example circuit shown in figure 2.20 with the following parameters:

The peak supply voltage	V_m	$100V$
The peak line current	I_m	$6.7A$
The DC link voltage	V_{dc}	$60V$
The supply frequency	f	$50Hz$
The line resistance	r	0.5Ω
The line inductance	l	$11mH$
The DC-link capacitance	C	$1000\mu F$
The load resistance	R	32Ω

Table 2.3: system parameters

The plant dynamics is:

$$G_v(s) = \frac{226.5}{(s + 31.25)} \tag{2.45}$$

The plant $G_v(s)$ can be controlled by a PI controller. The root locus design method can be used to design the PI controller. The PI controller transfer function is:

$$C_v(s) = 5.3\left(\frac{0.027s + 1}{s}\right) \tag{2.46}$$

Figure 2.23 shows the step responses of the current, voltage and nested control loops. It can be seen that the response of nested control loop to a step input is virtually identical to the voltage control loop response alone.

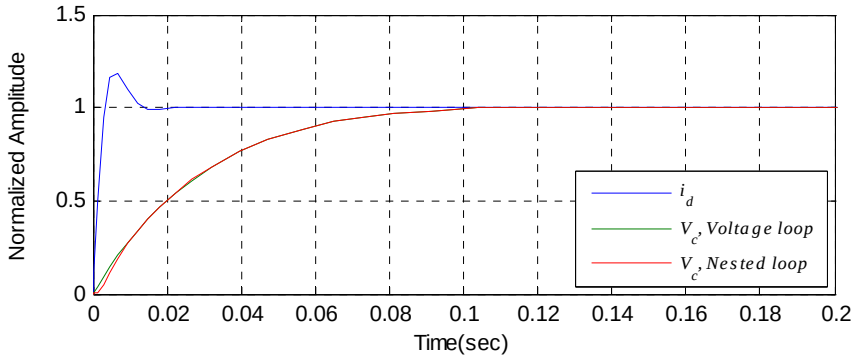


Figure 2.23: Step response of the current, voltage and nested control loop.

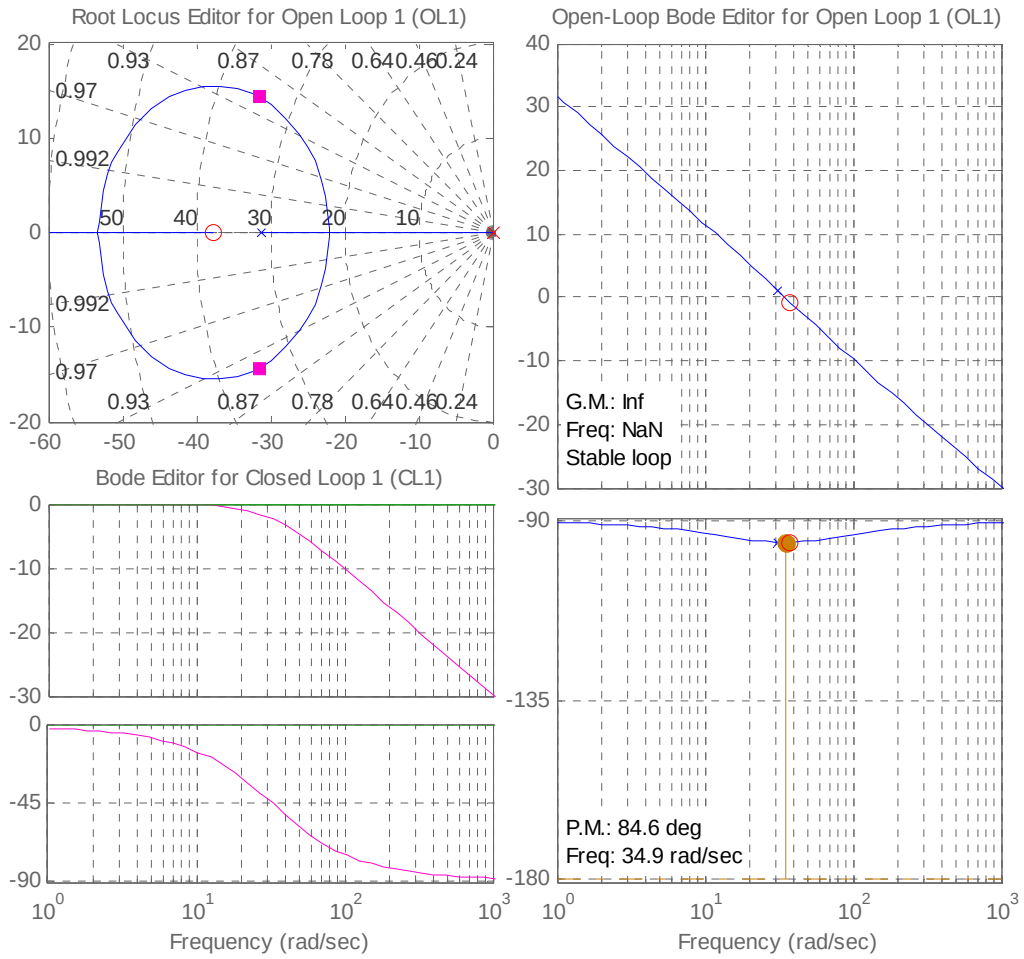


Figure 2.24(a): The root locus, bode plots for the voltage control loop

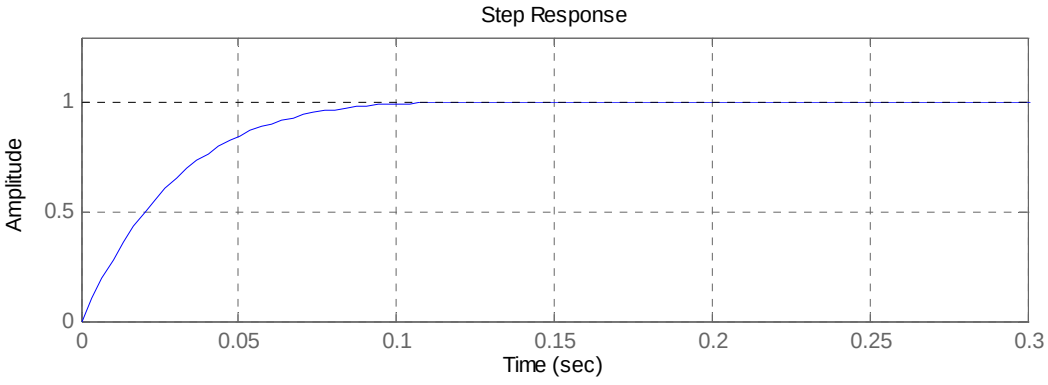
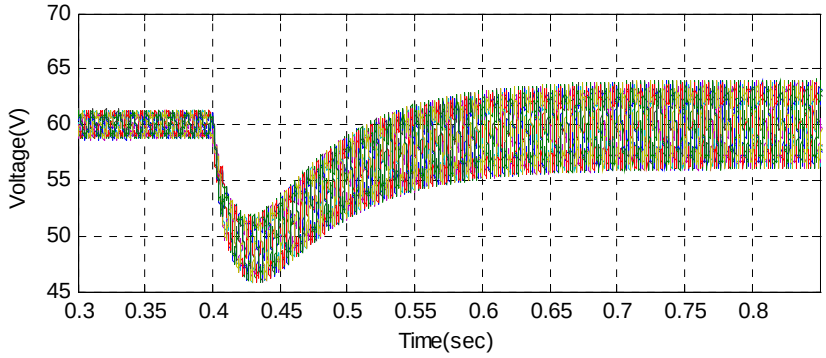


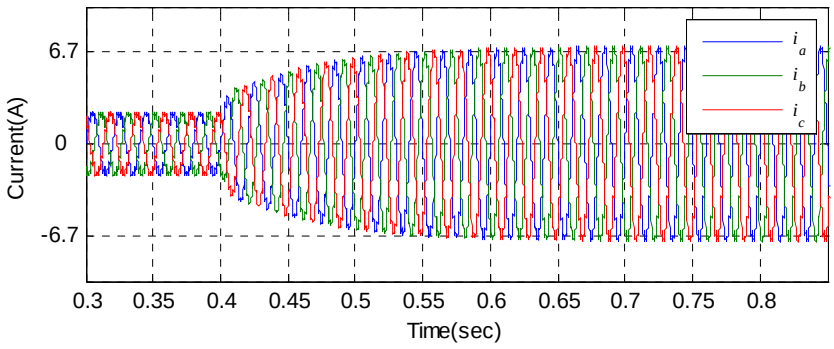
Figure 2.24(b): The step response for the voltage control loop

The root locus, bode plots and step response for voltage control loop are shown in figure 2.24. The poles of the closed-loop system are located at $-31.6 \pm i14.3$ and have a natural

frequency equal to $34.6\,rad/s$. The damping ratio is set to $\zeta = 0.91$. The open loop phase margin is 34.9° and gain margin is infinite.



(a) DC link voltages $v_{c1} - v_{c9}$.



(b) Line currents i_a, i_b and i_c .

Figure 2.25: Voltage control loop simulation results.

The simulation results are shown in figure 2.25. A step change in load resistance is applied at $t = 0.4s$. The load resistance is changed from 100Ω to 32Ω. Capacitor voltages are shown in figure 2.25(a). Simulation result confirms that voltage control loop is stable. After a step change in load the capacitor voltages converge to reference value in $20ms$. There is no steady state error in capacitor voltage values. The line currents are shown in figure 2.25(b). There is no over current situation which means the dynamic of the designed voltage controller is not too fast.

2.6.3. The capacitor voltage balancer

The objective of the capacitor voltage balancer is to equalize all the DC-link voltages in the H-bridges. Under any type of unbalance operating conditions the capacitor voltages would diverge without the capacitor voltage balancer control loop. The capacitor voltage balancer modifies the amplitude modulation ratio M of each cell to control the associated DC link voltage. The average model shown in figure 2.5 is used to design the capacitor voltage balancer loop. The capacitor voltage can be described by:

$$i_{dc} = i_c(t) + \frac{v_c(t)}{R} = Csv_c + \frac{v_c}{R} \tag{2.47}$$

The i_{dc} is described by equation 2.7. The average value of i_{dc} charges the capacitor. Placing the average value of i_{dc} in equation 2.47 results in:

$$\frac{MI_m}{2}\cos\theta \ = Csv_c + \frac{v_c}{R} \tag{2.48}$$

It is assumed that $\cos\theta$ is close to one. Under unity power factor condition the relation between peak amplitude of line current I_m and rotating current i_d is:

$$I_m = \left(\sqrt{2/3}\right) i_d \tag{2.49}$$

Rearranging equation 2.48 and combining with equation 2.49 results:

$$v_c = \frac{1}{\sqrt{6}\left(Cs + \frac{1}{R}\right)} M.i_d \tag{2.50}$$

As explained in section 2.6.2, figure 2.22, the reference value for the rotating current i_d is determined by voltage control loop. Figure 2.26 shows a block diagram of mathematical model of a single H-bridge including voltage controller and capacitor voltage balancer.

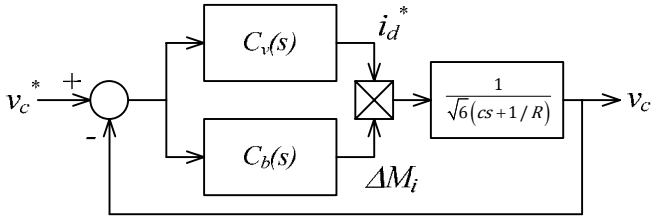


Figure 2.26: The model of single H-bridge including voltage controller and capacitor voltage balancer

If the capacitor voltage balancer is significantly slower than voltage control loop therefore current i_d can be considered as a constant. Based on this assumption and by using equation 2.50 the plant transfer function to design capacitor voltage balancer is:

$$G_b(s) = \frac{i_d}{\sqrt{6}\left(Cs + \frac{1}{R}\right)} \tag{2.51}$$

The capacitor voltage balancer diagram is shown in figure 2.27.

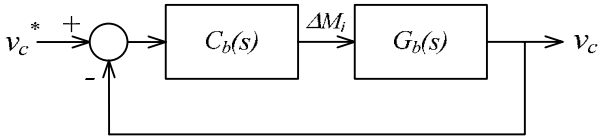


Figure 2.27: The capacitor voltage balancer loop

The plant $G_b(s)$ can be controlled by a PI controller. The root locus design method can be used to design the PI controller. The dynamic of capacitor voltage balancer should be significantly slower than voltage control loop. For a voltage control loop with a bandwidth of $6Hz$ the capacitor voltage balancer bandwidth can be $0.5Hz$. The plant for capacitor voltage balancer in this example is:

$$G_b(s) = \frac{i_d}{\sqrt{6}\left(Cs + \frac{1}{R}\right)} = \left(\frac{3350}{s + 31.25}\right) \tag{2.52}$$

The corresponding controller can be designed as:

$$C_b(s) = 0.04\left(\frac{1 + 0.1s}{s}\right) \tag{2.53}$$

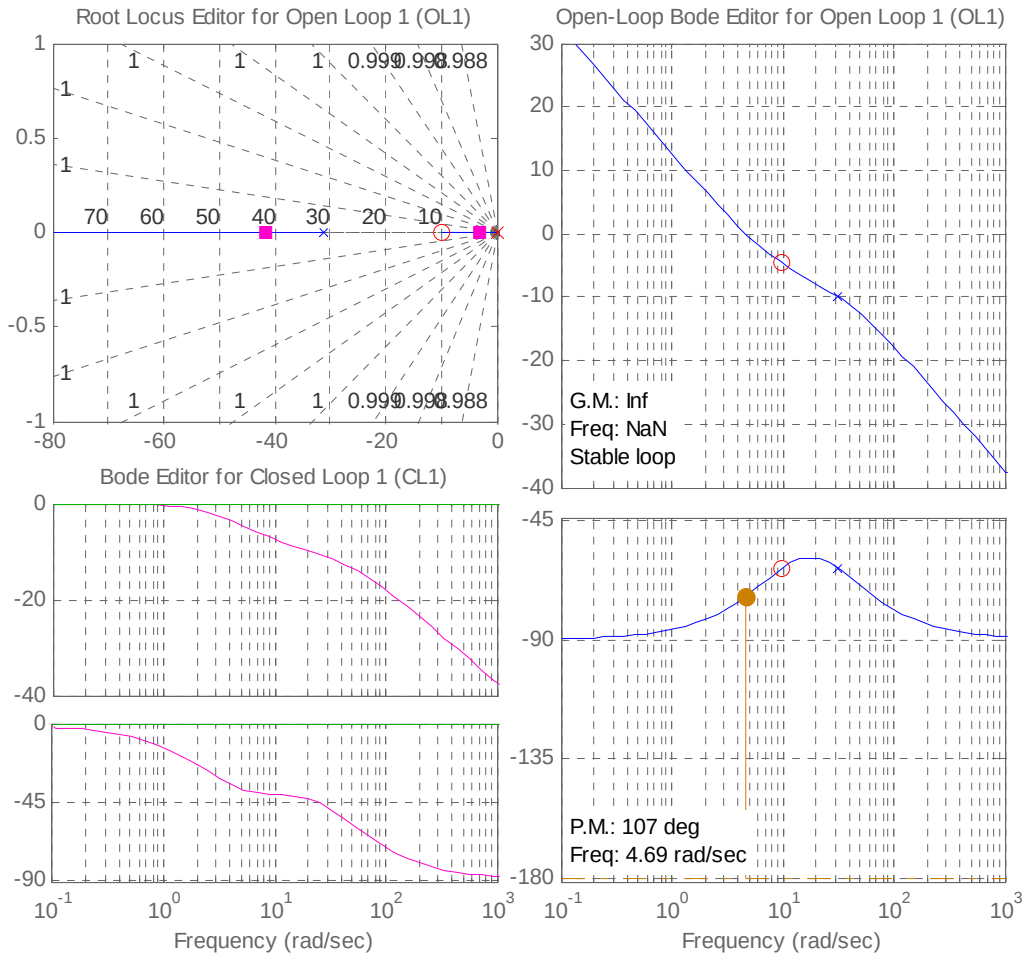


Figure 2.28(a): The root locus, bode plots for the capacitor voltage balancer loop

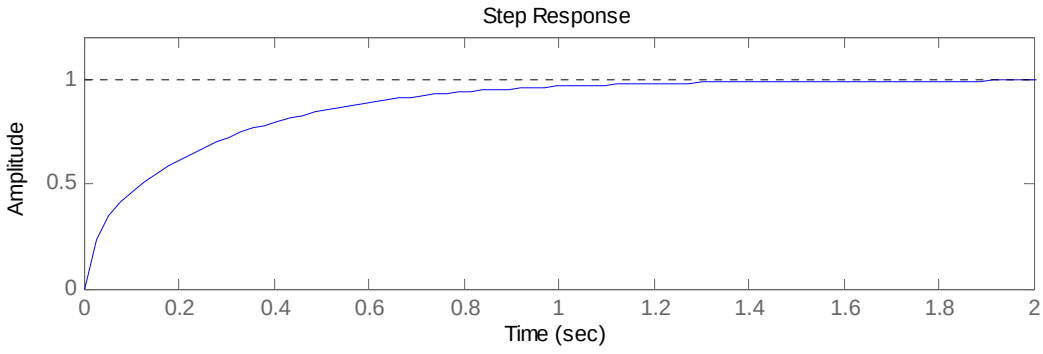


Figure 2.28(b): The step-response for the capacitor voltage balancer loop

The poles of the closed-loop system are located at -41.5 and -3.23. The settling time of step response is $1.2sec$. The open loop phase margin is 107° and gain margin is infinite. The

circuit shown in figure 2.20 is used to generate the simulation results for capacitor voltage balancer. The system parameters are listed in table 2.3. Step changes in load resistances R_1 and R_3 are applied at $= 1s$. The simulation results are presented in figure 2.29. Capacitor voltages v_{c1}, v_{c2} and v_{c3} without capacitor voltage balancer are shown in figure 2.29(a). Capacitor voltages diverge under unbalanced load condition without balancer.

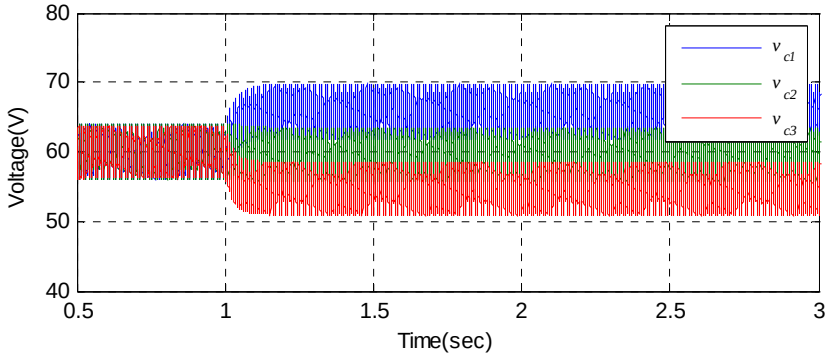


Figure 2.29 (a): voltage balancer loop (dc-link voltages v_{c1}, v_{c2} and v_{c3} without balancer loop)

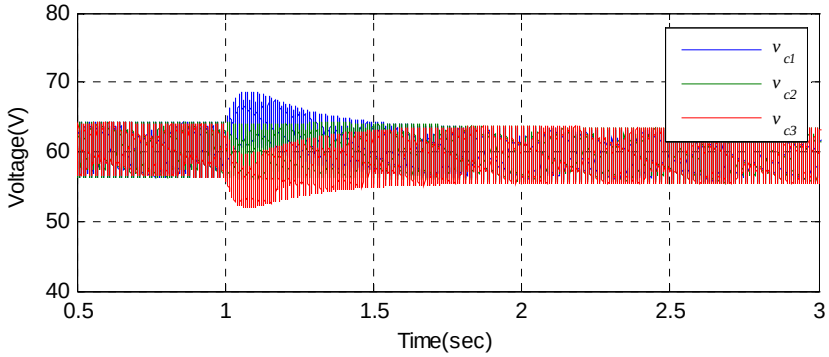
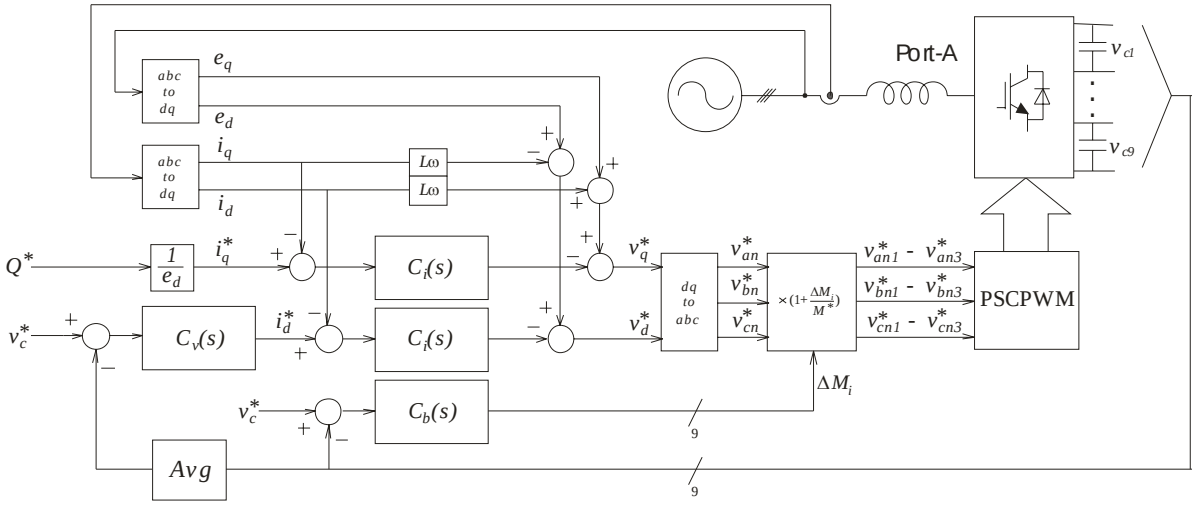


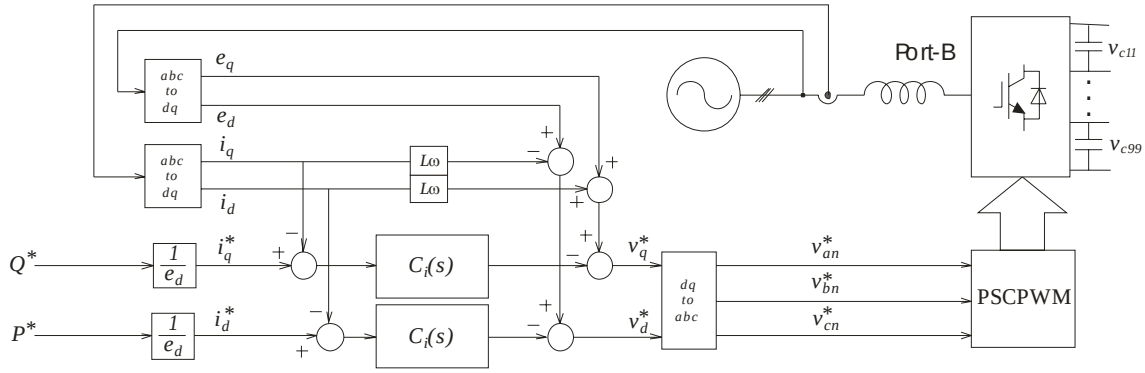
Figure 2.29 (b): voltage balancer loop (dc-link voltages v_{c1}, v_{c2} and v_{c3} with balancer loop)

Figure 2.29(b) shows the capacitor voltages v_{c1}, v_{c2} and v_{c3} under unbalanced load condition with capacitor voltage balancer. Simulation result confirms that capacitor voltage balancer is stable. There is no steady state error in capacitor voltage values.

The complete power converter and associated controllers for ports A and B are shown in figure 2.30. At port-A there is a current loop, a voltage loop and nine capacitor voltage balancers. There is only one current control loop for port-B, which controls the active and reactive power.



(a) Port-A controller diagram in detail.



(b) Port-B controller diagram in detail.

Figure 2.30: The complete controller diagram.

The controllers in figure 2.30 are designed under the assumption that the supply at both ports is balanced. The instantaneous angle of the rotating reference frame at each port is calculated using the supply voltage at that port therefore the converter can be connected to supplies with different frequencies and different phase angles. The reference value for the reactive power is set to zero to have unity power factor condition at both ports.

2.7. The DC-DC Converter

The DC-DC converter is used in the power converter structure to provide galvanic isolation between the H-bridges. The structure of the DC-DC converter is shown in figure 2.31. The DC-DC converter consists of two H-bridge converters and a medium frequency transformer. In this example the DC-DC converter is used to equalize the capacitor voltages v_{ci} and v_{cii}. The capacitor voltages are maintained and controlled by active power flow between the input and output of the DC-DC converter. The active power flow is controlled by controlling the phase shift between the square-wave voltages across transformer's leakage inductance L. The relation between active power flow and phase shift between the voltages is [25]:

$$P = \frac{v_{ci} \cdot v_{cii}}{\omega L}\left(\delta - \frac{\delta^2}{\pi}\right) \tag{2.54}$$

Where ω is the angular frequency of square-wave voltages and the δ is phase shift between the square-wave voltages across the leakage inductance of transformer.

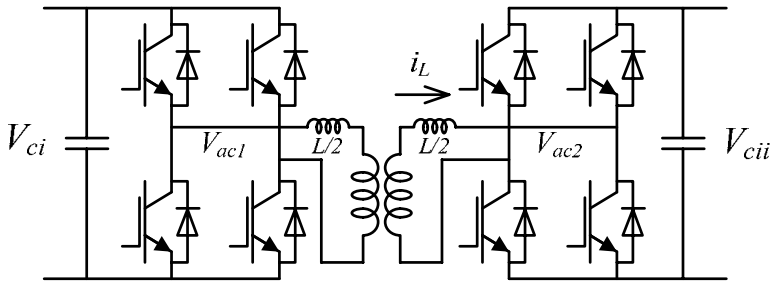


Figure 2.31: The DC-DC converter circuit

The DC-DC converter control diagram is shown in figure 2.32. The details of DC-DC converter and controller design used in this work can be found in [25].

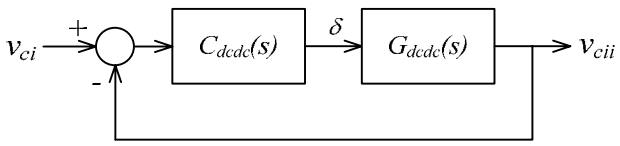


Figure 2.32: The DC-DC controller diagram

The voltages across transformer terminals and transformer current are shown in figure 2.33.

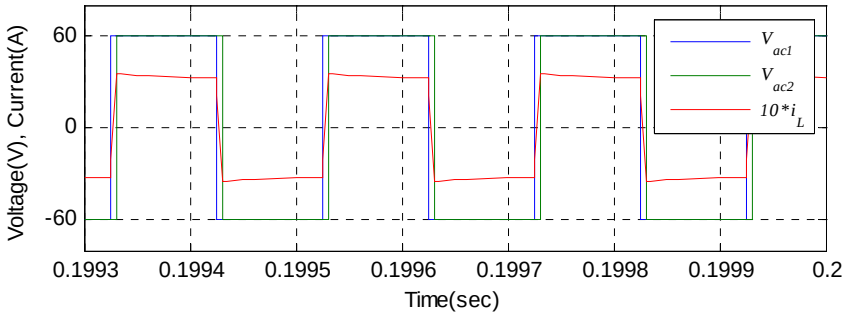


Figure 2.33: The DC-DC converter waveforms.

In this diagram V_{ac2} lags V_{ac1}which means that power flow is from left to right.

2.8. Simulation Results for the 2-Port Power Converter

In a two-port converter there are two capacitors in each module, either side of the DC-DC converters. By neglecting the dynamics of DC-DC converters it can be assumed that the two capacitors in each module will be in parallel and the equivalent capacitance will be doubled. Therefore the dynamics of a two port converter are different from a one-port converter and new voltage control loop and capacitor voltage balancer loop would need to be designed. However the current loop controller $C_i(s)$ is the same for a two-port and a one-port converter. The PI controller design procedure has been explained in detail in the previous section. Figure 2.34 shows the complete power converter topology used in these simulations. The peak amplitude of the three-phase supply voltages at both ports is taken as $100V$ with a frequency of $50Hz$. The line inductance is $11mH$. The DC link capacitance is $1000\mu F$ and the reference value for the DC link voltages is set to $60V$.

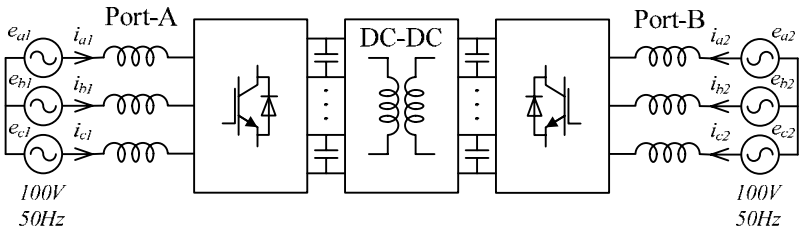
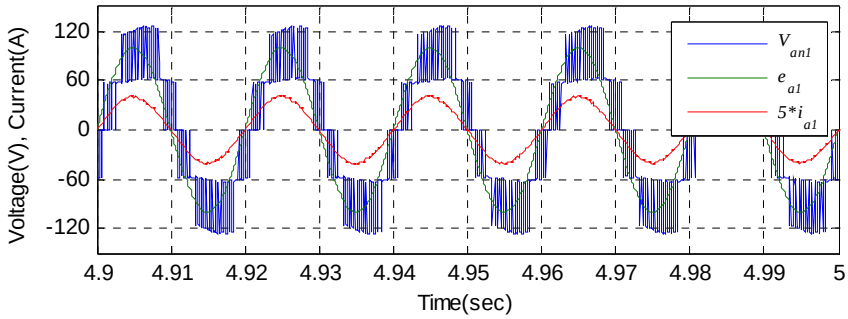
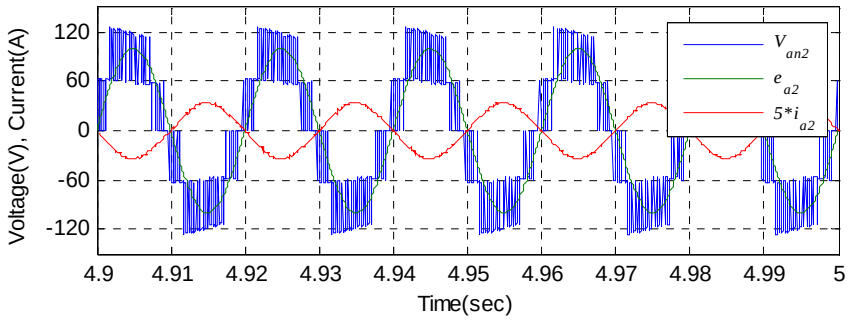


Figure 2.34: Complete power converter circuit diagram

Figure 2.35 shows the simulated waveforms of the ac current and voltages at ports A and B.



(a) Supply voltage e_{a1} , Converter voltage v_{an1} , and line current i_{a1} at phase-a, Port-A.



(b) Supply voltage e_{a2} , Converter voltage v_{an2} , and line current i_{a2} at phase-a, Port-B

Figure 2.35: Two-port converter waveforms.

The line current and supply voltage at port-A are in phase, showing the converter is operating under unity power factor condition. Also converter voltage lags the supply voltage which means port-A is delivering active power to converter. The converter voltage leads the supply voltage at port-B, which means port-B is absorbing active power from power converter. The power-converter is operating under unity power factor conditions at port-B as well.

Figure 2.36 shows the capacitor voltages across the DC-DC converters, which is switching at $5KHz$.

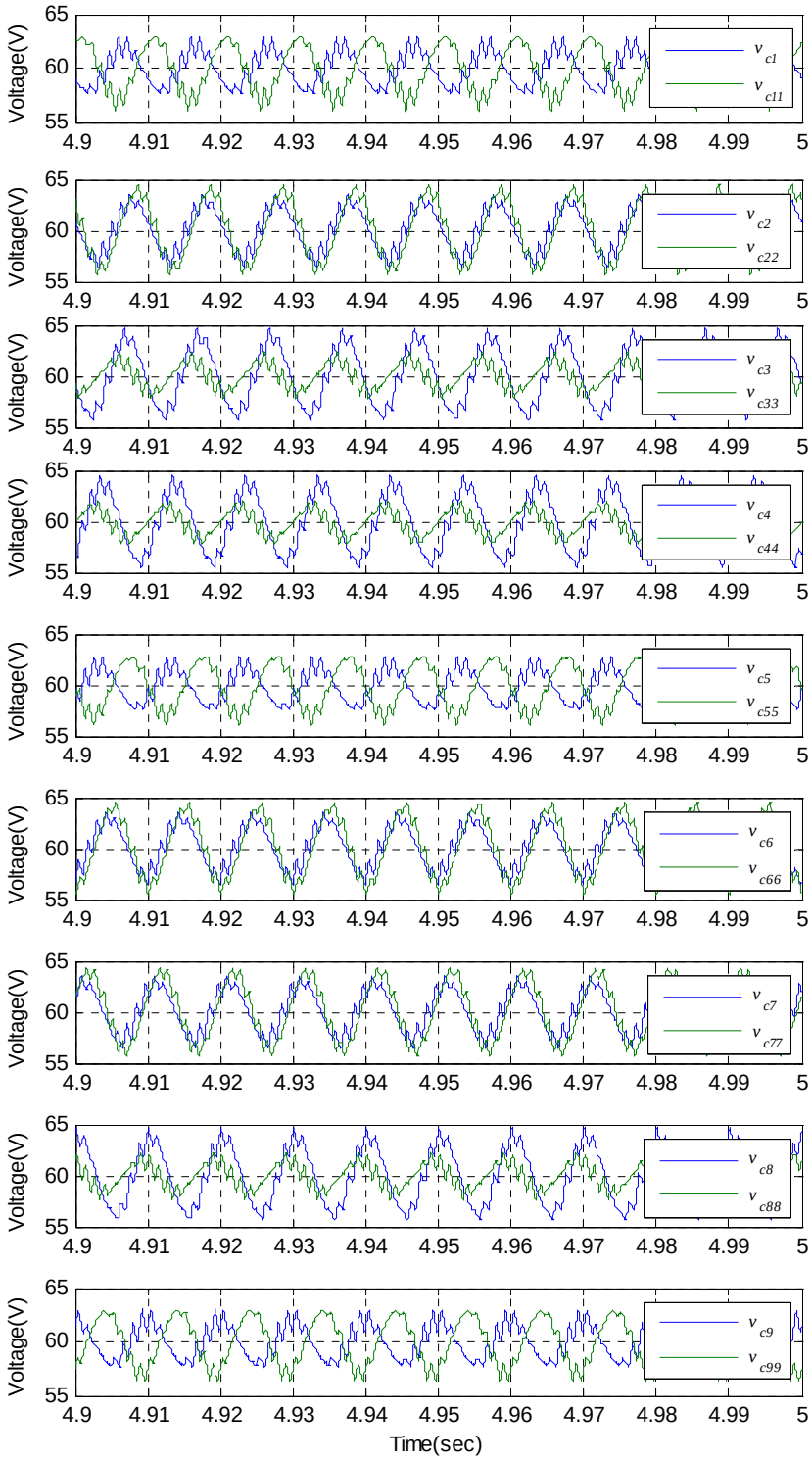


Figure 2.36: DC link voltages across DC-DC converters.

The average values of all capacitor voltages across the DC-DC converters are equal, which confirm the correct operation of DC-DC converter and capacitor voltage balancer.

To demonstrate that the frequency of the power converter ports can be different the supply frequency at port-B is changed to $60Hz$. Figure 2.37 shows the simulated power converter topology.

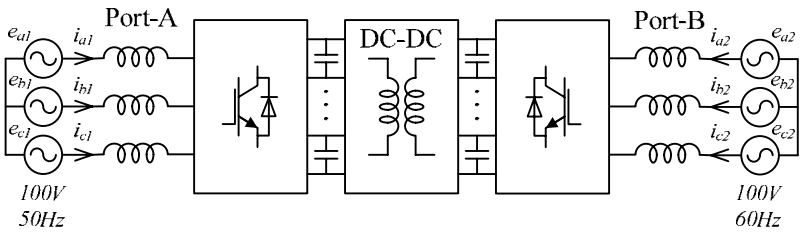
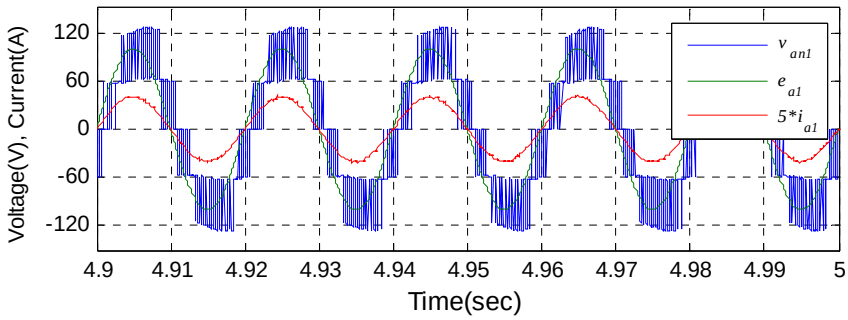
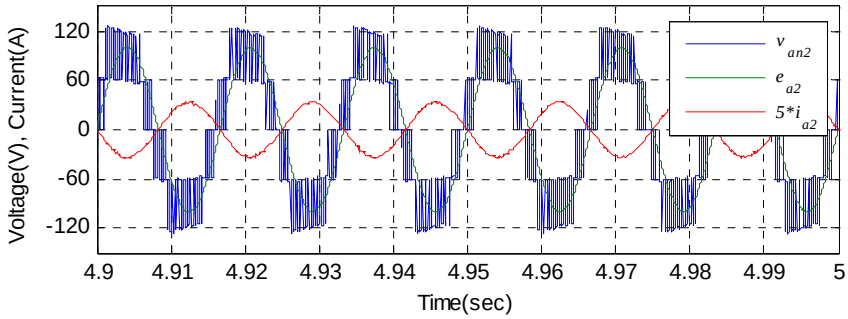


Figure 2.37: Complete power converter circuit diagram

Figure 2.38 shows the simulated waveforms for the current and voltage at ports A and B. The power flow is from port-A to port-B under unity power factor conditions.



(a) Supply voltage e_a , Converter voltage v_{an} , and line current i_a at phase-a, Port-A at $50Hz$.



(b) Supply voltage e_a , Converter voltage v_{an} , and line current i_a at phase-a, Port-B at $60Hz$.

Figure 2.38: Two-port converter waveforms.

Simulation results in figure 2.38 confirm the correct operation of power converter while its ports are connected three-phase supplies with different frequencies.

Figure 2.39 shows the capacitor voltages across the DC-DC converters.

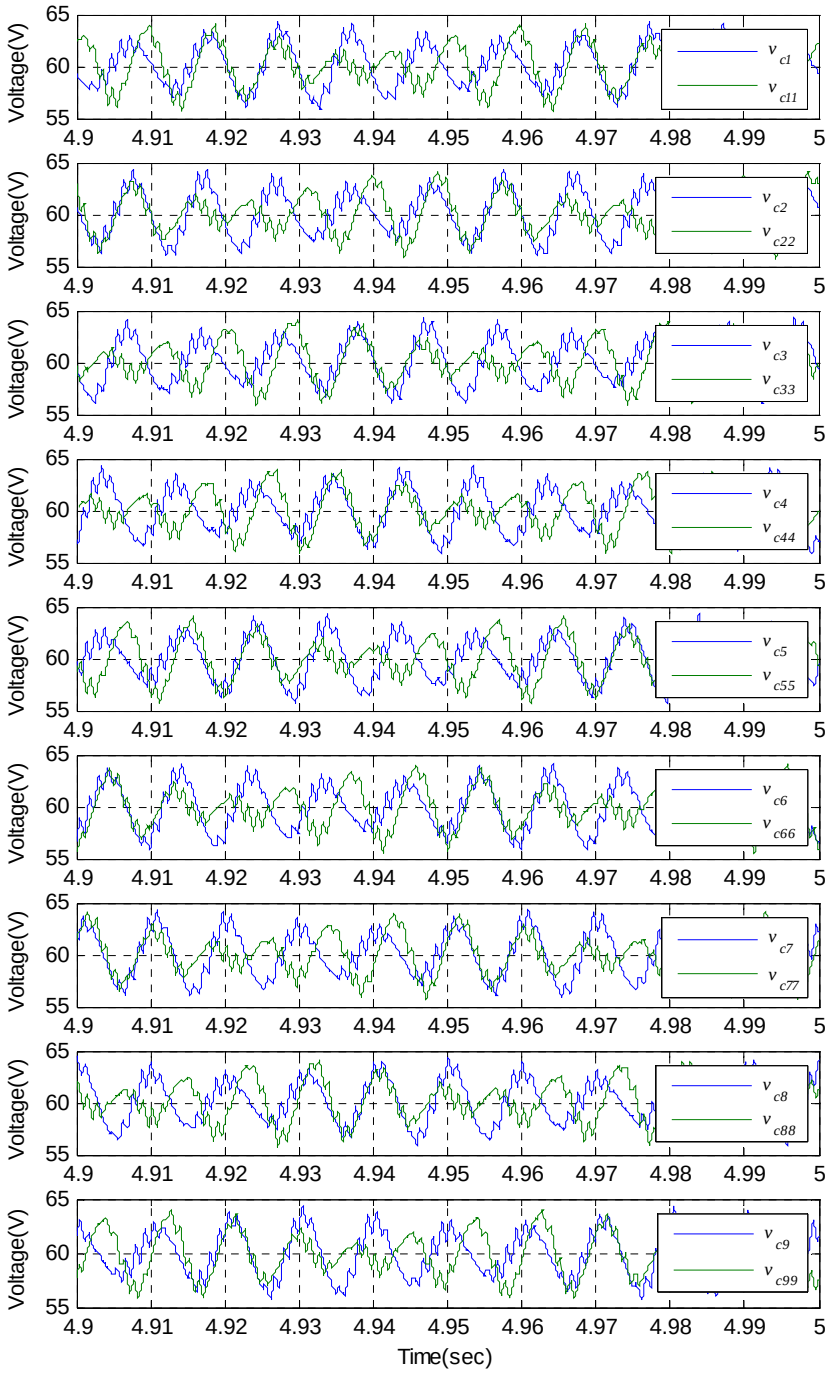


Figure 2.39: DC link voltages across DC-DC converters.

The capacitor voltages across each DC-DC converter have different ripple frequencies but the average value of all capacitor voltages are equal, which confirm the correct operation of DC-DC converter and capacitor voltage balancer.

2.9. Summary

In this chapter the design method for the control loops for a multi-cellular two-port power converter has been presented. The dq transformation has been used to decouple the system equations for the AC waveforms. Three control models have been presented and used to design the current control loop, voltage control loop and capacitor voltage balancer. Phase-Shifted-Cascaded PWM has been selected and implemented as the power converter modulation technique. A complete control diagram has been presented for ports A and B of the converter. The structure and basic theory of the DC-DC converter has been presented. Finally, simulation results have been presented to show the complete operation of the two-port power converter.

Chapter 3

Sliding Mode Observers

3.1 Introduction

This chapter presents a review of sliding mode observers. First a history of the invention of observers is presented. Then a background of the variable structure system is given. The structure of the traditional sliding mode observer and the sliding mode observer using an equivalent control method are described. Finally, simulation results for the sliding mode observer using the equivalent control method are presented and discussed. The Luenberger observer and traditional SMO aren't robust to uncertainty in system model or parameters. The "SMO using the equivalent control method" has robustness to system parameter uncertainty. Therefore "SMO using the equivalent control method" has been selected to be applied to power converter.

3.2 History of observer

The idea of using a dynamic system, called an observer, to estimate system state vectors was introduced by Luenberger in 1964 [26][27][28] and further developed by him later in 1966

[29]. In many control system designs it is assumed that the system state vectors are available by direct measurement, however this is not the case in many practical cases. Application of theories like state feedback controllers, which assume that the state vectors are known, is limited in these cases. An observer generates an estimate of the system state vectors. The observer uses information from the input and output variables of the original system to estimate the system states [29]. The estimation of the system state variables can be used instead of the real state variables in feedback loops without loss of system stability. Consider a dynamic system defined by:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx \end{cases} \tag{3.1}$$

Where $x \in \mathbb{R}^n, u \in \mathbb{R}^p, y \in \mathbb{R}^m$ and $A \in \mathbb{R}^{n\times n}, B \in \mathbb{R}^{n\times p}, C \in \mathbb{R}^{m\times n}$ are constant matrices. The mathematical model of the Luenberger observer will be [24]:

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + L(\hat{y} - y) + Bu \\ \hat{y} = C\hat{x} \end{cases} \tag{3.2}$$

Where $\hat{x}$ is the estimation of system state vector, $\hat{y}$ is the estimation of the system output and L is the observer gain matrix. Figure 3.1 shows the diagram of a system and associated Luenberger observer.

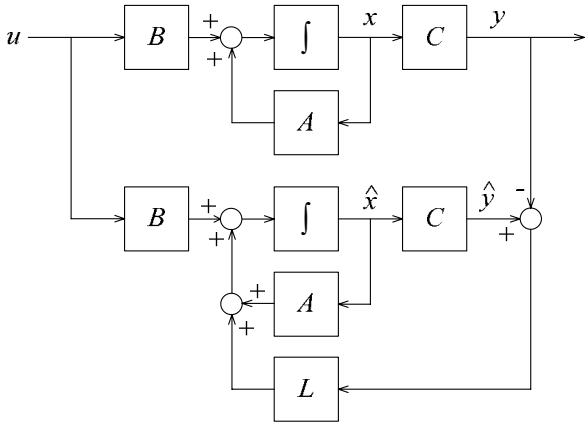


Figure 3.1: Luenberger observer diagram

Subtracting equation 3.2 from equation 3.1 will give the dynamics of the error vector e_x:

$$\begin{cases} \dot{e_x} = Ae_x + Le_y \\ e_y = Ce_x \end{cases} \tag{3.3}$$

$$e_x = \hat{x} - x, \qquad e_y = \hat{y} - y \tag{3.4}$$

By choosing the proper value for L, the eigenvalues of $(A + LC)$ can be placed in the left-hand half plane (LHP) to force the error vector e_x towards zero. As figure 3.1 shows, in order to construct the Luenberger observer one needs to accurately know the system parameters. Before designing the observer, it is necessary to check the observability of the system. The observability matrix of the system is defined as:

$$\mathcal{O} = \begin{bmatrix} C \\ CA \\ \vdots \\ CA^{n-1} \end{bmatrix} \tag{3.5}$$

The system described by equations 3.1 and 3.2 is observable if, and only, if the rank of the observability matrix is equal to n. This type of observer is only for linear systems with completely known parameters. Any modelling or measurement error leads to error in observation values and loss of observer action [30].

3.3 Variable structure systems

The theory of variable structure system (VSS) was first introduced in Soviet literature in early 1950's by Emelyanov and other researchers [31][32]. VSS theory is based on the using discontinuous feedback control [33][34]. This feedback control is achieved using high speed switching control action between two distinctively different system structures, which forces the trajectory of the system onto a manifold or sliding surface [35][32][36][37]. Having reached the intersection, the trajectory will remain on the manifold and slides on it. This mode of the system is called sliding mode [35][36]. The VSS theory can be used for the design of feedback control laws for uncertain systems. During sliding mode the variable structure controllers are robust to parameter uncertainty and also disturbance [34][38]. VSS control has four main advantages [39]:

- The manifold (switching surface) can be selected in a way that system is robust to disturbances and parameter changes during the sliding mode.

- During the sliding mode the system emulates a reduced order system and if the system has bounded nonlinearities, then under some conditions system behaves like linear system.
- Control algorithm is very simple, and can even be implemented by using a comparator and relay.
- By varying the switching surface the problem of tracking can be addressed.

Although VSS theory has robustness properties against parametric uncertainty and disturbances, classical variable structure control has several drawbacks that limit its practical applicability [40][41]. Variable structure control involves large control authority and control chattering. Chattering is a oscillation with finite frequency and amplitude about the sliding mode manifold [42] which can be harmful and undesirable in some practical applications. This chattering can lead to low control accuracy and high stress on mechanical parts.

There are two possible causes of chattering [36][42][43]. First is the neglected fast dynamics of fast actuators, servomechanisms, sensors and data processors which can be excited by the high switching frequencies and will produce non-decaying oscillations with finite amplitude and frequency. Second is the practical issue of switches that are not capable of switching with infinite frequency and hence will cause chattering affects. Some solutions to improve the chattering problem are suggested in [44][42][45][46][47] but these are limited in application.

3.4 Sliding mode observer

The theory of the sliding mode observer is based on the theory of variable structure systems [48][49]. Sliding mode observers can be applied to both linear and nonlinear systems. Several nonlinear sliding mode observers have been proposed by Misawa, Hedrick and Slotine [43][50][40] as well as Xiong and Saif [51]. Generally there are two methods of sliding mode observer implementation [52]. One method is based on equivalent control theory and the other is based on Lyapunov theory. Several sliding mode observers based on Lyapunov observer have been proposed by Walcott and Zak [53][54][55][56][39], Edwards and Spurgeon [57] as well as Zinober and Koshkouei [58].

Sliding mode observers using the equivalent control method have been published by Utkin and Drakunov [59][60], Hashimoto, Utkin, Xu, Suzuki and Harashima [61] and Haskara, Ozguner and Utkin [62][49]. Sliding mode observers using the equivalent control method are well established for linear systems and have good robustness against system disturbances.

The system studied in this thesis is linear so we are interested in sliding mode observers for linear system hence the main focus of this chapter is on the sliding mode observers based on the equivalent control method.

3.4.1 Traditional sliding mode observers

Early sliding mode observers were introduced by Utkin [49]. In this type of observer the original system is transformed into a canonical form. In the canonical form the output variable appears as a part of state vector. The observed values converge to real states asymptotically. The traditional sliding mode observer is applicable to linear systems. It has no robustness against system uncertainty. Consider a dynamical system defined by:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx \end{cases} \tag{3.6}$$

Where $x \in \mathbb{R}^n, u \in \mathbb{R}^p, y \in \mathbb{R}^m$ and $A \in \mathbb{R}^{n\times n}, B \in \mathbb{R}^{n\times p}, C \in \mathbb{R}^{m\times n}$ are constant matrices. This system can be transformed into the following canonical form:

$$\begin{bmatrix} \dot{y} \\ \dot{x_1} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} y \\ x_1 \end{bmatrix} + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} u \tag{3.7}$$

By a non-singular transformation:

$$\begin{bmatrix} y \\ x_1 \end{bmatrix} = Tx \tag{3.8}$$

T is a non-singular transformation matrix:

$$T = \begin{bmatrix} C \\ R_1 \end{bmatrix} \tag{3.9}$$

Where $R_1 \in \mathbb{R}^{(n-m)\times n}$ is an arbitrary matrix as long as T remains non-singular and $x_1 \in \mathbb{R}^{(n-m)}$ is equal to $R_1 x$. The corresponding sliding mode observer for equation 3.7 would be in the form given in equation 3.10 [47]:

$$\begin{bmatrix} \dot{\hat{y}} \\ \dot{\hat{x}}_1 \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} \hat{y} \\ \hat{x}_1 \end{bmatrix} + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} u + \begin{bmatrix} -1 \\ k \end{bmatrix} v \tag{3.10}$$

Where:

$$v = M.sgn(e_y) \tag{3.11}$$

Where e_y is the measurement error and sgn is sign function, as shown in figure 3.2.

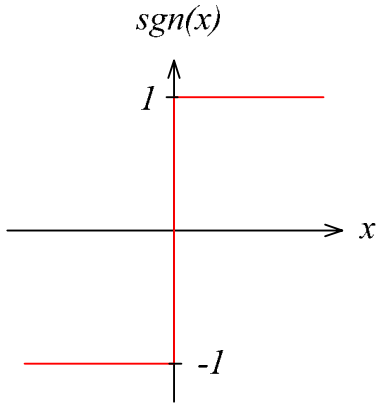


Figure 3.2: $sgn()$ function

The dynamic error is obtained by subtracting equation 3.7 from equation 3.10.

$$\begin{bmatrix} \dot{e_y} \\ \dot{e_{x1}} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} e_y \\ e_{x1} \end{bmatrix} + \begin{bmatrix} -1 \\ k \end{bmatrix} v \tag{3.12}$$

Where:

$$e_{x1} = \hat{x}_1 - x_1, \qquad e_y = \hat{y} - y \tag{3.13}$$

By appropriate choice of M, it is possible that e_y reaches on manifold $S(e_y = 0)$ and slides on this surface. The manifold S is shown in figure 3.3.

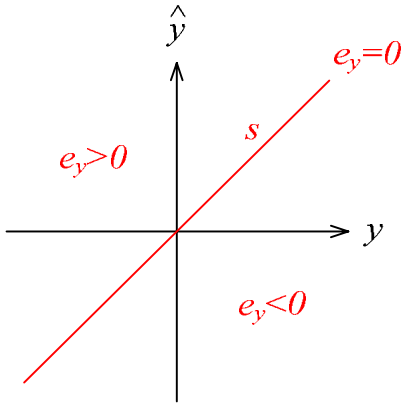


Figure 3.3: Manifold S

In order to force e_y to reach on manifold S and slide on the surface, e_y and $\dot{e_y}$ should have different signs [35].

$$e_y \, \dot{e_y} < 0 \tag{3.14}$$

But if the initial condition of e_y is far from manifold S then condition (3.14) cannot guarantee the reaching mode in a finite time. To make sure that the reaching mode finishes in a finite time the following condition is used [63]:

$$e_y \, \dot{e_y} < -\eta |e_y| \ , \qquad \eta > 0 \tag{3.15}$$

Combining equations (3.12) with equation (3.15) results in the following equations:

$$e_y \left(A_{11} e_y + A_{12} e_{x1} - M.sgn(e_y) \right) < -\eta |e_y| \tag{3.16}$$

Or

$$e_y > 0 : \quad \left(A_{11} e_y + A_{12} e_{x1} - M \right) < -\eta \tag{3.17}$$

$$e_y < 0 : \quad \left(A_{11} e_y + A_{12} e_{x1} - M \right) > +\eta \tag{3.18}$$

Combining equations 3.17 and 3.18 will result in equation 3.19.

$$\left| A_{11} e_y + A_{12} e_{x1} \right| + \eta < M \tag{3.19}$$

By choosing M to be large enough, the reaching mode will be achieved in a finite time and the sliding mode will be guaranteed. In the sliding mode e_y and $\dot{e_y}$ are forced to zero. By replacing e_y and $\dot{e_y}$ by zero in equation 3.12 the solution for equivalent value of discontinuous control input v can be derived:

$$A_{12}e_{x1} = v_{eq} \tag{3.20}$$

By replacing the v_{eq} in second line of equation 3.12, the dynamic of e_{x1} is derived as:

$$\dot{e_{x1}} = (A_{22} + kA_{12})e_{x1} \tag{3.21}$$

By choosing the appropriate value for k we can assign stable eigenvalues for $A_{22} + kA_{12}$ and control the speed of convergence of e_{x1} to zero.

3.4.2 Sliding mode observer using the equivalent control method

A sliding mode observer by using the equivalent control method is proposed by Utkin and Drakunov [59][60], Hashimoto, Utkin, Xu, Suzuki and Harashima [61] and Haskara, Ozguner and Utkin [49][62]. Consider a dynamical system defined by:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx \end{cases} \tag{3.22}$$

Where $x \in \mathbb{R}^n, u \in \mathbb{R}^p, y \in \mathbb{R}^m$ and $A \in \mathbb{R}^{n\times n}, B \in \mathbb{R}^{n\times p}, C \in \mathbb{R}^{m\times n}$ are constant matrices. This system can be transformed into the following canonical form:

$$\begin{cases} \dot{y} = A_{11}y + A_{12}x_1 + B_1u \\ \dot{x}_1 = A_{21}y + A_{22}\,x_1 + B_2u \end{cases} \tag{3.23}$$

Using a non-singular transformation $T \in \mathbb{R}^{n\times n}$:

$$T = \begin{bmatrix} C \\ R_1 \end{bmatrix} \tag{3.24}$$

Where $R_1 \in \mathbb{R}^{(n-m)\times n}$ is an arbitrary matrix as long as T remains non-singular.

$$Tx = \begin{bmatrix} y \\ x_1 \end{bmatrix},\ TAT^{-1} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix},\ TB = \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} \tag{3.25}$$

The rank of $A_{12} \in \mathbb{R}^{m\times(n-m)}$ is m_1, where $m_1 \leq m$, $m_1 \leq n-m$. There exist a matrix $D_1 \in \mathbb{R}^{m_1\times m}$ such that rank $\{D_1A_{12}\} = m_1$. At this stage a new variable $y_1 \in \mathbb{R}^{m_1}$ is defined and is combined with the second line of equation 3.23:

$$\begin{cases} \dot{x}_1 = A_{21}y + A_{22}x_1 + B_2u \\ y_1 = D_1A_{12}x_1 \end{cases} \tag{3.26}$$

This system can be transformed into the following canonical form:

$$\begin{cases} \dot{y}_1 = A_{31}y_1 + A_{32}x_2 + A_{33}y + B_3u \\ \dot{x}_2 = A_{41}y_1 + A_{42}x_2 + A_{43}y + B_4u \end{cases} \tag{3.27}$$

Using a non-singular transformation $T_1 \in \mathbb{R}^{(n-m)\times(n-m)}$:

$$T_1 = \begin{bmatrix} D_1A_{12} \\ R_2 \end{bmatrix} \tag{3.28}$$

Where $R_2 \in \mathbb{R}^{(n-m-m_1)\times(n-m)}$ is an arbitrary matrix as long as T_1 remains non-singular.

$$T_1x_1 = \begin{bmatrix} y_1 \\ x_2 \end{bmatrix},\ T_1A_{22}{T_1}^{-1} = \begin{bmatrix} A_{31} & A_{32} \\ A_{41} & A_{42} \end{bmatrix},\ T_1B_2 = \begin{bmatrix} B_3 \\ B_4 \end{bmatrix} \tag{3.29}$$

The rank of $A_{32} \in \mathbb{R}^{m_1\times(n-m-m_1)}$ is m_2. There exist a matrix $D_2 \in \mathbb{R}^{m_2\times m_1}$ such that rank $\{D_2A_{32}\} = m_2$.

At this stage a new variable $y_2 \in \mathbb{R}^{m_2}$ is defined and is combined with the second line of equation 3.27.

$$\begin{cases} \dot{x}_2 = A_{41}y_1 + A_{42}x_2 + A_{43}y + B_4u \\ y_2 = D_2A_{32}x_2 \end{cases} \tag{3.30}$$

This system can be transformed into the following canonical form:

$$\begin{cases}\dot{y}_2 = A_{51}y_2 + A_{52}x_3 + A_{53}y + A_{54}y_1 + B_5u \\ \dot{x}_3 = A_{61}y_2 + A_{62}x_3 + A_{63}y + A_{64}y_1 + B_6u\end{cases} \tag{3.31}$$

by a non-singular transformation $T_2 \in \mathbb{R}^{(n-m-m_1)\times(n-m-m_1)}$:

$$T_2 = \begin{bmatrix}D_2A_{32} \\ R_3\end{bmatrix} \tag{3.32}$$

Where $R_3 \in \mathbb{R}^{(n-m-m_1-m_2)\times(n-m-m_1)}$ is an arbitrary matrix as long as T_2 remains non-singular.

$$T_2x_2 = \begin{bmatrix}y_2 \\ x_3\end{bmatrix},\ \ T_2A_{42}{T_2}^{-1} = \begin{bmatrix}A_{51} & A_{52} \\ A_{61} & A_{62}\end{bmatrix},\ \ T_2B_4 = \begin{bmatrix}B_5 \\ B_6\end{bmatrix} \tag{3.33}$$

at step k the canonical form of system equations will be:

$$\begin{cases}\dot{y}_{k-1} = A_{2k-1,1}y_{k-1} + A_{2k-1,2}x_k + A_{2k-1,3}y + \cdots + A_{2k-1,k+1}y_{k-2} + B_{2k-1}u \\ \dot{x}_k = A_{2k,1}y_{k-1} + A_{2k,2}x_k + A_{2k,3}y + \cdots + A_{2k,k+1}y_{k-2} + B_{2k}u\end{cases} \tag{3.34}$$

Using a non-singular transformation $T_{k-1} \in \mathbb{R}^{(n-m-\sum_1^{k-2}m_i)\times(n-m-\sum_1^{k-2}m_i)}$:

$$T_{k-1} = \begin{bmatrix}D_{k-1}A_{2k-3,2} \\ R_k\end{bmatrix} \tag{3.35}$$

Where:

$$T_{k-1}x_{k-1} = \begin{bmatrix}y_{k-1} \\ x_k\end{bmatrix} \tag{3.36}$$

Where $R_k \in \mathbb{R}^{(n-m-\sum_1^{k-1}m_i)\times(n-m-\sum_1^{k-2}m_i)}$ is an arbitrary matrix as long as T_{k-1} remains non-singular. At each step the dimension of dimension of the new system decreases. This procedure will be repeated until step r where $n = m + \sum_{i=1}^{r} m_i$. At step r a new variable $y_r \in \mathbb{R}^{m_r}$ is defined and can be combined with an expression for $\dot{x}_r$ as follows:

$$\begin{cases} \dot{x}_r = A_{2r,1}y_{r-1} + A_{2r,2}x_r + A_{2r,3}y + \cdots + A_{2r,r+1}y_{r-2} + B_{2r}u \\ y_r = D_r A_{2r-1,2}x_r \end{cases} \tag{3.37}$$

D_r is chosen in such a way that the rank of $D_r A_{2r-1,2}$ is equal to m_r. Also y_r and x_r are related by a non-singular transformation $T_r \in \mathbb{R}^{m_r \times m_r}$:

$$T_r = \left[D_r A_{2r-1,2}\right] \tag{3.38}$$

The complete set of system equations in canonical form will then be defined by:

$$\begin{cases} \dot{y} = A_{11}y + A_{12}x_1 + B_1u \\ \dot{y}_1 = A_{31}y_1 + A_{32}x_2 + A_{33}y + B_3u \\ \dot{y}_2 = A_{51}y_2 + A_{52}x_3 + A_{53}y + A_{54}y_1 + B_5u \\ \vdots \\ \dot{y}_{r-1} = A_{2r-1,1}y_{r-1} + A_{2r-1,2}x_r + A_{2r-1,3}y + \cdots + A_{2r-1,r+1}y_{r-2} + B_{2r-1}u \\ \dot{y}_r = A_{2r+1,1}y_r + A_{2r+1,3}y + \cdots + A_{2r+1,r+2}y_{r-1} + B_{2r+1}u \end{cases} \tag{3.39}$$

The complete set of observer equations for above system equations set will be:

$$\begin{cases} \dot{\hat{y}} = A_{11}\hat{y} + A_{12}\hat{x}_1 + B_1u - L_1 sgn(\hat{y} - y) \\ \dot{\hat{y}}_1 = A_{31}\hat{y}_1 + A_{32}\hat{x}_2 + A_{33}\hat{y} + B_3u - L_2 sgn(\hat{y}_1 - y_1) \\ \dot{\hat{y}}_2 = A_{51}\hat{y}_2 + A_{52}\hat{x}_3 + A_{53}\hat{y} + A_{54}\hat{y}_1 + B_5u - L_3 sgn(\hat{y}_2 - y_2) \\ \vdots \\ \dot{\hat{y}}_{r-1} = A_{2r-1,1}\hat{y}_{r-1} + A_{2r-1,2}\hat{x}_r + A_{2r-1,3}\hat{y} + \cdots + A_{2r-1,r+1}\hat{y}_{r-2} + B_{2r-1}u \\ \qquad -L_r sgn(\hat{y}_{r-1} - y_{r-1}) \\ \dot{\hat{y}}_r = A_{2r+1,1}\hat{y}_r + A_{2r+1,3}\hat{y} + \cdots + A_{2r+1,r+2}\hat{y}_{r-1} + B_{2r+1}u - L_{r+1} sgn(\hat{y}_r - y_r) \end{cases} \tag{3.40}$$

Where $L_{k+1} \in \mathbb{R}^{m_k \times m_k}$ is a diagonal matrix for the kth step and by choosing the elements to be large enough the sliding mode will take place at kth step on manifold; $S_k(e_y = 0 \cap e_{y_1} = 0 \cap \ldots \cap e_{y_k} = 0)$.

Where e_{y_k} is the error between observed value and system output values and can be defined as:

$$e_{y_k} = \hat{y}_k - y_k \tag{3.41}$$

By subtracting the equation set 3.39 from equation set 3.40 the errors can be defined as:

$$\begin{cases} \dot{e}_y = A_{11}e_y + A_{12}e_{x_1} - L_1 sgn(e_y) \\ \dot{e}_{y_1} = A_{31}e_{y_1} + A_{32}e_{x_2} + A_{33}e_y - L_2 sgn(e_{y_1}) \\ \dot{e}_{y_2} = A_{51}e_{y_2} + A_{52}e_{x_3} + A_{53}e_y + A_{54}e_{y_1} - L_3.sgn(e_{y_2}) \\ \vdots \\ \dot{e}_{y_{r-1}} = A_{2r-1,1}e_{y_{r-1}} + A_{2r-1,2}e_{x_r} + A_{2r-1,3}e_y + \cdots + A_{2r-1,r+1}e_{y_{r-2}} \\ \quad -L_r sgn(e_{y_{r-1}}) \\ \dot{e}_{y_r} = A_{2r+1,1}\hat{y}_r + A_{2r+1,3}\hat{y} + \cdots + A_{2r+1,r+2}\hat{y}_{r-1} - L_{r+1} sgn(e_{y_r}) \end{cases} \tag{3.42}$$

In sliding mode, the discontinuous control input $L_{k+1}sgn(e_{y_k})$ forces the $\dot{e}_{y_k}$and e_{y_k} towards zero. In order to find the equivalent value of the discontinuous control input $L_{k+1}sgn(e_{y_k})$, $\dot{e}_{y_k}$and $e_{y_k}$are replaced by zero in equation 3.42, therefore:

$$\left[L_{k+1}sgn(e_{y_k})\right]_{eq} = A_{2k+1,2}e_{x_{k+1}} \tag{3.43}$$

The equivalent value by physical meaning is the average value of the discontinuous control function [49][59]. A low pass filter can be used to realize the equivalent value of the discontinues control input $L_{k+1}sgn(e_{y_k})$:

$$\tau_{k+1}\dot{z}_{k+1} + z_{k+1} = L_{k+1}sgn(e_{y_k}) \tag{3.44}$$

Where z_{k+1} is the output of the low pass filter and can be used as the equivalent value of discontinuous control signal. The filter time constant τ_{k+1} should be very small in comparison to other variables in order to get good results. Therefore:

$$z_{k+1} = \left[L_{k+1}sgn(e_{y_k})\right]_{eq} \tag{3.45}$$

Based on the definition of the new variables $y_k = D_r A_{2k-1,2} x_k$ at each step:

$$e_{y_k} = D_r A_{2k-1,2} e_{x_k} \tag{3.46}$$

Combining equations 3.46 and 3.43 will give:

$$e_{y_{k+1}} = D_{k+1}\left[L_{k+1} sgn\left(e_{y_k}\right)\right]_{eq} \tag{3.47}$$

And combining equation 3.47 with 3.45 will result in:

$$e_{y_k} = D_k z_k \tag{3.48}$$

The final form of the observer equations can then be written by using the new expression for the error signal in equation 3.48:

$$\begin{cases} \dot{\hat{y}} = A_{11}\hat{y} + A_{12}\hat{x}_1 + B_1 u - L_1 sgn\left(e_y\right) \\ \dot{\hat{y}}_1 = A_{31}\hat{y}_1 + A_{32}\hat{x}_2 + A_{33}\hat{y} + B_3 u - L_2 sgn(D_1 z_1) \\ \dot{\hat{y}}_2 = A_{51}\hat{y}_2 + A_{52}\hat{x}_3 + A_{53}\hat{y} + A_{54}\hat{y}_1 + B_5 u - L_3 sgn(D_2 z_2) \\ \vdots \\ \dot{\hat{y}}_{r-1} = A_{2r-1,1}\hat{y}_{r-1} + A_{2r-1,2}\hat{x}_r + A_{2r-1,3}\hat{y} + \cdots + A_{2r-1,r+1}\hat{y}_{r-2} + B_{2r-1}u \\ \qquad -L_r sgn(D_{r-1} z_{r-1}) \\ \dot{\hat{y}}_r = A_{2r+1,1}\hat{y}_r + A_{2r+1,3}\hat{y} + \cdots + A_{2r+1,r+2}\hat{y}_{r-1} + B_{2r+1}u - L_{r+1} sgn(D_r z_r) \end{cases} \tag{3.49}$$

Once all the observed values for $\hat{y}_k$ are known, by inverse transformation, the system real state vector can be constructed. From the observer equations set 3.49 the $\hat{y}_r, \hat{y}_{r-1}, \dots, \hat{y}$ are known. Then the $\hat{x}_r, \hat{x}_{r-1}, \dots, \hat{x}$ can be calculated by following equations:

$$\hat{x}_r = {T_r}^{-1}\hat{y}_r \tag{3.50}$$

According to equation 3.36 the remaining state vectors can be calculated as follow:

$$\hat{x}_{r-1} = {T_{r-1}}^{-1}\begin{bmatrix}\hat{y}_{r-1}\\ {T_r}^{-1}\hat{y}_r\end{bmatrix} \tag{3.51}$$

$$\hat{x}_{r-2} = {T_{r-2}}^{-1}\begin{bmatrix}\hat{y}_{r-2}\\ {T_{r-1}}^{-1}\begin{bmatrix}\hat{y}_{r-1}\\ {T_r}^{-1}\hat{y}_r\end{bmatrix}\end{bmatrix} \tag{3.52}$$

$$\hat{x}_{r-3} = {T_{r-3}}^{-1}\begin{bmatrix}\hat{y}_{r-3}\\ {T_{r-2}}^{-1}\begin{bmatrix}\hat{y}_{r-2}\\ {T_{r-1}}^{-1}\begin{bmatrix}\hat{y}_{r-1}\\ {T_r}^{-1}\hat{y}_r\end{bmatrix}\end{bmatrix}\end{bmatrix} \tag{3.53}$$

$$\vdots$$

$$\hat{x} = T^{-1}\begin{bmatrix}\hat{y}\\ \vdots\\ {T_1}^{-1} & \begin{bmatrix}\ldots {T_{r-2}}^{-1}\begin{bmatrix}\hat{y}_{r-2}\\ {T_{r-1}}^{-1}\begin{bmatrix}\hat{y}_{r-1}\\ {T_r}^{-1}\hat{y}_r\end{bmatrix}\end{bmatrix}\end{bmatrix}\end{bmatrix} \tag{3.54}$$

3.5 Observer robustness against system uncertainty

In this section the robustness of the proposed observer against system uncertainty is tested. Consider a second-order linear equation in canonical form presented by equation 3.55, which contains an unknown function $f(t)$ in the second line.

$$\begin{cases}\dot{y} = a_1 y + b_1 y_1 + c_1 u_1\\ \dot{y}_1 = a_2 y + b_2 y_1 + c_2 u_2 + f(t)\end{cases} \tag{3.55}$$

Where y is the system output and y_1 is the system state to be observed. The function $f(t)$ can be caused by the uncertainty in the system model or parameters. The corresponding observer equation is:

$$\begin{cases}\dot{\hat{y}} = a_1\hat{y} + b_1\hat{y}_1 + c_1 u_1 - L_1 sgn(\hat{y} - y)\\ \dot{\hat{y}}_1 = a_2\hat{y} + b_2\hat{y}_1 + c_2 u_2 - L_2 sgn(b_1^{-1} z),\ \ z = (L_1 sgn(\hat{y} - y))/(1 + s\tau)\end{cases} \tag{3.56}$$

The dynamic of the system error can be described by:

$$\begin{cases} \dot{e}_y = a_1 e_y + b_1 e_{y_1} - L_1 sgn(e_y) \\ \dot{e}_{y_1} = a_2 e_y + b_2 e_{y_1} - f(t) - L_2 sgn(b_1^{-1} z) \end{cases} \quad (3.57)$$

In sliding mode the discontinuous control $L_1 sgn(e_y)$ will force $\dot{e}_y$ and e_y to zero. The equivalent value of the discontinuous control $L_1 sgn(e_y)$ can be calculated:

$$(\dot{e}_y = e_y = 0) \Rightarrow [L_1 sgn(e_y)]_{eq} = z = b_1 e_{y_1} \quad (3.58)$$

Substituting equation 3.58 in the second line of equation 3.57 results:

$$\dot{e}_{y_1} = a_2 e_y + b_2 e_{y_1} - f(t) - L_2 sgn(e_{y_1}) \quad (3.59)$$

The discontinuous control $L_2 sgn(e_{y_1})$ will force $\dot{e}_{y_1}$ and e_{y_1} to zero. The equivalent value of the discontinuous control $L_1 sgn(e_y)$ can be calculated:

$$(\dot{e}_{y_1} = e_{y_1} = 0) \Rightarrow \left[L_2 sgn(e_{y_1})\right]_{eq} = -f(t) \quad (3.60)$$

Therefore the proposed observer has robustness against uncertain functions in the second line of system equation 3.55. In order to check the proposed observer robustness against uncertain terms in the first line of the system equation, consider equation 3.61.

$$\begin{cases} \dot{y} = a_1 y + b_1 y_1 + c_1 u_1 + g(t) \\ \dot{y}_1 = a_2 y + b_2 y_1 + c_2 u_2 \end{cases} \quad (3.61)$$

The function $g(t)$ can be caused by the uncertainty in the system model or parameters. The corresponding observer equation is presented by 3.56. The dynamic of the system error can be described by:

$$\begin{cases} \dot{e}_y = a_1 e_y + b_1 e_{y_1} - g(t) - L_1 sgn(e_y) \\ \dot{e}_{y_1} = a_2 e_y + b_2 e_{y_1} - L_2 sgn(b_1^{-1} z) \end{cases} \quad (3.62)$$

In sliding mode the discontinuous control $L_1 sgn(e_y)$ will force $\dot{e}_y$ and e_y to zero. The equivalent value of the discontinuous control $L_1 sgn(e_y)$ can be calculated:

$$\left(\dot{e}_y = e_y = 0\right) \Rightarrow \left[L_1 sgn(e_y)\right]_{eq} = z = b_1 e_{y_1} - g(t) \tag{3.63}$$

Substituting equation 3.63 in the second line of equation 3.62 results:

$$\dot{e}_{y_1} = a_2 e_y + b_2 e_{y_1} - L_2 sgn\left(e_{y_1} - b_1^{-1} g(t)\right) \tag{3.64}$$

The discontinuous control $L_2 sgn\left(e_{y_1} - b_1^{-1} g(t)\right)$ cannot force $\dot{e}_{y_1}$ and e_{y_1} to zero. Therefore the proposed observer has no robustness to uncertain terms in the first line of the system equations.

3.6 Simulation results

The 'sliding mode observer using the equivalent control method' can be used to observe the states of a second order linear circuit shown in figure 3.4.

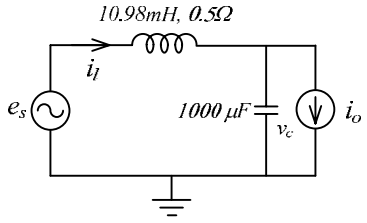


Figure 3.4: Second order linear circuit.

The state space equation of the circuit is:

$$\begin{cases} \dot{x} = \begin{bmatrix} -45.5 & -91 \\ 1000 & 0 \end{bmatrix} x + \begin{bmatrix} 0 & 91 \\ -1000 & 0 \end{bmatrix} u \\ y = [1 \quad 0] x \end{cases} \tag{3.65}$$

Where:

$$x = \begin{bmatrix} i_l \\ v_c \end{bmatrix}, \quad u = \begin{bmatrix} i_o \\ e_s \end{bmatrix} \tag{3.66}$$

The observability matrix can be defined as:

$$\mathcal{O} = \begin{bmatrix} C \\ CA \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -45.5 & -91 \end{bmatrix} \tag{3.67}$$

This observability matrix is full rank and system is therefore observable. In order to write the observer equations using equivalent control method, equation 3.55 should be transformed into the following canonical form where y and y_1 are scalars.

$$\begin{cases} \dot{y} = -45.5y - 91y_1 + 91u_2 \\ \dot{y}_1 = 1000y - 1000u_1 \end{cases} \tag{3.68}$$

Using a non-singular transformation $T \in \mathbb{R}^{2\times 2}$:

$$T = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{3.69}$$

Where

$$\hat{x} = \begin{bmatrix} \hat{y} \\ \hat{y}_1 \end{bmatrix} \tag{3.70}$$

The observer equations for the system described in equation 3.68 can be defined as:

$$\begin{cases} \dot{\hat{y}} = -45.5\hat{y} - 91\hat{y}_1 + 91u_2 - L_1 sgn(e_y) \\ \dot{\hat{y}}_1 = 1000\hat{y} - 1000u_1 - L_2 sgn\left(\frac{z_1}{-91}\right), \quad z_1 = \frac{L_1 sgn(e_y)}{1 + 0.0002s} \end{cases} \tag{3.71}$$

By choosing $L_1 = L_2 = 5000$, the sliding mode will be guaranteed. The time-constant of the low-pass filter is set to 0.0002s to have precise results. Figure 3.5 shows a simulation results for the observer designed for the second order linear circuit. In figure 3.5(a) observed value of line current i_l or $\hat{y}$ and line current i_l or y are presented. The observed value of capacitor voltage v_c or $\hat{y}_1$ and capacitor voltage v_c or y_1 are presented in figure 3.5(b). The chattering effect can be seen on $\hat{y}_1$ waveform. In figure 3.5(c) the discontinuous signal $L_1 sgn(e_y)$ and

its equivalent value z_1 is shown. In figure 3.5(d) the discontinuous signal $L_2 sgn\left(\frac{z_1}{-91}\right)$ is presented.

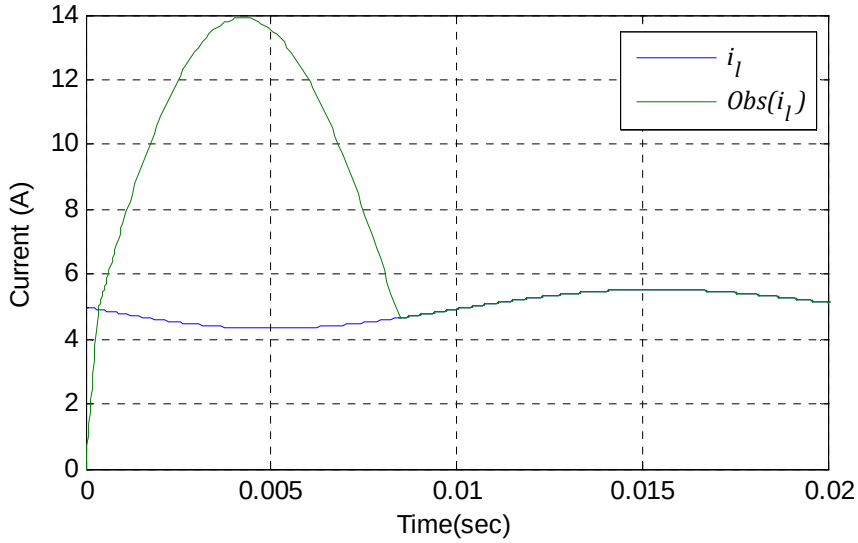


Figure 3.5 (a) $\hat{y}$ and y

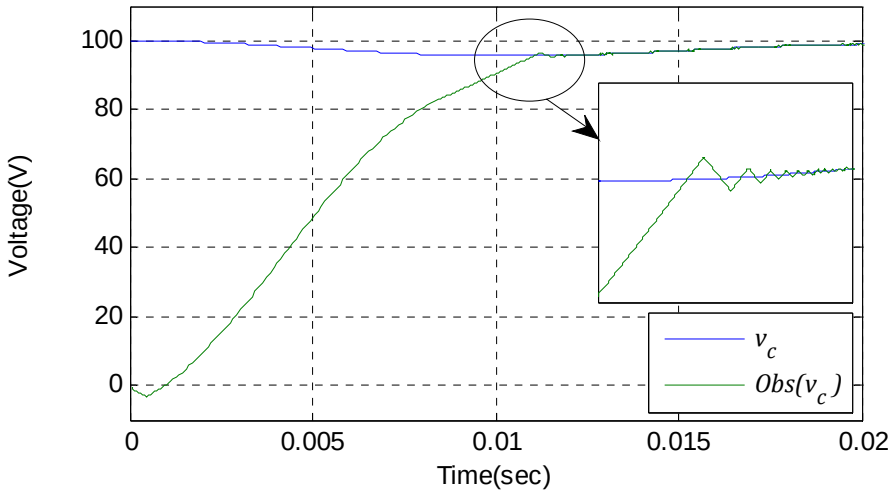
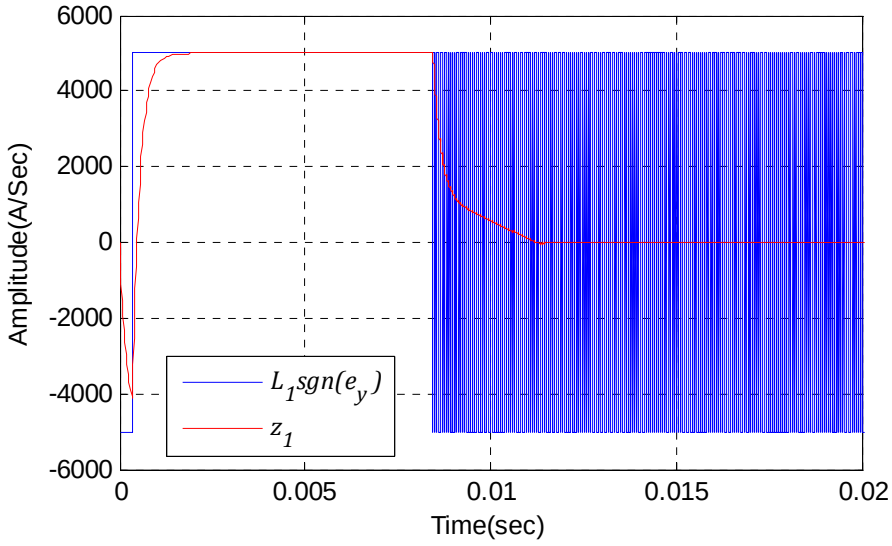
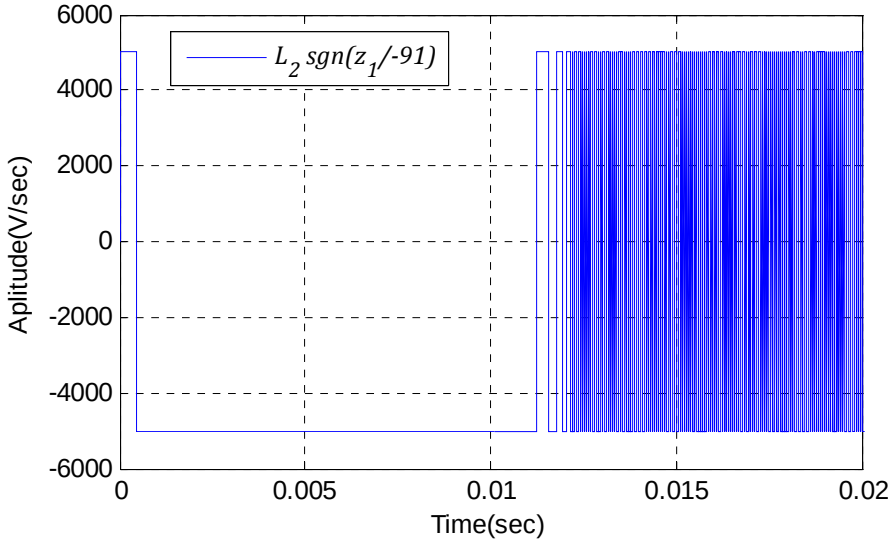


Figure 3.5 (b) $\hat{y}_1$ and y_1, chattering can be seen on $\hat{y}_1$ waveform.

The reaching time for the observed value of the inductor current is 8.45 ms and for the observed value of capacitor voltage is 11.1 ms. After observed value of the inductor current enters to sliding mode, the second-order system simplifies to a first-order system.



(c) $L_1 sgn(e_y)$ and z_1



(d) $L_2 sgn\left(\frac{z_1}{-91}\right)$

Figure 3.5: simulation results for Sliding mode observer using equivalent control method with sgn function.

The high frequency oscillation generated by $sgn()$ function is shown in figures 3.5(c) and 3.5 (d). The waveform z_1 is the equivalent value of the $L_1 sgn(e_y)$. A low-pass filter is used to realize the equivalent value of $L_1 sgn(e_y)$.

3.6.1 Observer using sat function

Chattering is undesirable in practical application because of the high control activity and other associated problems. Unlike the sliding mode control, chattering in sliding mode observers is only linked to the numerical implementation [40]. The problem of chattering can be solved by using smooth control instead of on-off control. To achieve this goal a piecewise linear approximation of sgn can be used, as shown in figure (3.6).

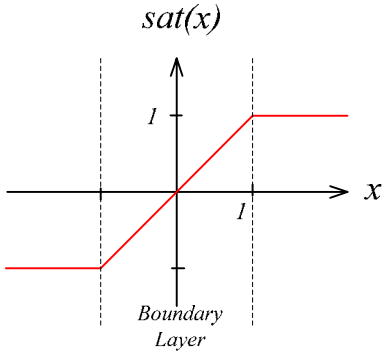


Figure 3.6: sat function

In order to avoid the high frequency switching functions in sliding mode the sign function, sgn, can be replaced by a saturation function, sat. By using the sat function instead of the sgn function there will be two operating region for observer, these are the inside of the boundary layer $(-1 < x < 1)$ where $sat(x) = x$ and the outside of the boundary layer $(x > 1 \; and \; x < -1)$ where $sat(x) = sgn(x)$. The observer given in equation 3.71 with the sat function becomes:

$$\begin{cases} \dot{\hat{y}} = -45.5\hat{y} - 91\hat{y}_1 + 91u_2 - 5000sat(e_y) \\ \dot{\hat{y}}_1 = 1000\hat{y} - 1000u_1 - 5000sat\left(\frac{z_1}{-91}\right) \end{cases} \tag{3.72}$$

Since $5000sat(e_y)$ is a 'smooth' function, then the output of low pass filter is the same as its input which means there is no need to implement the low-pass filter. Therefore z_1 can be replaced by $5000sat(e_y)$.

$$z_1 \approx 5000sat(e_y) \tag{3.73}$$

The final observer equation using sat function can be then written as:

$$\begin{cases} \dot{\hat{y}} = -45.5\hat{y} - 91\hat{y}_1 + 91u_2 - 5000sat(e_y) \\ \dot{\hat{y}}_1 = 1000\hat{y} - 1000u_1 - 5000sat\left(\frac{5000}{-91}sat(e_y)\right) \end{cases} \quad (3.74)$$

The dynamic error signal is:

$$\begin{cases} \dot{e}_y = -45.5e_y - 91e_{y_1} - 5000sat(e_y) \\ \dot{e}_{y_1} = 1000e_y - 5000sat\left(\frac{5000}{-91}sat(e_y)\right) \end{cases} \quad (3.75)$$

According to figure 3.6 outside of boundary layer, ($x < -1$ and $x > +1$) the $sat(x)$ and $sgn(x)$ are same. Inside the boundary layer ($-1 < x < +1$) the $sat(x)$ function is:

$$sat(x) = x \quad (3.76)$$

By using equation 3.76, equation 3.75 simplifies to:

$$\begin{cases} \dot{e}_y = -5045.5e_y - 91e_{y_1} \\ \dot{e}_{y_1} = +275725e_y \end{cases} \quad (3.77)$$

The eigenvalues of the system in equation 3.77 are $(-2523 \pm 4327i)$ which have large negative real parts, guarantying the fast convergence of e_y and e_{y_1} to zero inside the boundary layer. Figure 3.7 shows the simulation results for this revised observer. In figure 3.7(a) observed value of line current i_l or $\hat{y}$ and line current i_l or y are presented. The observed value of capacitor voltage v_c or $\hat{y}_1$ and capacitor voltage v_c or y_1 are presented in figure 3.7(b). As it can be seen, signal $\hat{y}_1$ reaches to y_1 smoothly and there is no chattering. In figure 3.7(c) the signal $L_1 sat(e_y)$ is shown and the signal $L_2 sat\left(\frac{L_1}{-91}sat(e_y)\right)$ is presented in figure 3.7(d).

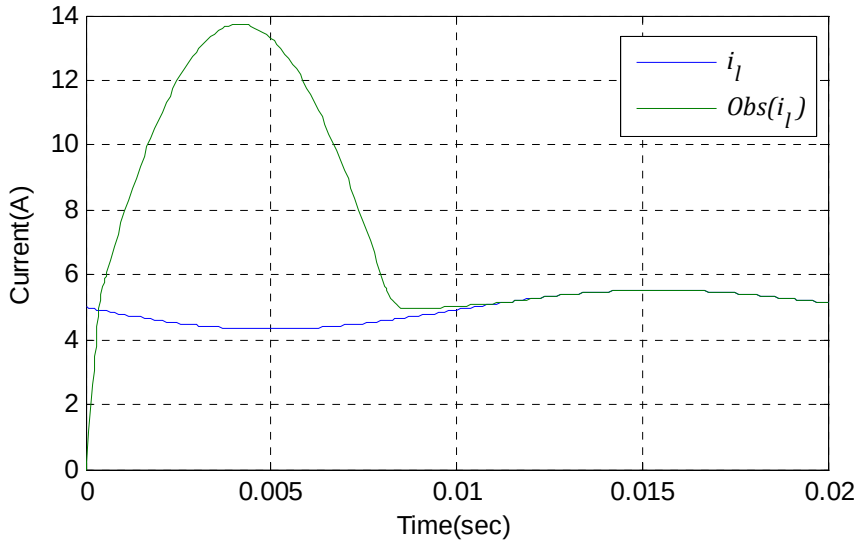


Figure 3.7 (a) $\hat{y}$ and y

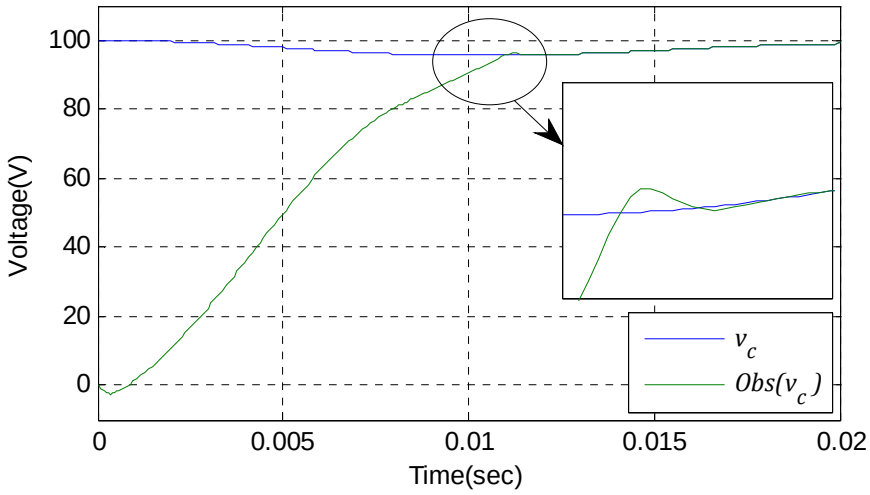
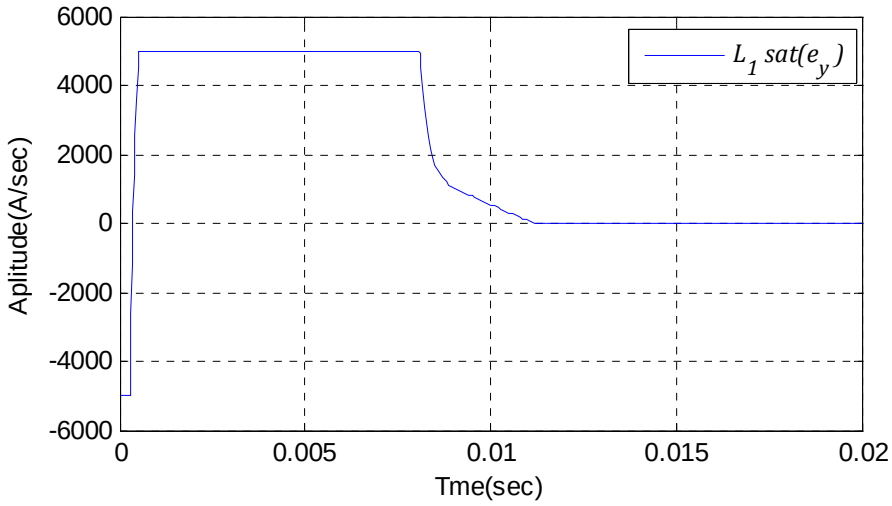
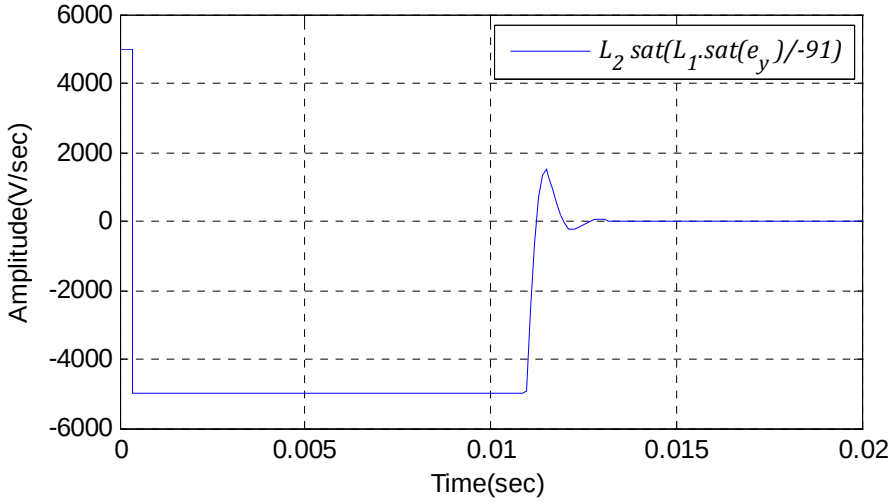


Figure 3.7 (b) $\hat{y}_1$ and y_1

According to simulation results in figure 3.7, there is no chattering or high-frequency oscillation in waveforms. The observed values of inductor current and capacitor voltage approaches to the real values smoothly.



(c) $L_1 sat(e_y)$



(d) $L_2 sat\left(\frac{L_1}{-91} sat(e_y)\right)$

Figure 3.7: simulation results for Sliding mode observer using equivalent control method with sat function.

The waveform of $L_1 sat(e_y)$ in figure 3.7(c) is quite similar to the waveform of z_1 in figure 3.5 (c). This confirms that using a $sat()$ function in observer equation is equivalent of using a $sgn()$ function and a low-pass filter. In this example the simulation results confirm that using a $sat()$ function instead of $sgn()$ function eliminates chattering and high-frequency oscillations.

3.6.2 Observer for the systems with uncertain terms

In this section the robustness of the proposed observer against uncertainty in system model or parameters is tested. Consider the system equation presented by equation 3.78:

$$\begin{cases} \dot{y} = -45.5y - 91y_1 + 91u_2 \\ \dot{y}_1 = 1000y - 1000u_1 + f(t) \end{cases} \tag{3.78}$$

The corresponding observer equation is presented in equation 3.71. The simulation results are presented in figure 3.8.

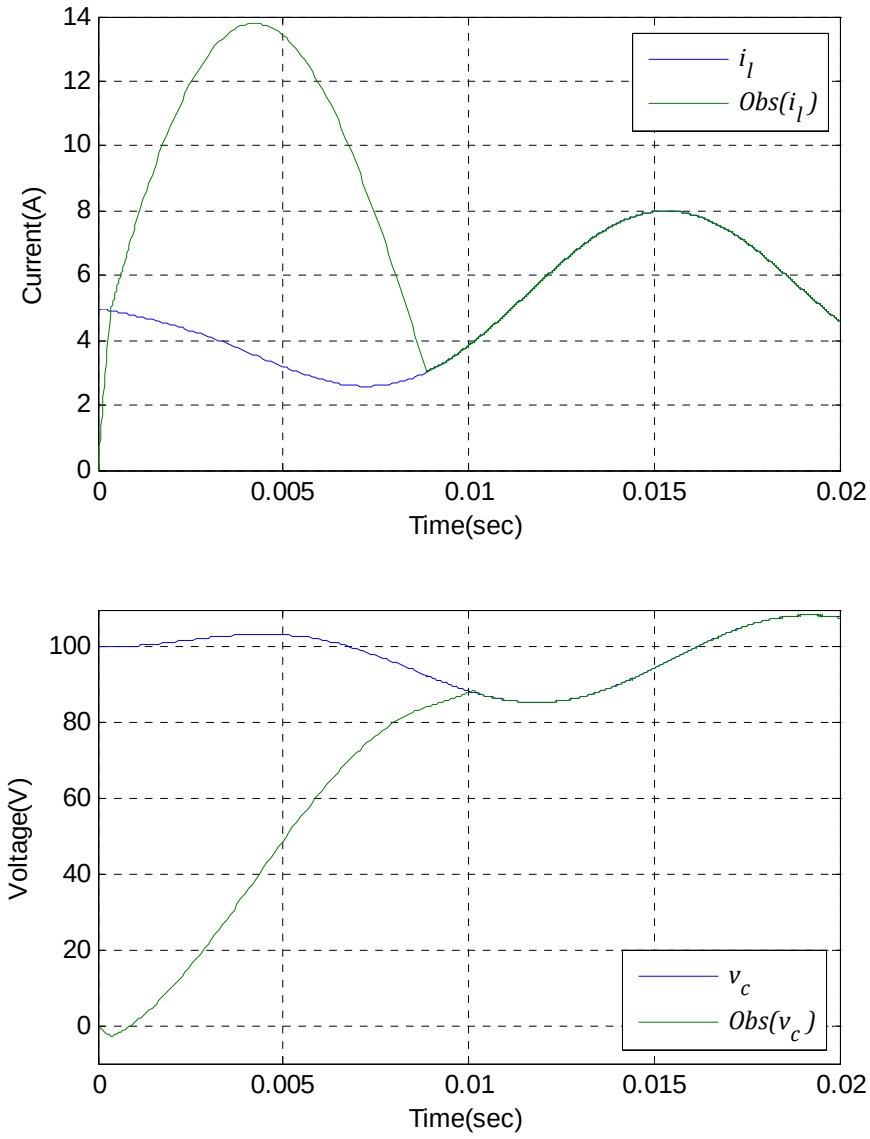
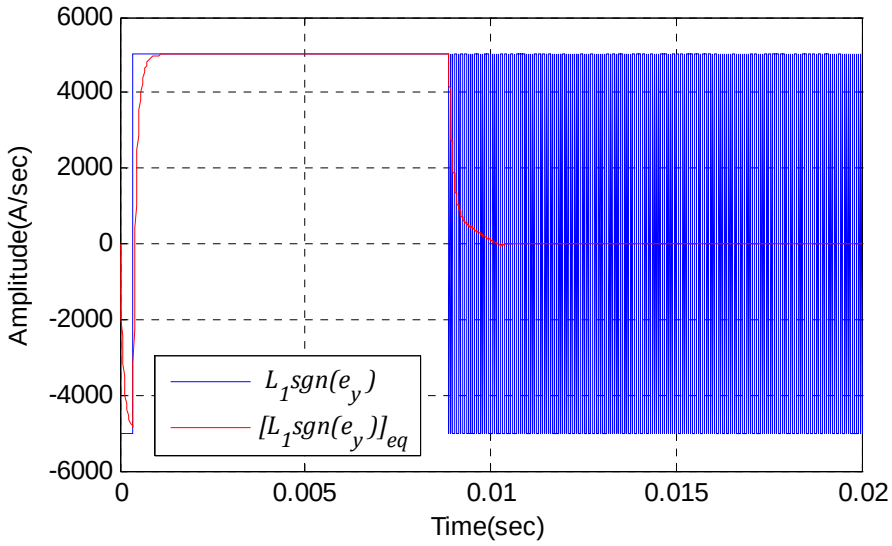
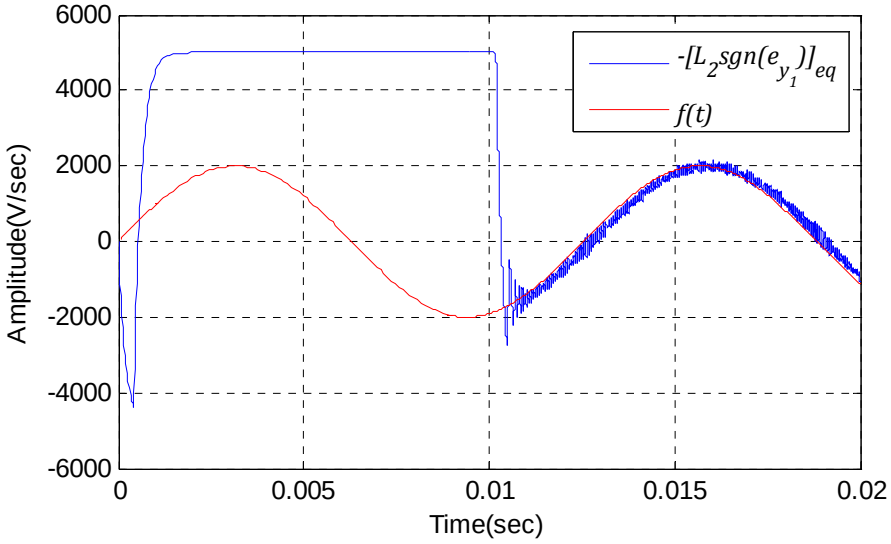


Figure 3.8 (a) $\hat{y}$ and , (b) $\hat{y}_1$ and y_1

In figure 3.8(a) observed value of line current i_l or $\hat{y}$ and line current i_l or y are presented. The observed value of capacitor voltage v_c or $\hat{y}_1$ and capacitor voltage v_c or y_1 are presented in figure 3.8(b). In figure 3.8(c) the discontinuous signal $L_1 sgn(e_y)$ and its equivalent value is shown.



(c) $L_1 sgn(e_y)$ and $\left(L_1 sgn(e_y)\right)_{eq}$



(d) $f(t)$ and $\left(-\left[L_2 sgn(e_{y1})\right]_{eq}\right)$

Figure 3.8: simulation results for Sliding mode observer using equivalent control method for a system with an uncertain term $f(t)$.

In figure 3.8(d) the unknown function $f(t)$ and an estimation of $f(t)$, $\left(-\left[L_2 sgn\left(e_{y1}\right)\right]_{eq}\right)$, is presented. The simulation results confirm the robustness of proposed observer against uncertainties in the form of equation 3.78. In This example, the unknown function $f(t)$ can be caused by variation in the capacitance value or measurement error in the current i_o. Therefore the proposed observer is robust against uncertainty in capacitance value and current i_o.

3.7 Summary

In this chapter the theory of the sliding mode observers based on the equivalent control method has been studied. In order to implement the observer, system equations are transformed to a canonical form. The sliding conditions have been presented. In order to avoid high frequency discontinuous signals a boundary layer sat function is used instead of sign function. Finally simulation results for an example second order linear system using MATLAB are presented to show the operation of the observer.

Chapter 4

Sliding Mode Observer Implementation

4.1 Introduction

This chapter presents the implementation of the observer for the DC-link voltages of a two-port cascaded H-bridge (CHB) multilevel converter. The sliding mode observer (SMO) using the equivalent control method has been chosen as observation method. A switching model of a single H-bridge converter has been used to design the SMO. First the SMO design is described and the application to a single H-bridge converter is considered. The application of the observer to the CHB multilevel converter is then discussed. The SMO design procedure for a back-to-back topology is also explained. The effect of the DC-DC converter in the back-to-back topology on SMO implementation is examined. Finally the SMO design and application for a two-port power converter is described. Simulation results for SMO are presented in each section of the chapter.

4.2 SMO design for a single H-bridge converter

The H-bridge converter is the basic building block of the complete two-port power converter. Therefore as a first step, the SMO will be designed and implemented on a single H-bridge converter. The SMO using the equivalent control method has studied in detail in chapter 3. The first step in the design of SMO is to build a mathematical model of the system. In a system including an H-bridge converter the system mathematical model changes with the H-bridge switching action. The mathematical model must take into account the switching state of the H-bridge. The switching states S for the H-bridge converter are presented in table 4.1, based on the H-bridge converter topology shown in figure 4.1.

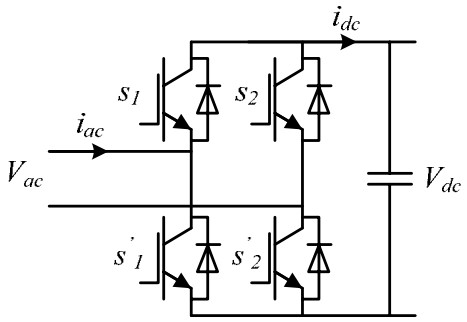


Figure 4.1: The H-Bridge converter circuit

S	
1	s_1 is on and s_2 is off
0	s_1 is on and s_2 is on
0	s_1 is off and s_2 is off
-1	s_1 is off and s_2 is on

Table 4.1: The H-Bridge converter switching states

The switching state determines the relationship between the ac-side and the dc-side voltages and currents. The H-bridge switching model is presented in equation1 for the H-bridge switching model diagram is shown in figure 4.2.

$$V_{ac} = S.V_{dc}$$
$$i_{dc} = S.i_{ac} \quad (4.1)$$

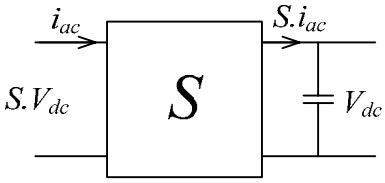


Figure 4.2: The H-Bridge converter switching model diagram

The objective of the SMO design for the functional circuit shown in figure 4.3 is to observe the capacitor voltage v_c by measuring the inductor current i_l and using knowledge of the voltage source e_s and load current i_o as system inputs.

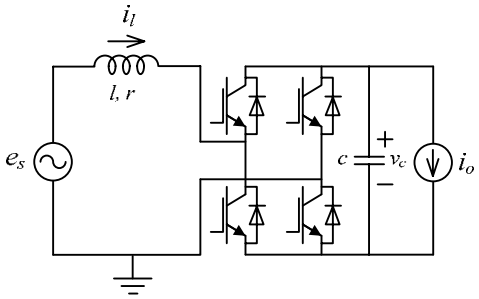


Figure 4.3: The functional circuit of the H-Bridge converter

The equivalent circuit switch diagram is shown in figure 4.4.

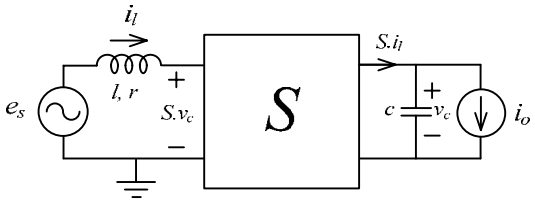


Figure 4.4: The switching diagram of the H-bridge equivalent circuit

The circuit equation in state space form is:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx \end{cases} \tag{4.2}$$

With

$$A = \begin{bmatrix} -\frac{r}{l} & -\frac{1}{l}S \\ \frac{1}{c}S & 0 \end{bmatrix} \quad B = \begin{bmatrix} 0 & \frac{1}{l} \\ -\frac{1}{c} & 0 \end{bmatrix} \quad C = \begin{bmatrix} 1 & 0 \end{bmatrix} \tag{4.3}$$

Where x is the system state vector and u is system input vector and are defined as:

$$x = \begin{bmatrix} i_l \\ v_c \end{bmatrix} \tag{4.4}$$

$$u = \begin{bmatrix} i_o \\ e_s \end{bmatrix} \tag{4.5}$$

The first step is to check the system observability. The system observability matrix is:

$$\mathcal{O} = \begin{bmatrix} C \\ CA \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-r}{l} & \frac{-1}{l}S \end{bmatrix} \tag{4.6}$$

The system is fully observable when the observability matrix $\mathcal{O}$ is full rank. Full observability means that all the system states are observable. It can be seen that the observability matrix is full rank only when $S = \pm 1$. When $S = 0$ the rank of observability matrix becomes 1, which means only i_l is observable. The canonical form of the system equations is:

$$\begin{cases} \frac{d}{dt} i_l = -\frac{1}{l}(r i_l + S v_c - e_s) \\ \frac{d}{dt} v_c = \frac{1}{c}(S i_l - i_o) \end{cases} \tag{4.7}$$

Based on observer design method discussed in chapter 3, the corresponding sliding mode observer is presented at equations 4.8 and 4.9. For $S = \pm 1$ both i_l and v_c are observable and the observer equations are:

$$\begin{cases} \frac{d}{dt} \hat{\imath}_l = -\frac{1}{l}(r \hat{\imath}_l + S v_c - e_s) - L_1 sat(\hat{\imath}_l - i_l) \\ \frac{d}{dt} \hat{v}_c = \frac{1}{c}(S \hat{\imath}_l - i_o) - L_2 sat\big(-lSL_1 sat(\hat{\imath}_l - i_l)\big) \end{cases} \tag{4.8}$$

Where $\hat{\imath}_l$ and $\hat{v}_c$ are the observed values for i_l and v_c respectively. For $S = 0$ only i_l is observable and the observer equations are:

$$\begin{cases} \frac{d}{dt} \hat{\imath}_l = -\frac{1}{l}(r \hat{\imath}_l - e_s) - L_1 sat(\hat{\imath}_l - i_l) \\ \frac{d}{dt} \hat{v}_c = \frac{1}{c}(S \hat{\imath}_l - i_o) \end{cases} \tag{4.9}$$

The simulation results for the circuit in figure 4.3 with $= 11mH$, $r = 0.5\Omega$ and $c = 1000\mu f$ are shown in figures 4.5 and 4.6. According to sliding mode condition explained in chapter 3 by equation 3.19, the observer gain $L_1 = 5000$, $L_2 = 5000$, which guarantees the sliding mode condition. The complete design of the SMO for system in figure 4.3 is presented in equation 4.10.

$$\begin{cases} \frac{d}{dt}\hat{\imath}_l = -91(0.5\hat{\imath}_l + Sv_c - e_s) - 5000sat(\hat{\imath}_l - i_l) \\ \frac{d}{dt}\hat{v}_c = 1000(S\hat{\imath}_l - i_o) - 5000sat\left(-55Ssat(\hat{\imath}_l - i_l)\right) \end{cases} \tag{4.10}$$

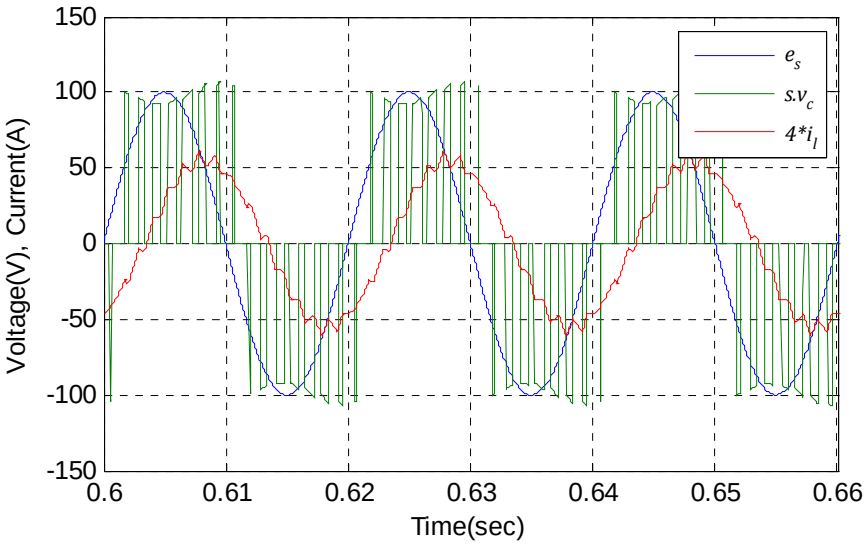


Figure 4.5: Source voltage, converter voltage and inductor current for the H-bridge

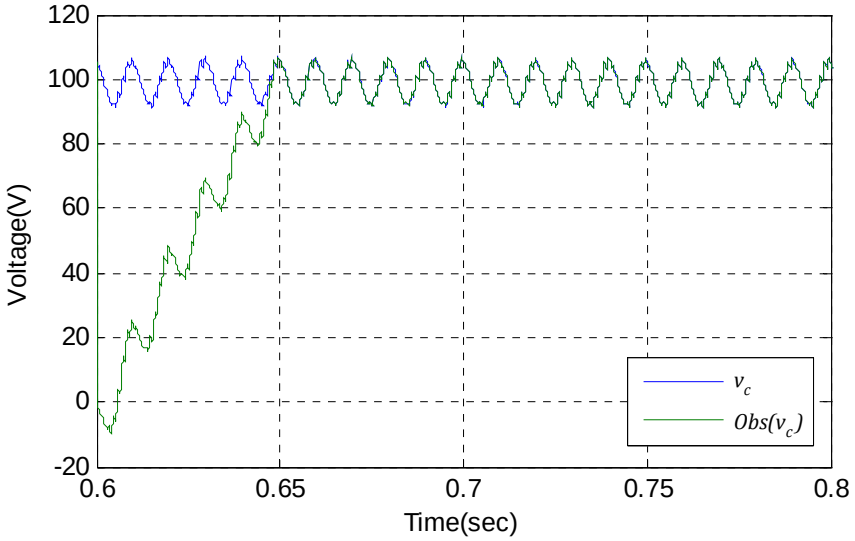
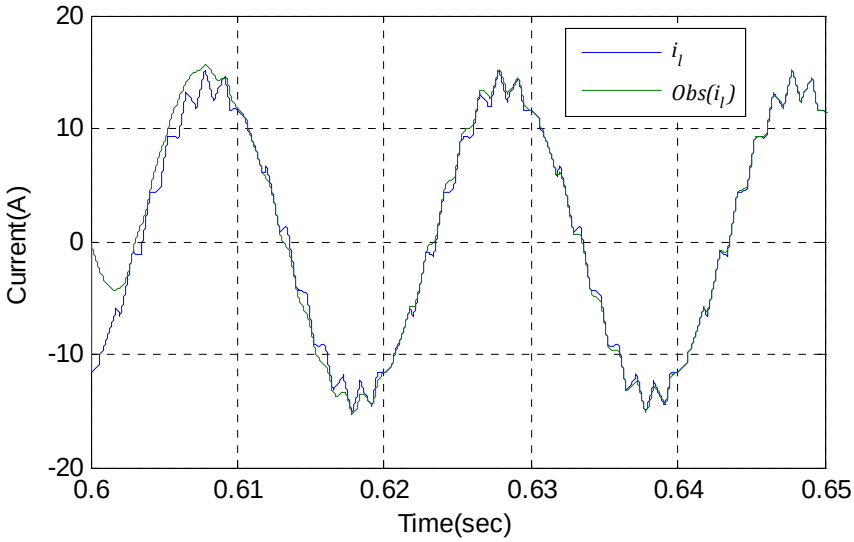


Figure 4.6 (a): The measured and observed values of capacitor voltage.



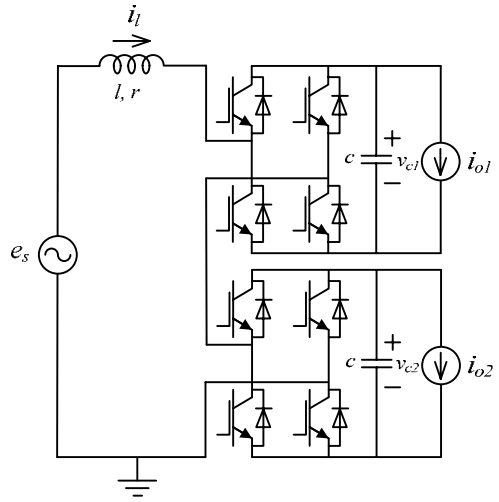
(b): The measured and observed values of inductor current.

Figure 4.6: The measured and observed values of the system variables.

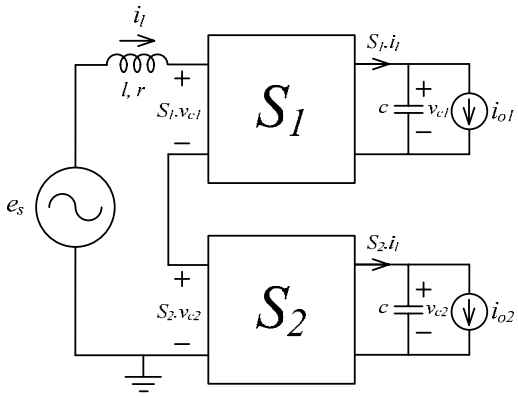
The simulation results are shown in figure 4.6. The reaching time for observed value of the capacitor voltage is $50ms$. In the sliding mode, the observed value and measured value of capacitor voltage matches perfectly. Simulation result confirms the correct operation and accuracy of proposed observation method for H-bridge converter. As explained in sections 3.5 and 3.6.2, the proposed observer for the H-bridge converter will have robustness only against variation in capacitance value and measurement error in load current i_o. Any other uncertainty in the system parameters or in system model like voltage drop across IGBTs will result in error in the observer output. Therefore in practical implementation of the observer, the voltage drop across IGBTs is modelled. This is presented in section 6.2.

4.3 SMO design for the cascaded H-bridge converter

In section 4.2 a sliding mode observer has been designed and successfully implemented on a single H-bridge converter. The complete two-port power converter is a multilevel converter comprising of cascaded H-bridge converters. Therefore it is necessary to evaluate the applicability of the proposed observer for cascaded H-bridge (CHB) multilevel converters. The topology and the switching model diagram of a two-level converter are shown in figure 4.7.



(a): The converter topology



(b): The switching model diagram

Figure 4.7: The two-level CHB converter

The circuit equation for the CHB converter in state space form is:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx \end{cases} \tag{4.11}$$

The system state vector , input vector u and constant matrices are defined as:

$$x = \begin{bmatrix} i_l \\ v_{c1} \\ v_{c2} \end{bmatrix} \tag{4.12}$$

$$u = \begin{bmatrix} i_{o1} \\ i_{o2} \\ e_s \end{bmatrix} \tag{4.13}$$

$$A = \begin{bmatrix} \frac{-r}{l} & \frac{-S_1}{l} & \frac{-S_2}{l} \\ \frac{S_1}{c} & 0 & 0 \\ \frac{S_2}{c} & 0 & 0 \end{bmatrix} \qquad B = \begin{bmatrix} 0 & 0 & \frac{1}{l} \\ -\frac{1}{c} & 0 & 0 \\ 0 & -\frac{1}{c} & 0 \end{bmatrix} \qquad C = [1 \quad 0 \quad 0] \tag{4.14}$$

Based on the switching states S_1 and S_2 there are four operating modes for the CHB topology shown in figure 4.7 as given in table 4.2.

	S_1	S_2
Mode-1	(± 1)	(± 1)
Mode-2	(± 1)	(0)
Mode-3	(0)	(± 1)
Mode-4	(0)	(0)

Table 4.2: The two-level CHB converter operation modes.

During mode-2 and mode-3 there is only one H-Bridge connected to the supply and the other H-bridge is not in circuit. The observer design method for mode-2 and mode-3 is exactly same as method used for the single H-bridge converter in the previous section. During mode-4 both H-bridges are out of circuit and system is not observable. Before designing the SMO for mode-1 the system observability is checked. The system observability matrix during mode-1 is presented in equation 4.15.

$$\mathcal{O} = \begin{bmatrix} C \\ CA \\ CA^2 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ \frac{-r}{l} & \frac{-S_1}{l} & \frac{-S_2}{l} \\ \left(\frac{r^2}{l^2} - \frac{(S_1)^2}{lc} - \frac{(S_2)^2}{lc}\right) & \frac{rS_1}{l^2} & \frac{rS_2}{l^2} \end{bmatrix} \tag{4.15}$$

The observability matrix $\mathcal{O}$ is full rank when its determinant is not zero. The determinant of equation 15 is calculated in equation 16 and it is equal to zero which means matrix $\mathcal{O}$ is not full rank. Therefore for mode-1 the system is not fully observable.

$$\det(\mathcal{O}) = -\frac{rS_1S_2}{l^3} + \frac{rS_1S_2}{l^3} = 0 \tag{4.16}$$

Hence during mode-1 none of capacitor voltages can be observed. The capacitor voltages can only be observed when there is one H-bridge connected to the supply and all the other H-bridges are out of circuit.

The switch model diagram for a 3-cell CHB converter is shown in figure 4.8. The system equations for this three-cell CHB converter are presented in equation 4.17.

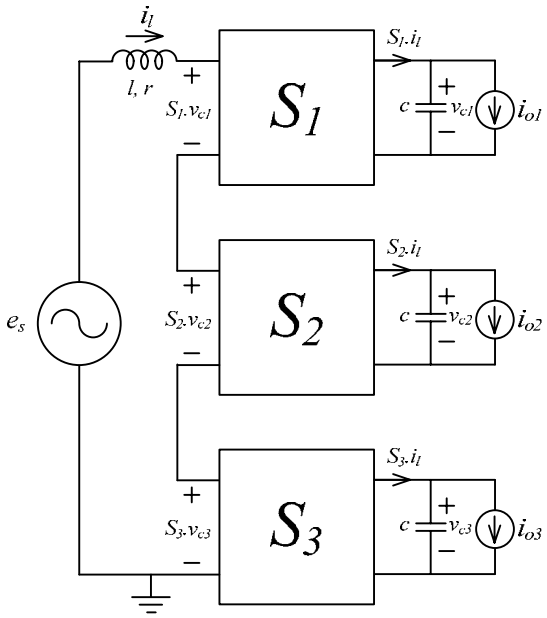


Figure 4.8: The switching model diagram of a three-level CHB converter

$$\begin{cases} \frac{d}{dt}i_l = -\frac{1}{l}(ri_l + S_1.v_{c1} + S_2.v_{c2} + S_3.v_{c3} - e_a) \\ \frac{d}{dt}v_{c1} = \frac{1}{c}(S_1.i_l - i_{o1}) \\ \frac{d}{dt}v_{c2} = \frac{1}{c}(S_2.i_l - i_{o2}) \\ \frac{d}{dt}v_{c3} = \frac{1}{c}(S_3.i_l - i_{o3}) \end{cases} \tag{4.17}$$

In a three-cell CHB converter, based on switching states of each H-bridge, there will be eight operating modes. The operating modes for the three-cell CHB converter are listed in table 4.2. As it can be seen, each capacitor voltage is observable only when the associated H-bridge is in circuit and other H-bridges are shorted. Obviously this time interval decrease as the number of cells increases.

	S_1	S_2	S_3	Observable DC-link voltages
Mode-1	(± 1)	(± 1)	(± 1)	None
Mode-2	(± 1)	(± 1)	(0)	None
Mode-3	(± 1)	(0)	(± 1)	None
Mode-4	(± 1)	(0)	(0)	v_{c1}
Mode-5	(0)	(± 1)	(± 1)	None
Mode-6	(0)	(± 1)	(0)	v_{c2}
Mode-7	(0)	(0)	(± 1)	v_{c3}
Mode-8	(0)	(0)	(0)	None

Table 4.2: The operating modes for the three-cell CHB converter.

For mode-4 only v_{c1} and i_l are observable, shown by the observer equations presented in equation 4.18.

$$\begin{cases} \frac{d}{dt}\hat{\imath}_l = -\frac{1}{l}(r\hat{\imath}_l + S_1.\hat{v}_{c1} - e_a) - L_1 sat(\hat{\imath}_l - i_l) \\ \frac{d}{dt}\hat{v}_{c1} = \frac{1}{c}(S_1.\hat{\imath}_l - i_{o1}) - L_2 sat\left(\frac{-l}{S_1}L_1 sat(\hat{\imath}_l - i_l)\right) \end{cases} \tag{4.18}$$

For mode-6 only v_{c2} and i_l are observable, shown by the observer equations presented in equation 4.19.

$$\begin{cases} \frac{d}{dt}\hat{\imath}_l = -\frac{1}{l}(r\hat{\imath}_l + S_2.\hat{v}_{c2} - e_a) - L_1 sat(\hat{\imath}_l - i_l) \\ \frac{d}{dt}\hat{v}_{c2} = \frac{1}{c}(S_2.\hat{\imath}_l - i_{o2}) - L_2 sat\left(\frac{-l}{S_2}L_1 sat(\hat{\imath}_l - i_l)\right) \end{cases} \tag{4.19}$$

For mode-7 only v_{c3} and i_l are observable, shown by the observer equations presented in equation 4.20.

$$\begin{cases} \frac{d}{dt}\hat{\imath}_l = -\frac{1}{l}(r\hat{\imath}_l + S_3.\hat{v}_{c3} - e_a) - L_1 sat(\hat{\imath}_l - i_l) \\ \frac{d}{dt}\hat{v}_{c3} = \frac{1}{c}(S_3.\hat{\imath}_l - i_{o3}) - L_2 sat\left(\frac{-l}{S_3}L_1 sat(\hat{\imath}_l - i_l)\right) \end{cases} \quad (4.20)$$

For the other modes only i_l is observable. The SMO equation for i_l is:

$$\frac{d}{dt}\hat{\imath}_l = -\frac{1}{l}(r\hat{\imath}_l + S_1.\hat{v}_{c1} + S_2.\hat{v}_{c2} + S_3.\hat{v}_{c3} - e_a) - L_1 sat(\hat{\imath}_l - i_l) \quad (4.21)$$

The observer equation for $\hat{v}_{c1}$, $\hat{v}_{c2}$ and $\hat{v}_{c3}$ during unobservable modes 1, 2, 3, 5 and 8 are shown in equation 4.22.

$$\begin{cases} \frac{d}{dt}\hat{v}_{c1} = \frac{1}{c}(S_1.\hat{\imath}_l - i_{o1}) \\ \frac{d}{dt}\hat{v}_{c2} = \frac{1}{c}(S_2.\hat{\imath}_l - i_{o2}) \\ \frac{d}{dt}\hat{v}_{c3} = \frac{1}{c}(S_3.\hat{\imath}_l - i_{o3}) \end{cases} \quad (4.22)$$

During the unobservable modes, the voltage observer equations are a pure integrator. During these modes the voltage observer equations track the voltage ripples without trying to eliminate the offset between observed values and measured values. During these modes there is voltage drift in observed values and any uncertainty in capacitance value or any measurement error in currents will increase the voltage drift. The unobservable states increase as number of cell increases.

The sliding surface is $(\hat{\imath}_l - i_l)$. The gains L_1 and L_2 should be chosen in a way to guarantee the reaching and sliding mode conditions as explained by equations 3.14 to 3.19 in chapter 3. The simulation results for the system with $l = 11mH$, $r = 0.5\Omega$ and $c = 1000\mu f$ are shown in figures 4.9 and 4.10. The observer gains $L_1 = 5000$ and $L_2 = 5000$ guarantees the reaching mode and sliding mode condition for this example. The designed SMO equation for v_{c1} in this example during mode-4 are presented in equations 4.23.

$$\begin{cases} \frac{d}{dt}\hat{\imath}_l = -91(0.5\hat{\imath}_l + S_1.\hat{v}_{c1} - e_a) - 5000 sat(\hat{\imath}_l - i_l) \\ \frac{d}{dt}\hat{v}_{c1} = 1000(S_1.\hat{\imath}_l - i_{o1}) - 5000 sat\big(-55 S_1 sat(\hat{\imath}_l - i_l)\big) \end{cases} \quad (4.23)$$

For all the other modes:

$$\begin{cases} \frac{d}{dt}\hat{\imath}_l = -91(0.5\hat{\imath}_l + S_1.\hat{v}_{c1} + S_2.\hat{v}_{c2} + S_3.\hat{v}_{c3} - e_a) - 5000sat(\hat{\imath}_l - i_l) \\ \frac{d}{dt}\hat{v}_{c1} = 1000(S_1.\hat{\imath}_l - i_{o1}) \end{cases} \quad (4.24)$$

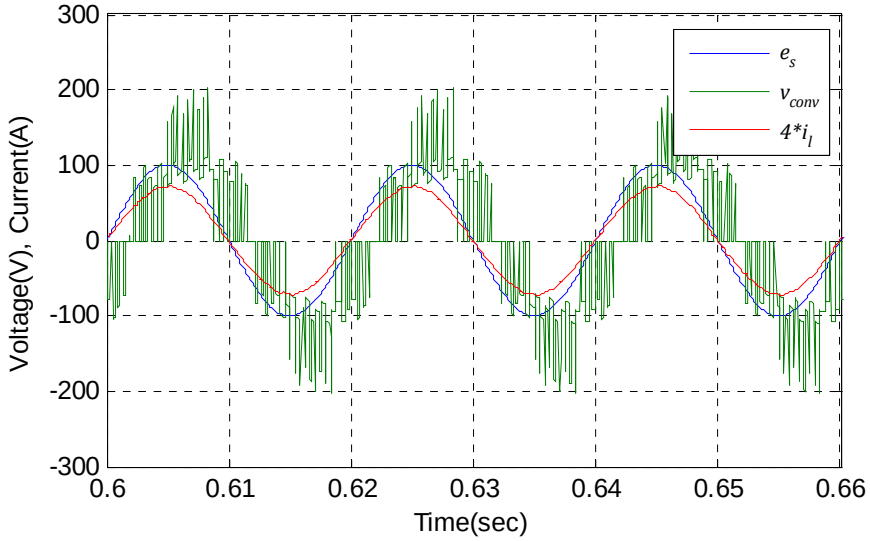


Figure 4.9: Source voltage, converter voltage and inductor current

The distorted converter voltage in figure 4.9 is because of unequal dc-link voltages. Unbalanced loads are applied to the dc-links to have three unequal dc-link voltages. By having different dc-link voltages, it is possible to evaluate the efficiency of the designed observer in observing each dc-link voltage.

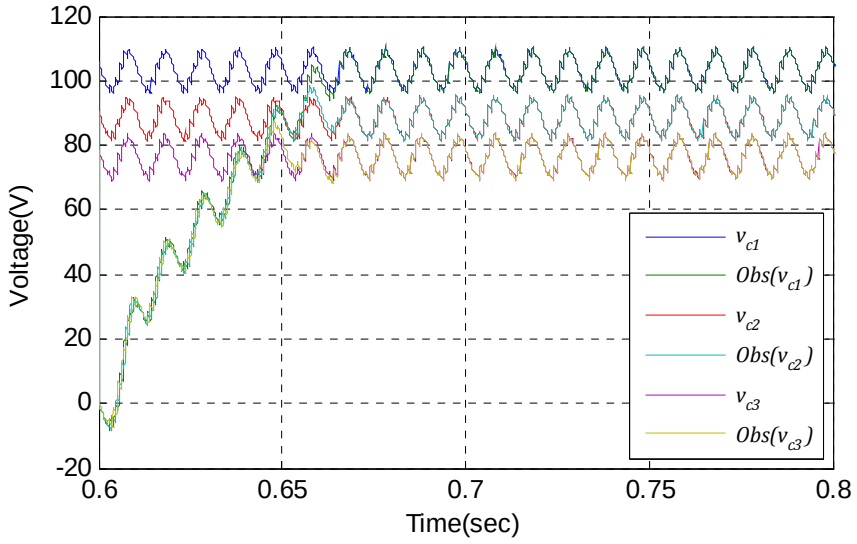


Figure 4.10(a): The measured and observed values of dc-link voltages.

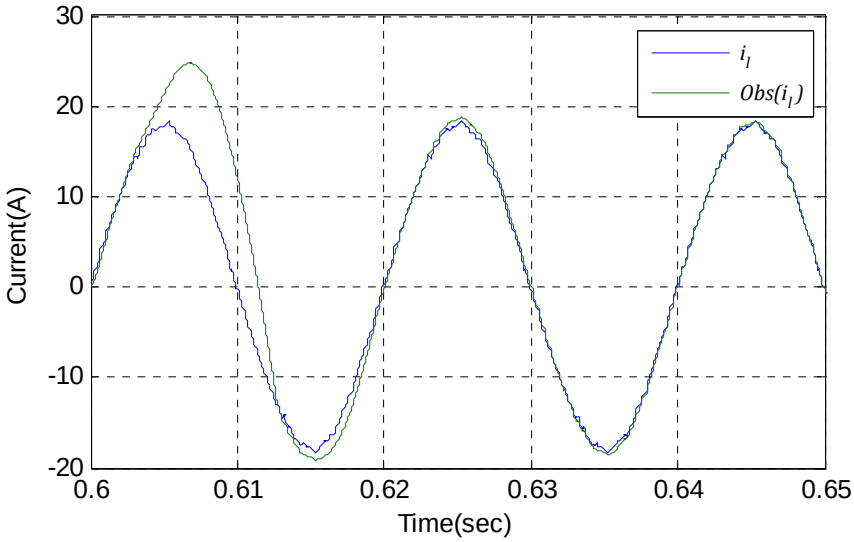


Figure 4.10(b): The measured and observed values of line current.

The reaching time for observed values for dc-link voltages is about $65ms$. In sliding mode, the observed value and measured value of the dc-link voltages are identical. Simulation result confirms the correct operation of proposed observation method for cascaded H-bridge converter.

4.4 SMO design for the three-phase CHB multilevel converter

The efficiency of the sliding mode observer using the equivalent control method for cascaded H-bridge converters has been shown in previous sections of this chapter. Almost all of works and researches in the field of application of observers on power electronic circuits have been done on single phase circuits. Application of SMO on three-phase power electronic converters is a new research area. The main issue in the three-phase power converters is the lack of direct voltage measurement of the floating node n. The SMO implementation on three-phase power converter is addressed in this section. The switching model of a three-phase CHB multilevel converter is shown in figure 4.11.

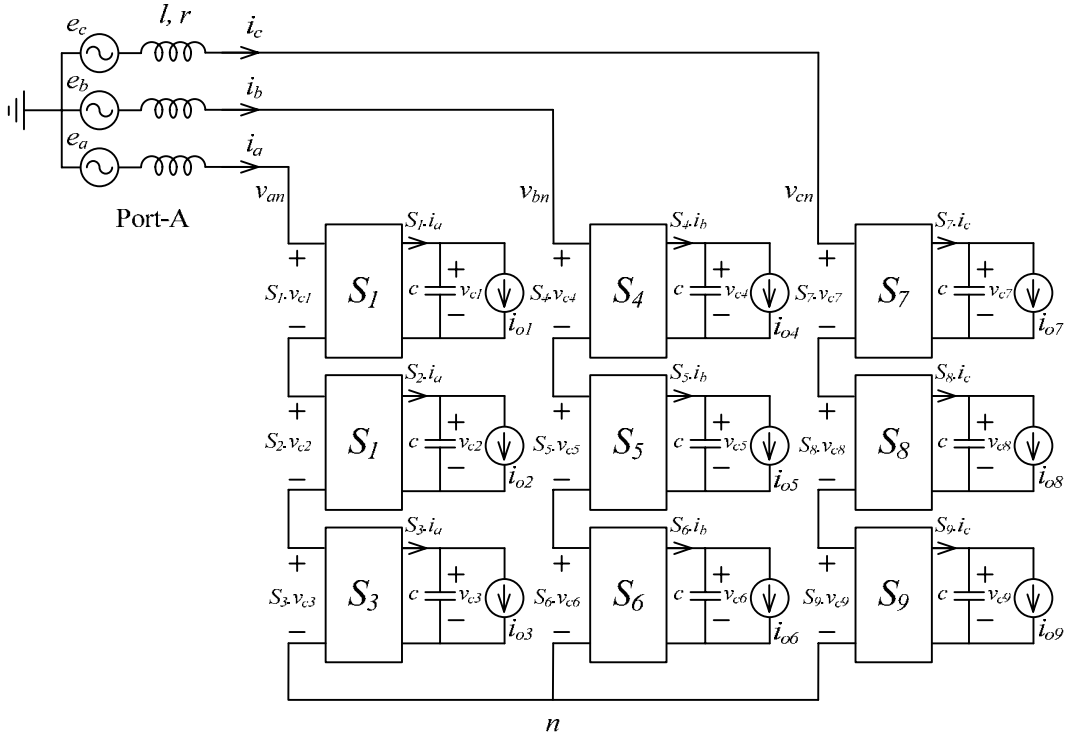


Figure 4.11: The switching model of a two-level CHB multilevel converter

The three-phase voltage equations for this converter are:

$$\begin{cases} e_a = (r + l\,s)i_a + S_1 v_{c1} + S_2 v_{c2} + S_3 v_{c3} + v_n \\ e_b = (r + l\,s)i_b + S_4 v_{c4} + S_5 v_{c5} + S_6 v_{c6} + v_n \\ e_c = (r + l\,s)i_c + S_7 v_{c7} + S_8 v_{c8} + S_9 v_{c9} + v_n \end{cases} \tag{4.25}$$

For a balanced three-phase system v_n is defined as:

$$v_n = -\frac{1}{3}\sum_{i=1}^{9} S_i v_{ci} \tag{4.26}$$

The three-phase equations for this converter in state-space form are presented in equations 4.27, 4.28 and 4.29.

$$\begin{cases} \frac{d}{dt} i_a = -\frac{1}{l}(r i_a + S_1.v_{c1} + S_2.v_{c2} + S_3.v_{c3} - e_a + v_n) \\ \frac{d}{dt} v_{c1} = \frac{1}{c}(S_1.i_a - i_{o1}) \\ \frac{d}{dt} v_{c2} = \frac{1}{c}(S_2.i_a - i_{o2}) \\ \frac{d}{dt} v_{c3} = \frac{1}{c}(S_3.i_a - i_{o3}) \end{cases} \quad (4.27)$$

$$\begin{cases} \frac{d}{dt} i_b = -\frac{1}{l}(r i_b + S_4.v_{c4} + S_5.v_{c5} + S_6.v_{c6} - e_b + v_n) \\ \frac{d}{dt} v_{c4} = \frac{1}{c}(S_4.i_b - i_{o4}) \\ \frac{d}{dt} v_{c5} = \frac{1}{c}(S_5.i_b - i_{o5}) \\ \frac{d}{dt} v_{c6} = \frac{1}{c}(S_6.i_b - i_{o6}) \end{cases} \quad (4.28)$$

$$\begin{cases} \frac{d}{dt} i_c = -\frac{1}{l}(r i_c + S_7.v_{c7} + S_8.v_{c8} + S_9.v_{c9} - e_c + v_n) \\ \frac{d}{dt} v_{c7} = \frac{1}{c}(S_7.i_c - i_{o7}) \\ \frac{d}{dt} v_{c8} = \frac{1}{c}(S_8.i_c - i_{o8}) \\ \frac{d}{dt} v_{c9} = \frac{1}{c}(S_9.i_c - i_{o9}) \end{cases} \quad (4.29)$$

The corresponding observer equations for v_{c1} in phase-a is shown in equations 4.30 and 4.31.

$$\begin{cases} \frac{d}{dt} \hat{\imath}_a = -\frac{1}{l}\left(r\hat{\imath}_a + S_1.\hat{v}_{c1} - e_a - \frac{1}{3}\sum_{i=1}^{9} S_i \hat{v}_{ci} \right) - L_1 sat(\hat{\imath}_a - i_a) \\ \frac{d}{dt} \hat{v}_{c1} = \frac{1}{c}(S_1.\hat{\imath}_a - i_{o1}) - L_2 sat\left(-lS_1 L_1 sat(\hat{\imath}_a - i_a)\right) \end{cases} \quad (4.30)$$

Equation 4.30 is valid for ($S_1 = \pm 1 \; and \; S_2 = 0 \; and \; S_3 = 0$) and equation 4.31 is valid for all other modes.

$$\begin{cases} \frac{d}{dt} \hat{\imath}_a = -\frac{1}{l}\left(r\hat{\imath}_a + \sum_{i=1}^{3} S_i \hat{v}_{ci} - e_a - \frac{1}{3}\sum_{i=1}^{9} S_i \hat{v}_{ci} \right) - L_1 sat(\hat{\imath}_a - i_a) \\ \frac{d}{dt} \hat{v}_{c1} = \frac{1}{c}(S_1.\hat{\imath}_a - i_{o1}) \end{cases} \quad (4.31)$$

The SMO equations for all the other capacitor voltages can be derived in the same way. The simulation results for the system with $l = 11mH, r = 0.5\Omega$ and $c = 1000\mu f$ are presented in figures 4.12 and 4.13. The observer gains $L_1 = 5000$ and $L_2 = 5000$ guarantees the sliding condition. The designed SMO equation for v_{c1} for ($S_1 = \pm 1$ and $S_2 = 0$ and $S_3 = 0$) are presented in equations 4.32 and 4.33.

$$\begin{cases} \frac{d}{dt}\hat{\imath}_a = -91\left(0.5\hat{\imath}_a + S_1.\hat{v}_{c1} - e_a - \frac{1}{3}\sum_{i=1}^{9} S_i\hat{v}_{ci}\right) - 5000sat(\hat{\imath}_a - i_a) \\ \frac{d}{dt}\hat{v}_{c1} = 1000(S_1.\hat{\imath}_a - i_{o1}) - 5000sat\left(-55S_1sat(\hat{\imath}_a - i_a)\right) \end{cases} \quad (4.32)$$

For all the other modes:

$$\begin{cases} \frac{d}{dt}\hat{\imath}_a = -91\left(0.5\hat{\imath}_a + \sum_{i=1}^{3} S_i\hat{v}_{ci} - e_a - \frac{1}{3}\sum_{i=1}^{9} S_i\hat{v}_{ci}\right) - L_1sat(\hat{\imath}_a - i_a) \\ \frac{d}{dt}\hat{v}_{c1} = 1000(S_1.\hat{\imath}_a - i_{o1}) \end{cases} \quad (4.33)$$

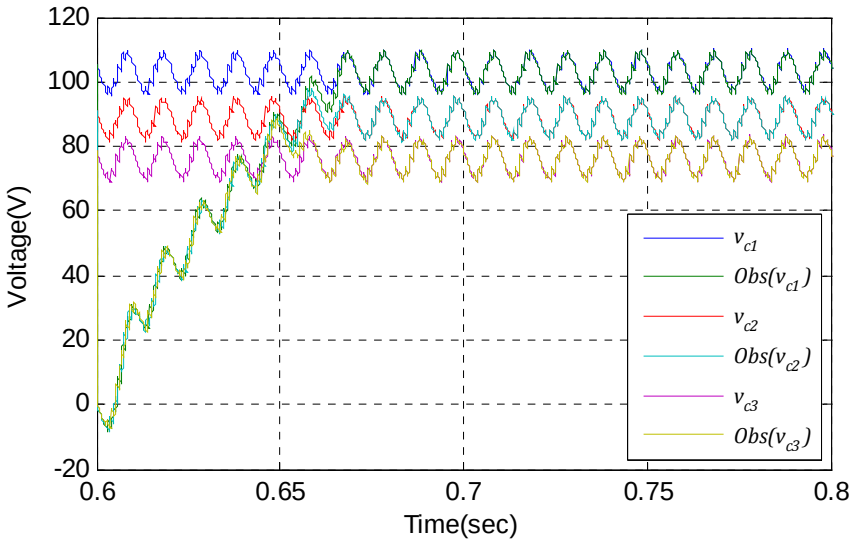


Figure 4.12: The measured and observed values of the capacitor voltages in phase-a of the three-phase, three-cell CHB converter

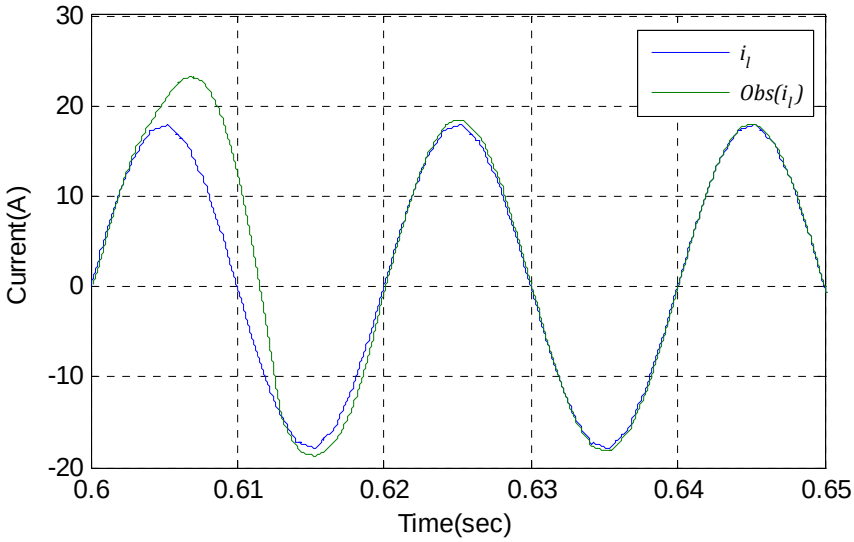


Figure 4.13: The measured and observed values of the line current in phase-a of the three-phase, three-cell CHB converter

The reaching time for observed values for dc-link voltages is about $68ms$. In sliding mode, the observed value and measured value of the dc-link voltages are identical. Simulation result confirms the correct operation of proposed observation method for three-phase, three-cell H-bridge converter.

4.5 SMO design for the back-to-back converter topology

So far it has been shown that the proposed SMO is successfully applicable for cascade H-bridge converters and three-phase multilevel power converters. The two-port power converter consists of back-to-back converters with isolation DC-DC converter. Therefore it is necessary to prove the applicability of the SMO for the back-to-back converter topology. The structure of a back-to-back converter topology is shown in figure 4.14. The switching model diagram of the back-to-back topology is presented in figure 4.15.

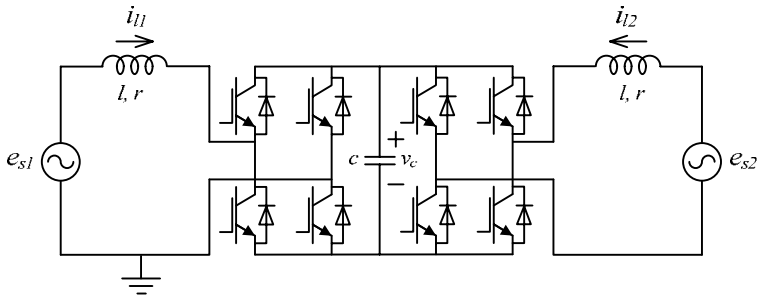


Figure 4.14: The back-to-back converter topology

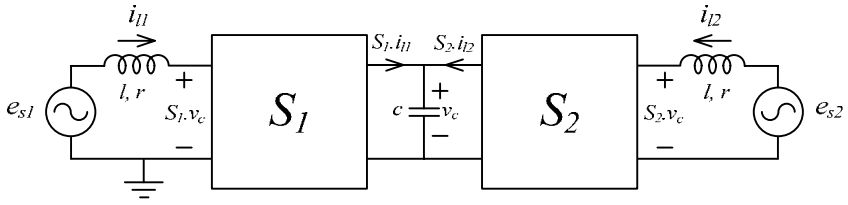


Figure 4.15: The switching model for the back-to-back converter topology

The canonical form of the system equations is given in equation 4.34.

$$\begin{cases} \frac{d}{dt} i_{l1} = -\frac{1}{l}(r i_{l1} + S_1 v_c - e_{s1}) \\ \frac{d}{dt} v_c = \frac{1}{c}(S_1 i_{l1} + S_2 i_{l2}) \end{cases} \tag{4.34}$$

The corresponding sliding mode observer can be written as:

$$\begin{cases} \frac{d}{dt} \hat{\imath}_{l1} = -\frac{1}{l}(r \hat{\imath}_{l1} + S_1 \hat{v}_c - e_{s1}) - L_1 sat(\hat{\imath}_{l1} - i_{l1}) \\ \frac{d}{dt} \hat{v}_c = \frac{1}{c}(S_1 \hat{\imath}_{l1} + S_2 i_{l2}) - L_2 sat\big(-l S_1 L_1 sat(\hat{\imath}_{l1} - i_{l1})\big) \end{cases} \tag{4.35}$$

The simulation results for the system with $= 11mH$, $r = 0.5\Omega$ and $c = 1000\mu f$ are presented in figures 4.16 and 4.17. The ports of the converter are connected to voltage sources with different frequencies. The supply frequencies are $50Hz$ and $60Hz$. The observer gains $L_1 = 5000$ and $L_2 = 5000$ guarantees the sliding condition.

The observer equations are:

$$\begin{cases} \frac{d}{dt}\hat{\imath}_{l1} = -91(0.5\hat{\imath}_{l1} + S_1\hat{v}_c - e_{s1}) - 5000sat(\hat{\imath}_{l1} - i_{l1}) \\ \frac{d}{dt}v_c = 1000(S_1\hat{\imath}_{l1} + S_2 i_{l2}) - 5000sat\left(-55S_1 sat(\hat{\imath}_{l1} - i_{l1})\right) \end{cases} \tag{4.36}$$

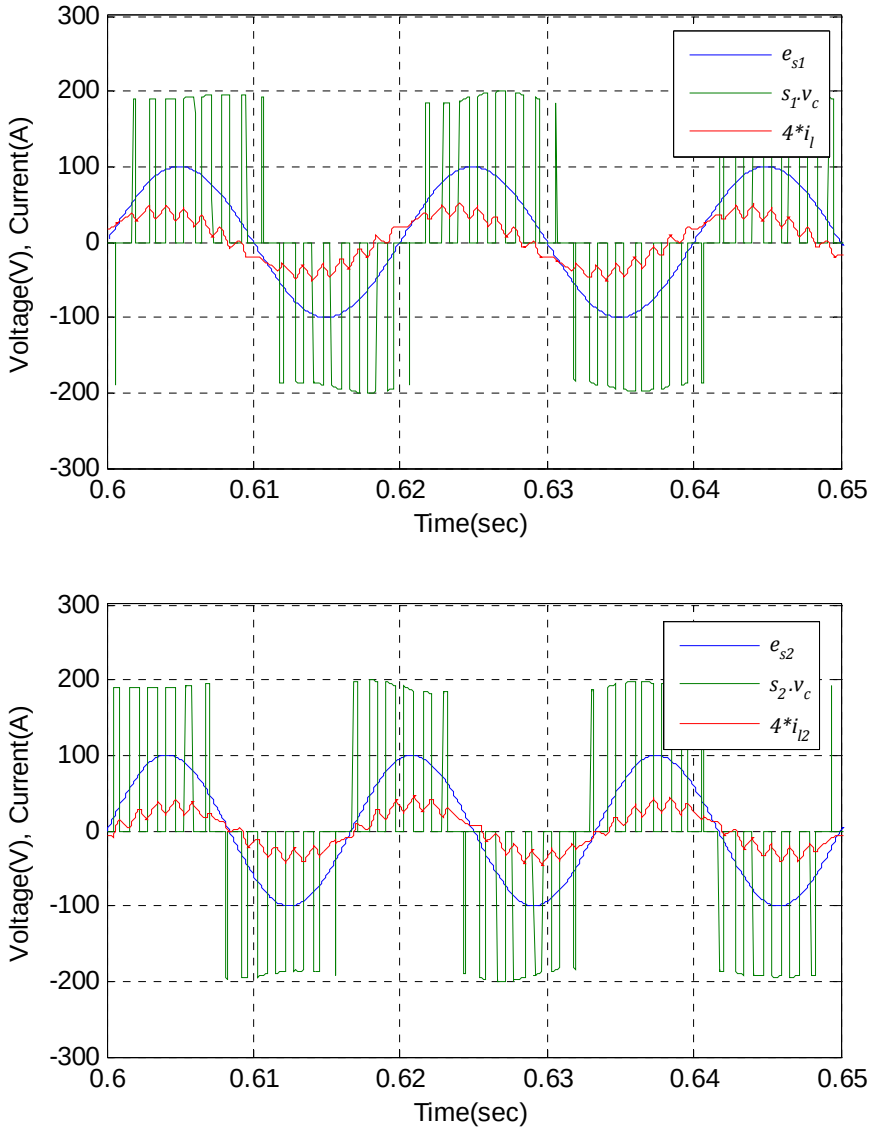


Figure 4.16: Source voltages, converter voltages and inductor currents at each port.

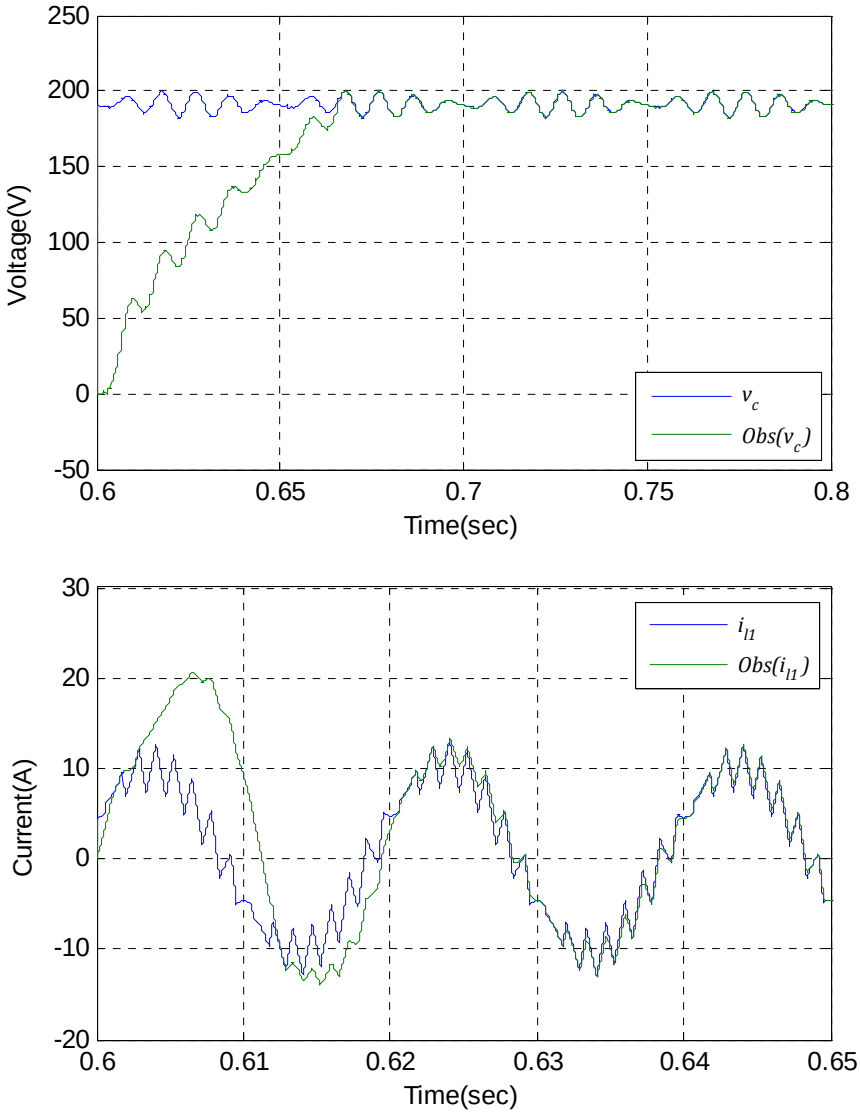


Figure 4.17: Measured and observed values of system states.

The reaching time for observed values for capacitor voltage is about $67ms$. In sliding mode, the observed value and measured value of the capacitor voltage are identical. Simulation result confirms the correct operation of proposed observation method for the back-to-back converter topology.

4.6 SMO for the back-to-back topology with a DC-DC converter

The back-to-back converter with DC-DC converter is the building block of the two-port power converter. The sliding mode observer has been successfully implemented on a back-to-back converter in previous section. In this section the applicability of the sliding mode observer on the back-to-back topology with isolation DC-DC converter will be evaluated. The structure of the back-to-back topology with DC-DC converter is shown in figure 4.18.

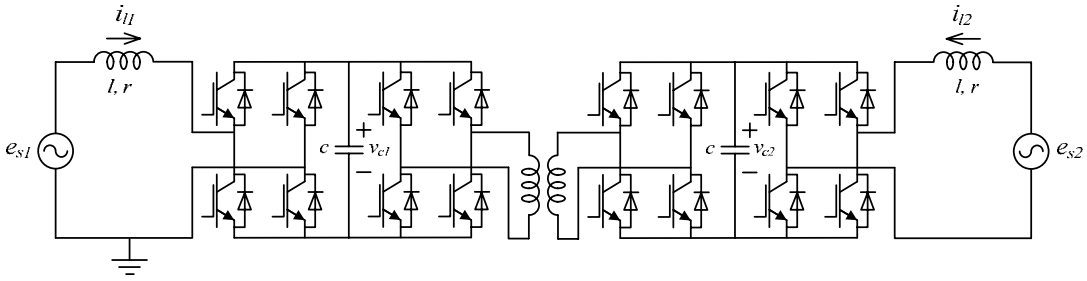


Figure 4.18: The back-to-back topology with isolation DC-DC converter

The SMO design for the back-to-back topology was described in previous section. The effect of adding the isolation DC-DC converter on the SMO equations is considered in this section. The DC-DC converter topology is shown in figure 4.19.

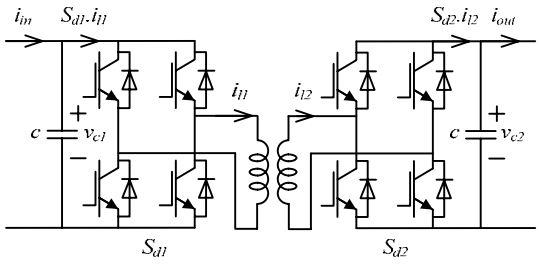


Figure 4.19: The DC-DC converter topology

The basic operating principles of the DC-DC converter are explained in Chapter 2. The i_{l1} and i_{l2} currents are almost equal if losses and magnetising current are ignored. The leakage inductance of the medium frequency transformer with 1:1 turns ratio in the DC-DC converter is small therefore the DC-DC converter operates with only a small phase shift. Having a small phase shift means that the terminal currents $S_{d1}i_{l1}$ and $S_{d2}i_{l2}$ are almost equal. The terminal voltages of the DC-DC converter are also almost equal, therefore the following assumption can be stated:

$$v_{c1} \approx v_{c2}$$
$$S_{d1} i_{l1} \approx S_{d2} i_{l2} \tag{4.37}$$

The switching model diagram of the DC-DC converter is presented in figure 4.20

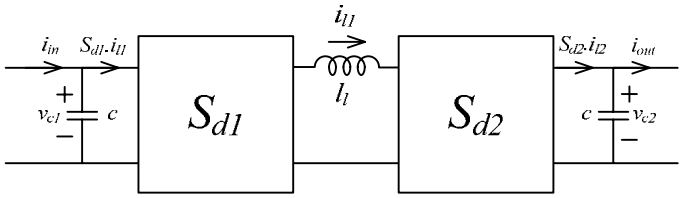


Figure 4.20: The switching model diagram DC-DC converter

Where l_l is the leakage inductance of the transformer. Using equation 4.37 a simplified functional model of switching diagram of DC-DC converter can be derived. This simplified model of the DC-DC converter is presented in figure 4.21.

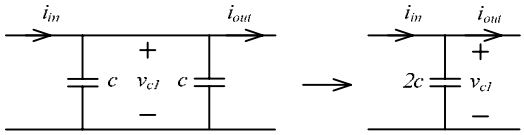


Figure 4.21: The simplified model of DC-DC converter

The switching model diagram of the back-to-back topology with a DC-DC converter is shown in 4.22 and the corresponding simplified switching model is presented in figure 4.23.

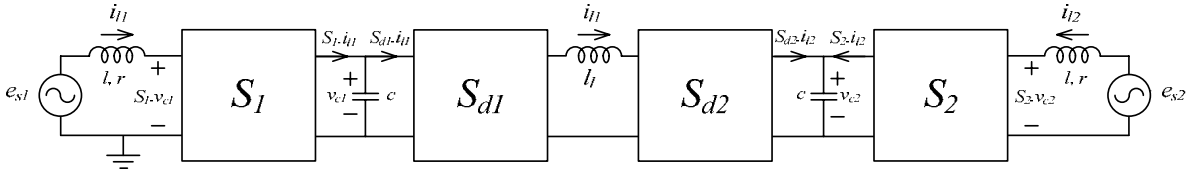


Figure 4.22: The switching model for the back-to-back topology with an isolated DC-DC converter

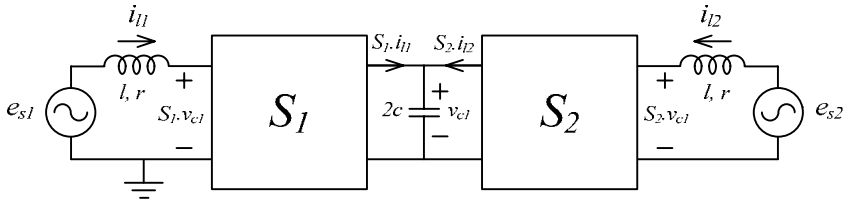


Figure 4.23: The simplified model for the back-to-back topology with an isolated DC-DC

The canonical form of the system equations can then be defined:

$$\begin{cases} \frac{d}{dt} i_{l1} = -\frac{1}{l}(r i_{l1} + S_1 v_{c1} - e_{s1}) \\ \frac{d}{dt} v_{c1} = \frac{1}{2c}(S_1 i_{l1} + S_2 i_{l2}) \end{cases} \tag{4.38}$$

The corresponding sliding mode observer is:

$$\begin{cases} \frac{d}{dt} \hat{\imath}_{l1} = -\frac{1}{l}(r \hat{\imath}_{l1} + S_1 \hat{v}_{c1} - e_{s1}) - L_1 sat(\hat{\imath}_{l1} - i_{l1}) \\ \frac{d}{dt} \hat{v}_{c1} = \frac{1}{2c}(S_1 \hat{\imath}_{l1} + S_2 i_{l2}) - L_2 sat\big(-l S_1 L_1 sat(\hat{\imath}_{l1} - i_{l1})\big) \end{cases} \tag{4.39}$$

The simulation results for the system with $= 11mH$, $r = 0.5\Omega$ and $c = 1000\mu f$ are presented in figures 4.24 – 4.26. The ports of the converter are connected to voltage sources with different frequencies. The supply frequencies are $50Hz$ and $60Hz$. The observer gains $L_1 = 5000$ and $L_2 = 5000$ guarantee the sliding condition.

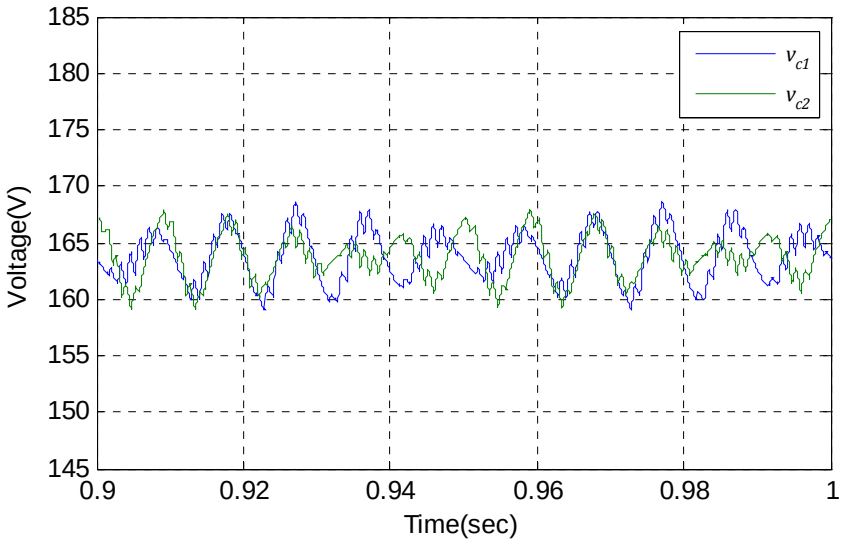
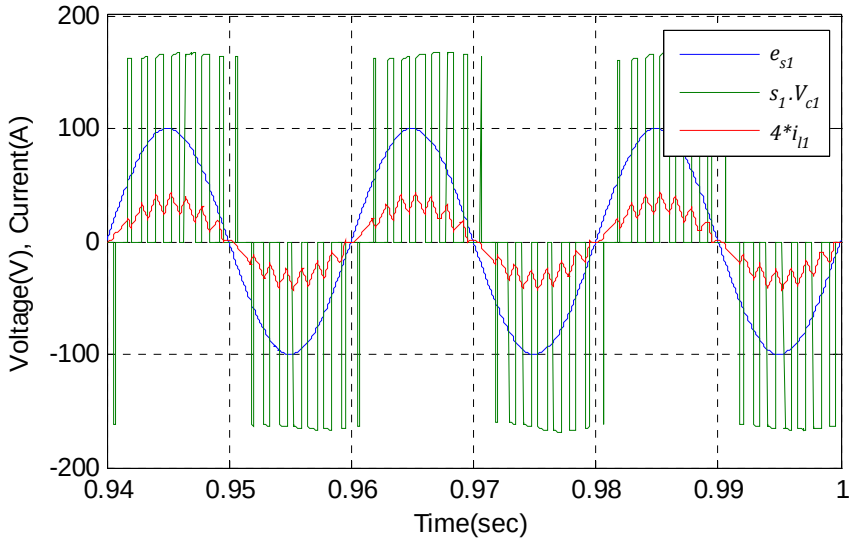
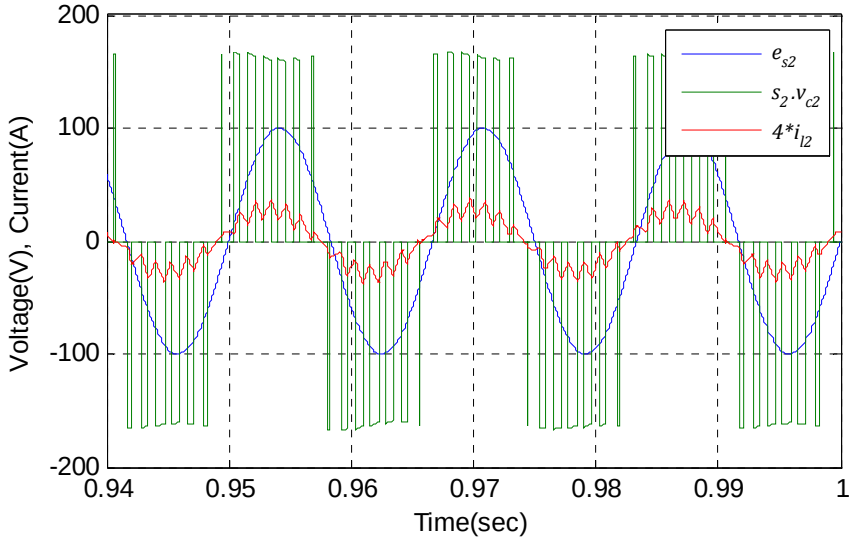


Figure 4.24: The voltages across the DC-DC converter terminals.



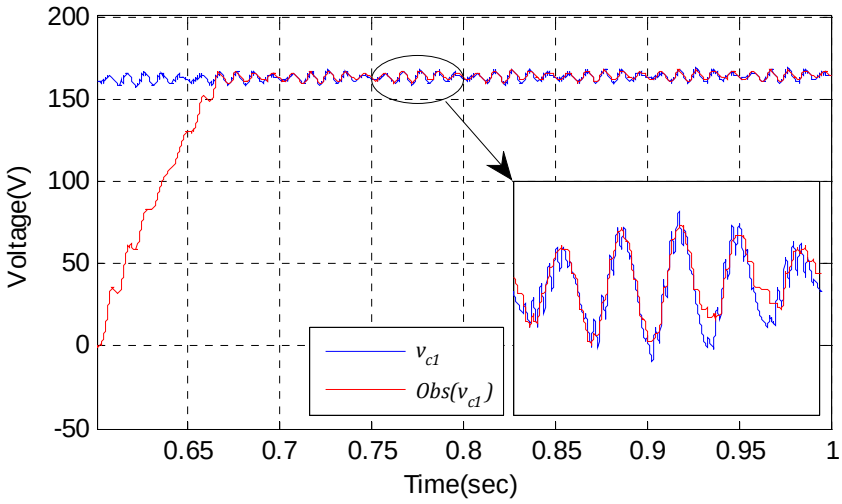
(a): Source voltage, converter voltage and inductor current at port-1.



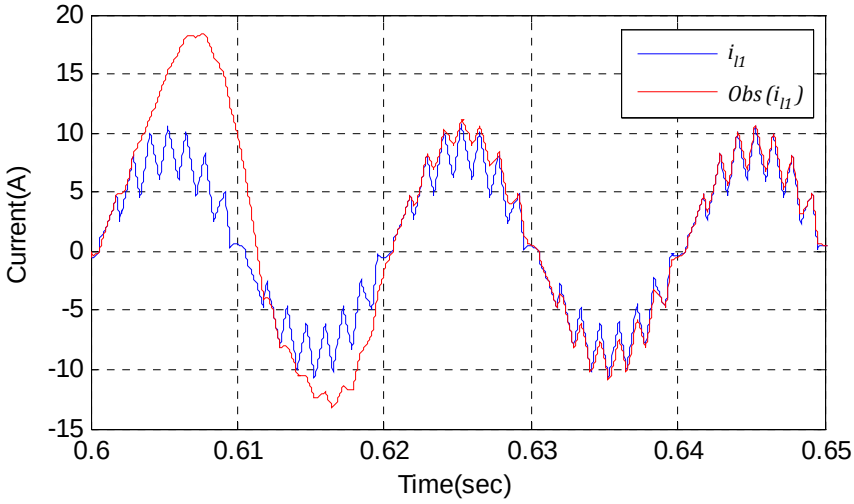
(b): Source voltage, converter voltage and inductor current at port-2.

Figure 4.25: The back-to-back converter waveforms.

As it can be seen in figure 4.24 the ripple frequencies of two capacitor voltages are different because of the different supply frequencies. The supply voltage, converter voltage and line current for each port are shown in figure 4.25. The power flow direction is from port-1 to port-2. This is obvious as converter voltage lags supply voltage in port-1 which means that the converter is in rectification mode and the supply voltage lags the converter voltage in port-2 which means that converter at port-2 is in inversion mode.



(a): Capacitor voltage.



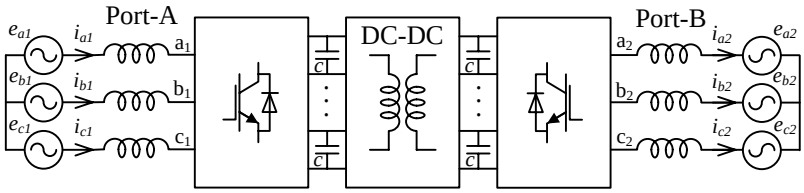
(b): line current.

Figure 4.26: Measured and observed values of system variables.

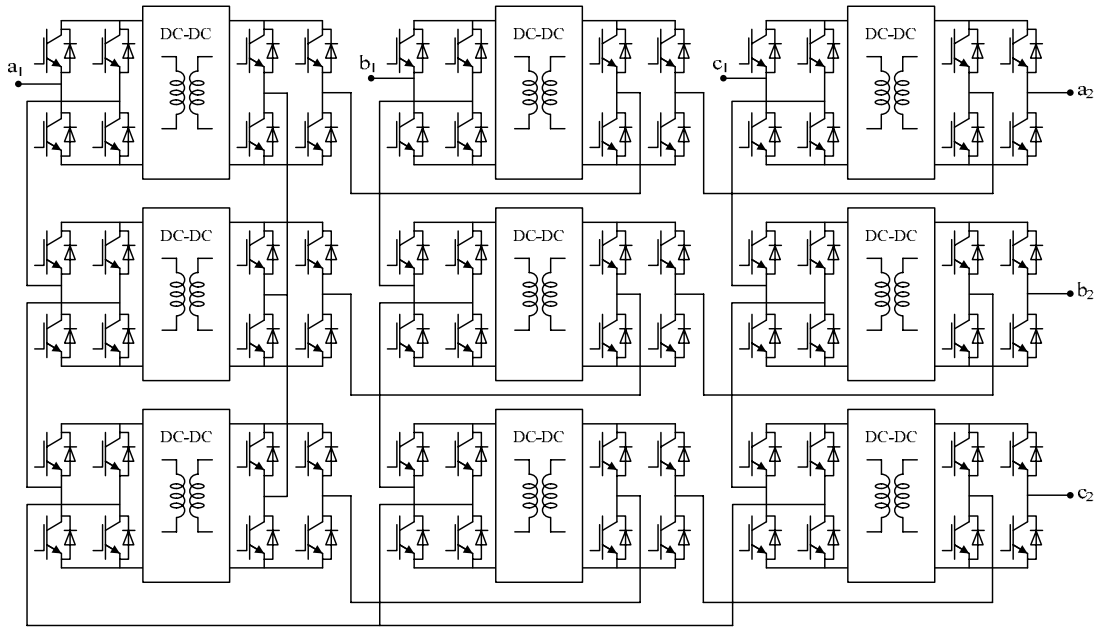
The reaching time for observed values for capacitor voltage is about $66ms$. In sliding mode, the observed value and measured value of the capacitor voltage are not quite identical. This is because of DC-DC converter and approximation made in observer equations. Simulation result confirms the correct operation of proposed observation method for the back-to-back converter with DC-DC converter.

4.7 The Sliding mode observer for the complete two-port power converter

The efficiency of 'sliding mode observer using the equivalent control method' for three-phase, three-cell power converter and back-to-back converter with DC-DC converter has been proved in the earlier sections of this chapter. The two-port power converter is a combination of converters which has been considered so far. In this section the sliding mode observer will be designed and implemented on a complete two-port power converter. The structure of the complete two-port power converter is shown in figure 4.27.



(a) Grid connection



(b) Converter topology

Figure 4.27: The two port power converter.

The two port power converter comprises of nine modules. Each module includes a back-to-back converter with a DC-DC converter isolation stage. In order to simplify the mathematical model of the two-port power converter, each module will be replaced by the model described in figure 4.23. This will result in the simplified model of two-port converter presented in figure 4.28.

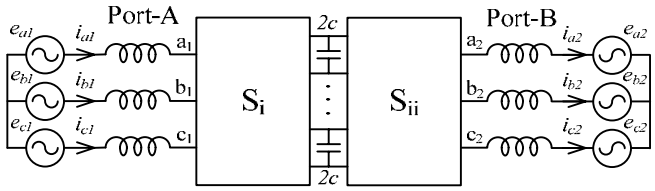


Figure 4.28: The simplified switching model of the two-port power converter.

The effect of port-B on observer equations can be modelled by current sources. The final model of the two-port converter used to design the SMO is presented in figure 4.29.

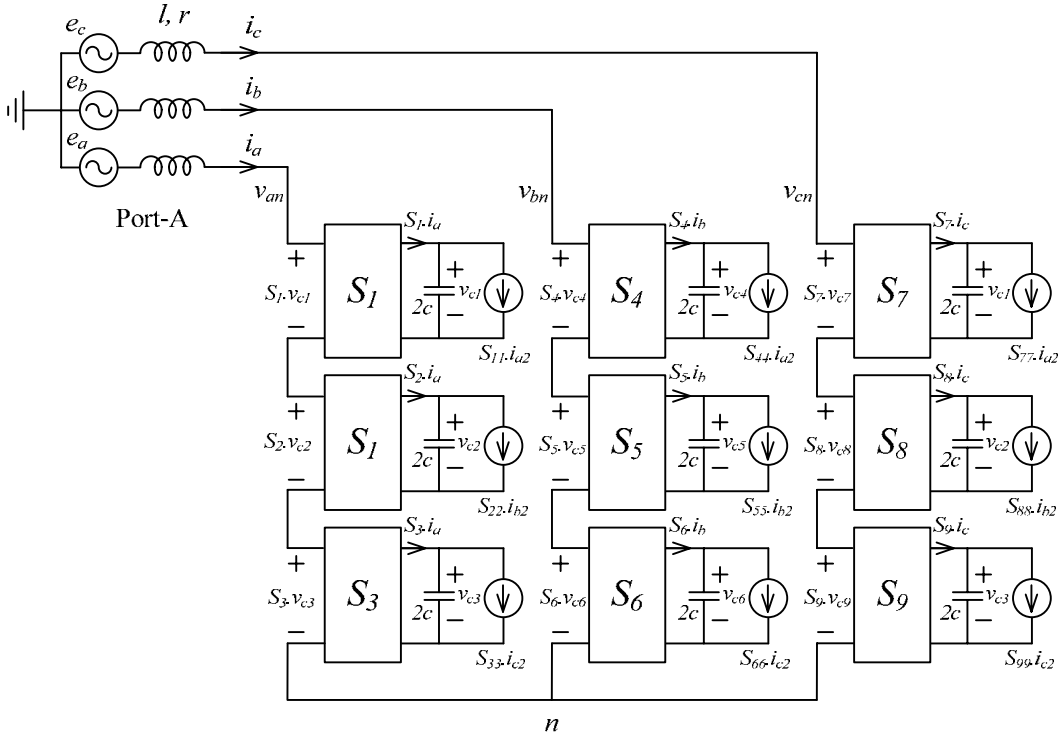


Figure 4.29: The simplified switching model of the two-port power converter

The three-phase voltage equations at port-A are:

$$\begin{cases} e_{a1} = (r + l\,s)i_{a1} + S_1 v_{c1} + S_2 v_{c2} + S_3 v_{c3} + v_n \\ e_{b1} = (r + l\,s)i_{b1} + S_4 v_{c4} + S_5 v_{c5} + S_6 v_{c6} + v_n \\ e_{c1} = (r + l\,s)i_{c1} + S_7 v_{c7} + S_8 v_{c8} + S_9 v_{c9} + v_n \end{cases} \tag{4.40}$$

In a balanced three-phase system v_n is:

$$v_n = -\frac{1}{3}\sum_{i=1}^{9} S_i v_{ci} \tag{4.41}$$

The three-phase equations in state-space form are presented in equations 4.42, 4.43 and 4.44.

$$\begin{cases} \frac{d}{dt} i_{a1} = -\frac{1}{l}(r i_{a1} + S_1.\, v_{c1} + S_2.\, v_{c2} + S_3.\, v_{c3} - e_{a1} + v_n) \\ \frac{d}{dt} v_{c1} = \frac{1}{2c}(S_1.\, i_{a1} - S_{11}.\, i_{a2}) \\ \frac{d}{dt} v_{c2} = \frac{1}{2c}(S_2.\, i_{a1} - S_{22}.\, i_{b2}) \\ \frac{d}{dt} v_{c3} = \frac{1}{2c}(S_3.\, i_{a1} - S_{33}.\, i_{c2}) \end{cases} \tag{4.42}$$

$$\begin{cases} \frac{d}{dt} i_{b1} = -\frac{1}{l}(r i_{b1} + S_4.\, v_{c4} + S_5.\, v_{c5} + S_6.\, v_{c6} - e_{b1} + v_n) \\ \frac{d}{dt} v_{c4} = \frac{1}{2c}(S_4.\, i_{b1} - S_{44}.\, i_{a2}) \\ \frac{d}{dt} v_{c5} = \frac{1}{2c}(S_5.\, i_{b1} - S_{55}.\, i_{b2}) \\ \frac{d}{dt} v_{c6} = \frac{1}{2c}(S_6.\, i_{b1} - S_{66}.\, i_{c2}) \end{cases} \tag{4.43}$$

$$\begin{cases} \frac{d}{dt} i_{c1} = -\frac{1}{l}(r i_{c1} + S_7.\, v_{c7} + S_8.\, v_{c8} + S_9.\, v_{c9} - e_{c1} + v_n) \\ \frac{d}{dt} v_{c7} = \frac{1}{2c}(S_7.\, i_{c1} - S_{77}.\, i_{a2}) \\ \frac{d}{dt} v_{c8} = \frac{1}{2c}(S_8.\, i_{c1} - S_{88}.\, i_{b2}) \\ \frac{d}{dt} v_{c9} = \frac{1}{2c}(S_9.\, i_{c1} - S_{99}.\, i_{c2}) \end{cases} \tag{4.44}$$

The corresponding observer equations for v_{c1} in phase-a are presented in equations 4.45 and 4.46. For the mode where $S_1 = \pm 1$ and $S_2 = 0$ and $S_3 = 0$ the observer equations are:

$$\begin{cases} \frac{d}{dt}\hat{\imath}_{a1} = -\frac{1}{l}\left(r\hat{\imath}_{a1} + S_1.\hat{v}_{c1} - e_{a1} - \frac{1}{3}\sum_{i=1}^{9} S_i\hat{v}_{ci}\right) - L_1 sat(\hat{\imath}_{a1} - i_{a1}) \\ \frac{d}{dt}\hat{v}_{c1} = \frac{1}{2c}(S_1.\hat{\imath}_{a1} - S_{11}.i_{a2}) - L_2 sat\left(-lS_1 L_1 sat(\hat{\imath}_{a1} - i_{a1})\right) \end{cases} \quad (4.45)$$

For all the other modes:

$$\begin{cases} \frac{d}{dt}\hat{\imath}_{a1} = -\frac{1}{l}\left(r\hat{\imath}_{a1} + \sum_{i=1}^{3} S_i\hat{v}_{ci} - e_{a1} - \frac{1}{3}\sum_{i=1}^{9} S_i\hat{v}_{ci}\right) - L_1 sat(\hat{\imath}_{a1} - i_{a1}) \\ \frac{d}{dt}\hat{v}_{c1} = \frac{1}{2c}(S_1.\hat{\imath}_{a1} - S_{11}.i_{a2}) \end{cases} \quad (4.46)$$

The SMO equations for all the other capacitor voltages can be derived in the same way. The simulation results for the system with $= 11mH$, $r = 0.5\Omega$ and $c = 1000\mu f$ are presented in figures 4.30 and 4.31. The observer gains of $L_1 = 5000$ and $L_2 = 5000$ guarantees the sliding condition. For example the SMO equations for v_{c1} for the mode where $S_1 = \pm 1$ and $S_2 = 0$ and $S_3 = 0$ are presented in equations 4.47 and 4.48.

$$\begin{cases} \frac{d}{dt}\hat{\imath}_{a1} = -91\left(0.5\hat{\imath}_{a1} + S_1.\hat{v}_{c1} - e_{a1} - \frac{1}{3}\sum_{i=1}^{9} S_i\hat{v}_{ci}\right) - 5000 sat(\hat{\imath}_{a1} - i_{a1}) \\ \frac{d}{dt}\hat{v}_{c1} = 500(S_1.\hat{\imath}_{a1} - S_{11}.i_{a2}) - 5000 sat\left(-55S_1 sat(\hat{\imath}_{a1} - i_{a1})\right) \end{cases} \quad (4.47)$$

For all the other modes:

$$\begin{cases} \frac{d}{dt}\hat{\imath}_{a1} = -91\left(0.5\hat{\imath}_{a1} + \sum_{i=1}^{3} S_i\hat{v}_{ci} - e_{a1} - \frac{1}{3}\sum_{i=1}^{9} S_i\hat{v}_{ci}\right) - 5000 sat(\hat{\imath}_{a1} - i_{a1}) \\ \frac{d}{dt}\hat{v}_{c1} = 500(S_1.\hat{\imath}_{a1} - S_{11}.i_{a2}) \end{cases} \quad (4.48)$$

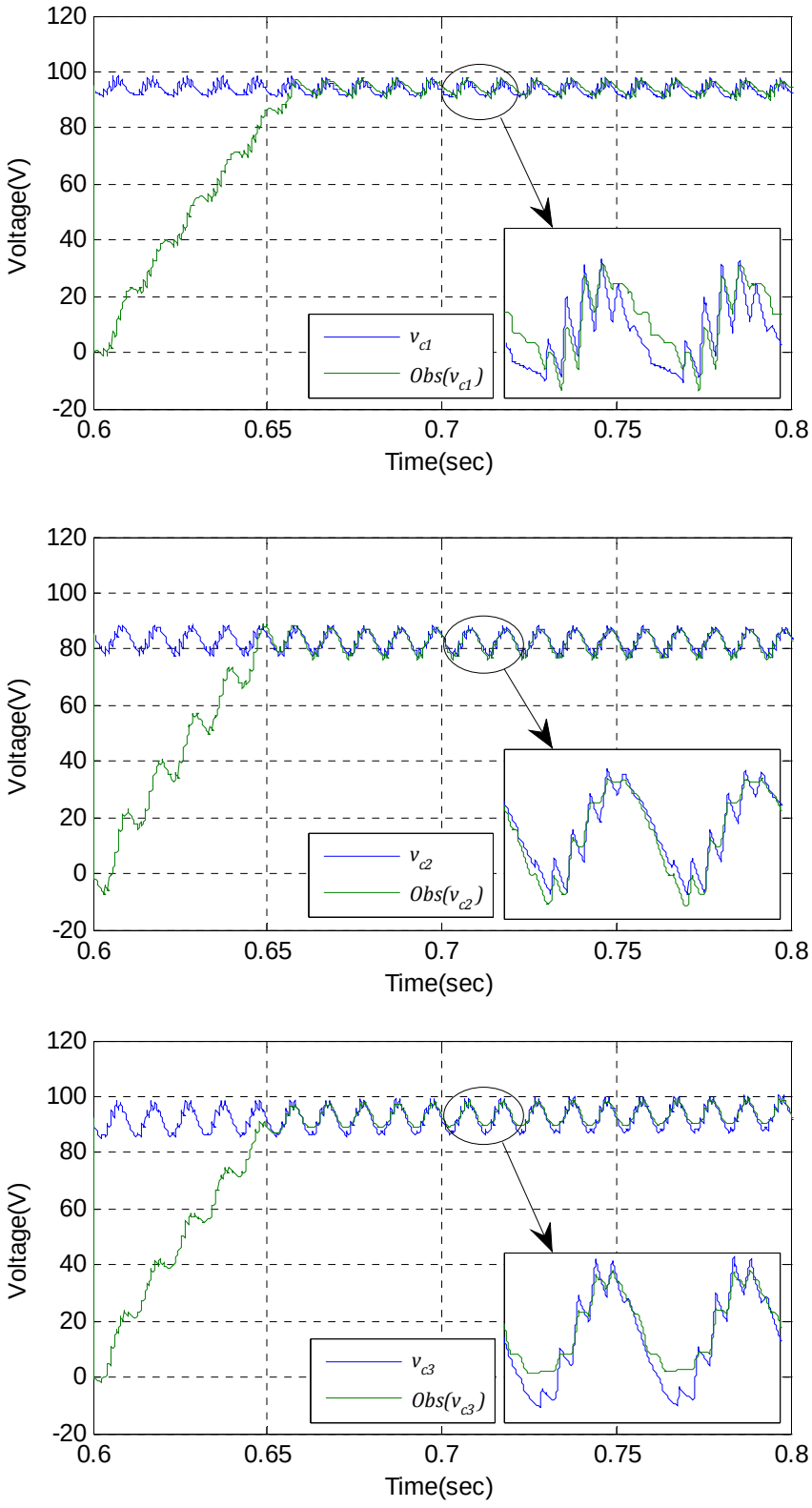


Figure 4.30: The measured and observed values of the capacitor voltages in phase-a of port-A of the two-port converter

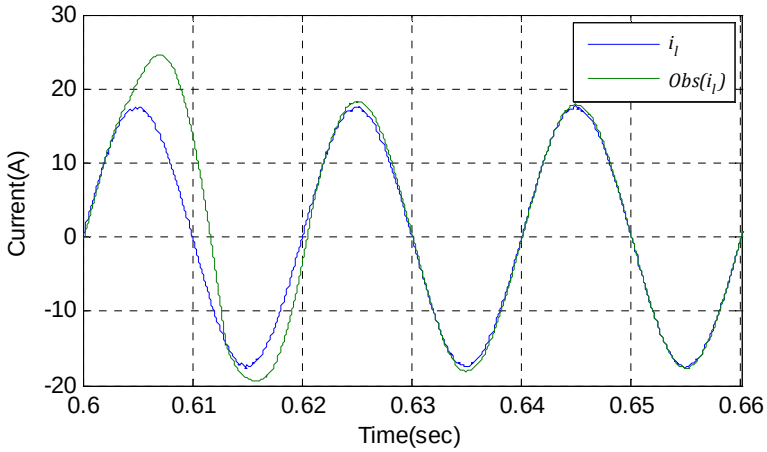


Figure 4.31: The measured and observed values of the line current in phase-a of port-A of converter

The simulated system has lots of nodes and equations. For such a complex model, the simulator fails to produce the precise results. Therefore to decrease the system model complexity and to have precise results, the voltage v_n is measured directly instead of using equation 4.41. The reaching time for observed values for capacitor voltage is about $67ms$. In sliding mode, the observed value and measured value of the capacitor voltage are not quite identical. This is because of DC-DC converter and approximation made in observer equations. Simulation result confirms the efficiency of proposed observation method for the complete two-port power converter.

4.8 Summary

In this chapter the sliding mode observers based on the equivalent control method have been applied to the complete two-port power converter. The switching model for the H-bridge converters has been used to design the SMO. The switching model has been extended to the single-phase CHB multilevel converter. The observability of the variables in the single-phase CHB multilevel converter has been examined. Then the SMO equations were derived for the three-phase one-port CHB multilevel converter. The effect of adding the DC-DC converter on observer equations for the back-to-back topology has been explained. Finally SABER simulation results for the two-port power converter have been presented. The simulation results confirm that the selected observer techniques are suitable for this power converter application.

Chapter 5

Experimental Power Converter

5.1. Introduction

In order to experimentally validate the proposed observer, a three-phase three-cell power converter prototype has been constructed. This chapter presents details of the construction and structure of experimental power converter as well as the practical results. First the power converter structure is explained, in details: then the digital and analog control units are explained in detail. Finally the experimental results of the power converter are presented.

5.2. Layout of experimental power converter

As explained in Chapter Four, the port-A voltage equations are enough to construct the observer equations for a two-port power converter. From the observer equation's point of view, port-B is just a load. Therefore to keep the prototype simple, port-B of the power converter is connected to a resistive load. This assumption does not affect the observer

equations. The block diagram and a photograph of the experimental power converter and the digital control unit are shown in figures 5.1 and 5.2 respectively. The prototype has three main units including a power converter unit, voltage and current transducers unit and a digital control unit.

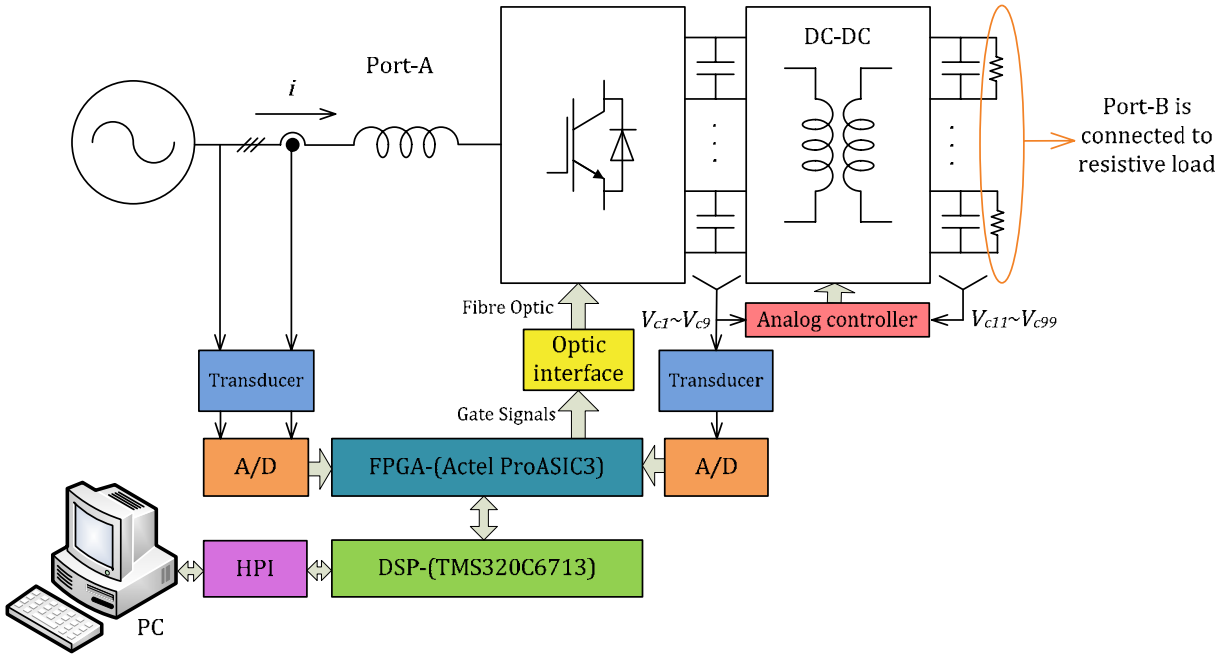


Figure 5.1: Block diagram of complete power converter and digital control unit

As it can be seen in figure 5.1, the dc-link voltages are measured to control the DC-DC converter. The main reason to observe the same voltages is to have redundant information about dc-link voltages to increase system reliability.

The power converter comprises of three 11mH line inductances and nine power modules. Each power module includes an H-bridge, two 1000µF dc-link capacitors and a DC-DC converter. The DC-DC converter is composed of two H-bridge converters across a medium-frequency transformer and an inductor. Each DC-DC converter has its own analog PI controller card. The PI controller is implemented using op-amps and passive elements. The 1200V and 30A Semikron SK30GH123 IGBT module is used for the H-bridge converters. The H-bridge gate drive circuit is equipped with a dead-time circuit to protect the device from short circuits in any H-bridge leg.

The voltage and current transducers measure the three-phase voltages and currents at port-A and nine dc-link voltages. The LEM LV 25-P and LEM LA 55-P transducers are used to measure the voltages and currents respectively.

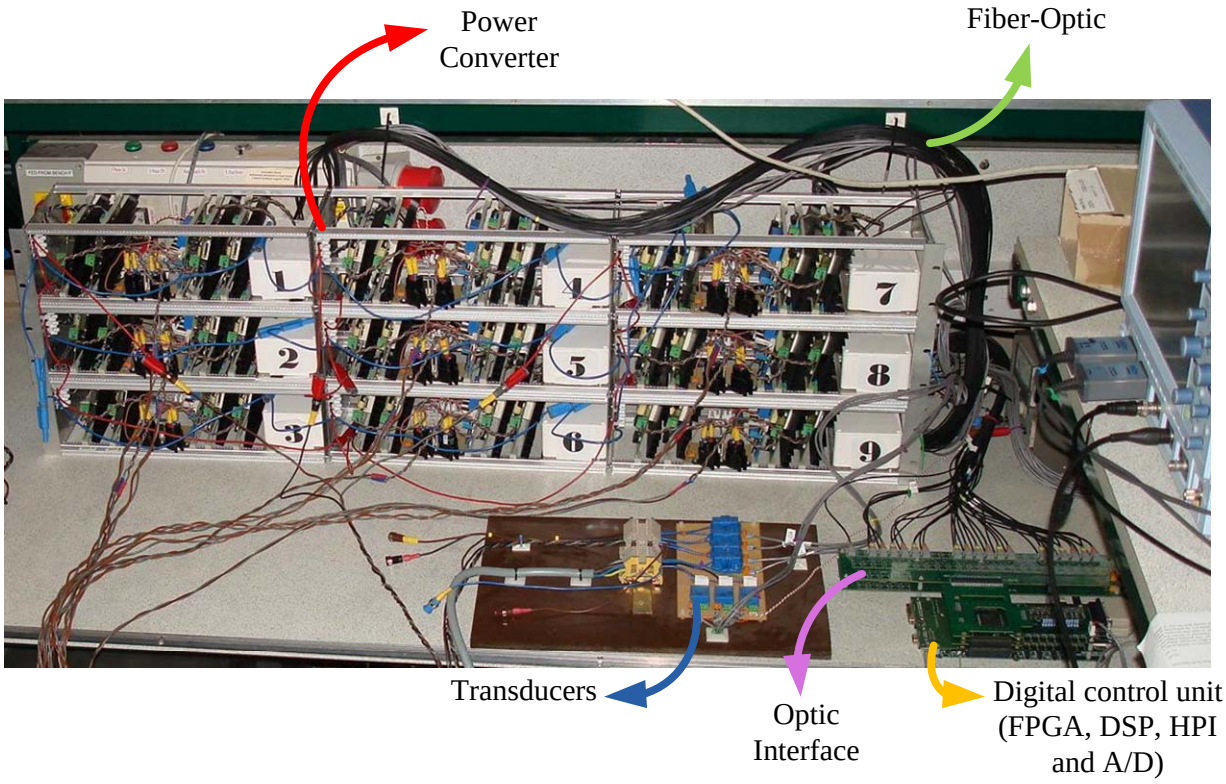


Figure 5.2: The complete power converter and digital control unit

The power flow between the supply and the power converter is controlled digitally. The digital control unit comprises of a high-performance floating-point TMS320C6713 DSP board, two ACTEL ProASIC3 FPGAs, a Host port interface (HPI) daughter card, twenty fourteen-bit A/D converters and a digital to optic interface board. The measured voltages and currents by transducers are transformed to digital values by A/D converters and are transferred to DSP through FPGA. The voltage control loop, current control loop and capacitor voltage balancer equations are written in discrete form in the DSP code. The Tustin method is used to transform the continuous equations to discrete form. The PSCPWM technique is implemented on the FPGA. The sliding mode observer equations are implemented on FPGA in a fixed-point format using the VHDL language. Because of the size of the power converter, there is a large distance between the control unit and the IGBTs. To eliminate noise effects, the gate signals are transformed to optical signals and then sent to

IGBT modules by fiber-optics. The design of the power converter, transducer and digital control unit are explained in detail in the following sections.

5.3. Current and voltage transducers

The LEM LV 25-P and LEM LA 55-P transducers are used to measure the voltages and currents respectively. The LEM LV 25-P is capable of measuring voltages up to 600V and LEM LA 55-P can measure currents up to 70A. The transducers provide galvanic isolation between the power circuit and the control unit. The output of both voltage and current transducers are in the form of current to reduce the noise effect on the measured signals while they are being transmitted to the control unit. The LEM LV 25-P and LEM LA 55-P transducer schematics are shown in figures 5.3 and 5.4 respectively.

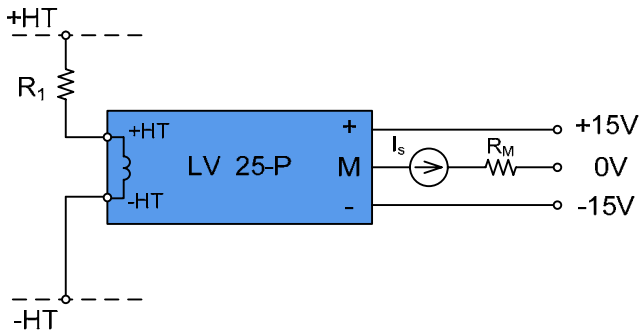


Figure 5.3: The LEM LV 25-P voltage transducer schematic.

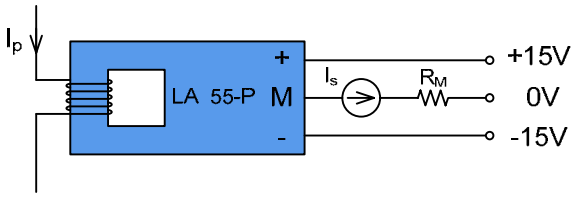


Figure 5.4: The LEM LA 55-P current transducer schematic.

In figure 5.3 the value of R_1 depends on the maximum measured voltage across +HT and –HT. The nominal value of the current flowing through resistor R_1, I_p, is $10mA$. The conversion ratio between the primary and secondary current for the LEM LV 25-P is:

$$\frac{I_s}{I_p} = 2.5 \tag{5.1}$$

The overall accuracy of transducer is around $\pm 0.9\,\%$ at $25°C$. For the current transducer, LEM LA 55-P, the number of turns at the primary side depends on the magnitude of the current to be measured. The nominal primary current for current transducer is 50A. To measure a current of 5A, the transducer needs to have 10 turns on the primary winding. The conversion ratio between the primary and secondary currents for the LEM LA 55-P is:

$$\frac{I_s}{I_p} = 0.001 \tag{5.2}$$

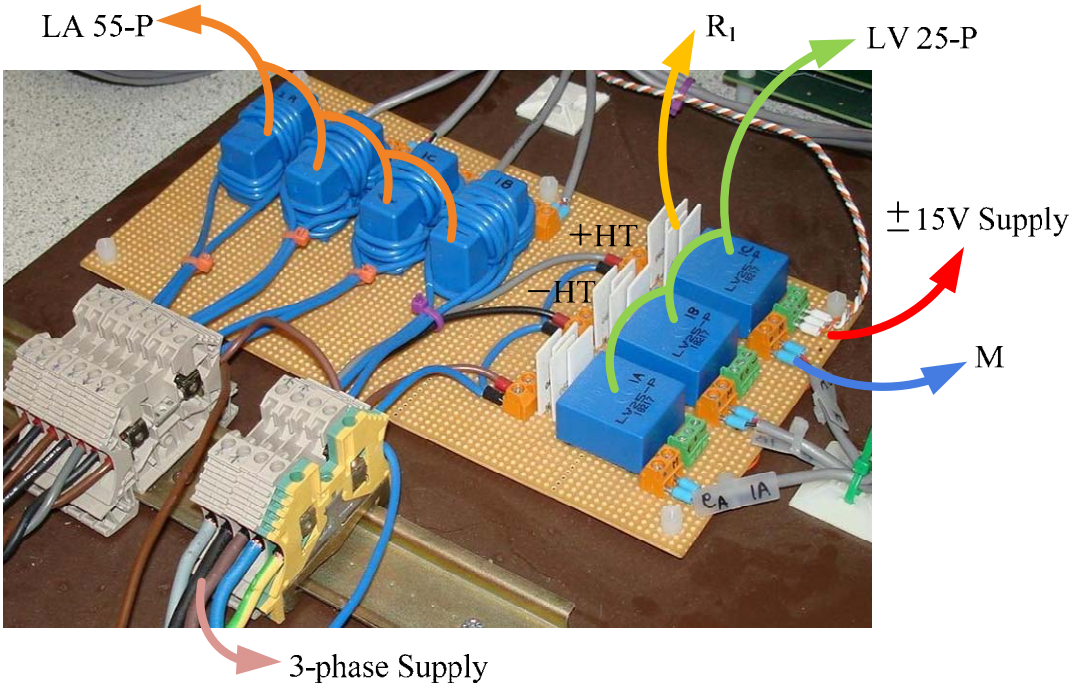


Figure 5.5: The measurement unit with voltage and current transducers

The measuring resistance R_M (burden resistor) is placed on the FPGA board. The measuring resistor value depends on the transducers secondary current and the maximum allowable voltage at the A/D inputs. The complete measurement unit including the current and voltage transducers is shown in figure 5.5.

5.4. Power converter module

Each power module comprises of an H-bridge rectifier at port-A, two dc-link capacitors, a DC-DC converter and a resistive load. The block diagram, circuit diagram and photograph of a power converter module are shown in figures 5.6 and 5.7. The H-bridge at port-A act as controlled ac-to-dc rectifier. The DC-DC converter equalizes the two dc-link voltages at its terminals. Its main role is to provide galvanic isolation between port-A and the load. The DC-DC converter includes two H-bridge converters, one medium frequency transformer, one inductor and an analog controller card. The basic operation principle of a DC-DC converter was explained in chapter-2.

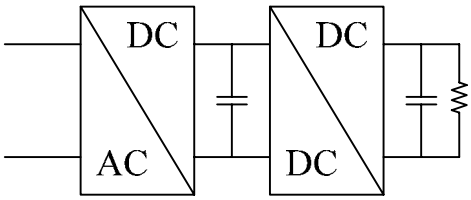


Figure 5.6(a): Block diagram of a power converter module

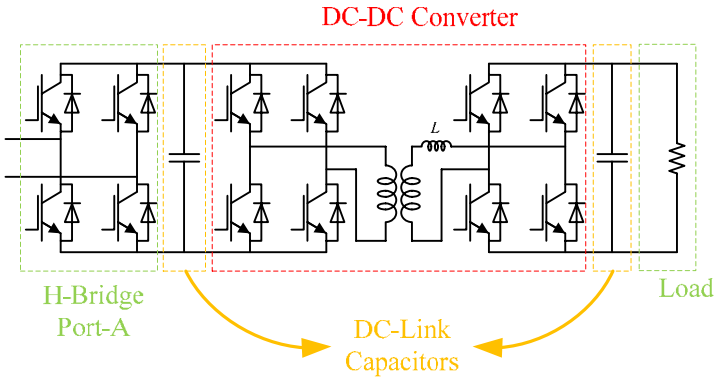


Figure 5.6(b): Circuit diagram of a power converter module

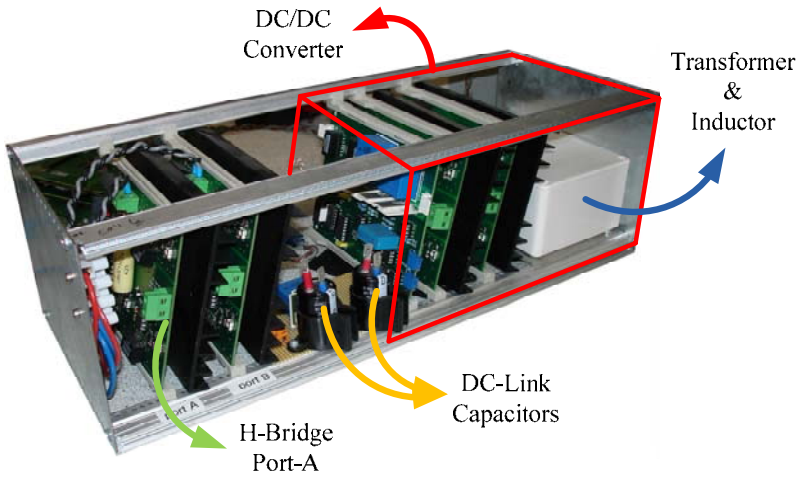


Figure 5.7: Power converter module

The DC-DC converter uses a switching frequency of 5 kHz. The circuit diagram of the DC-DC converter and the control scheme is shown in figure 5.8. The main controller units are the measurement section, PI regulator section, 10 kHz saw-tooth waveform generator, two comparators and two negative-edge-triggered JK flip-flops.

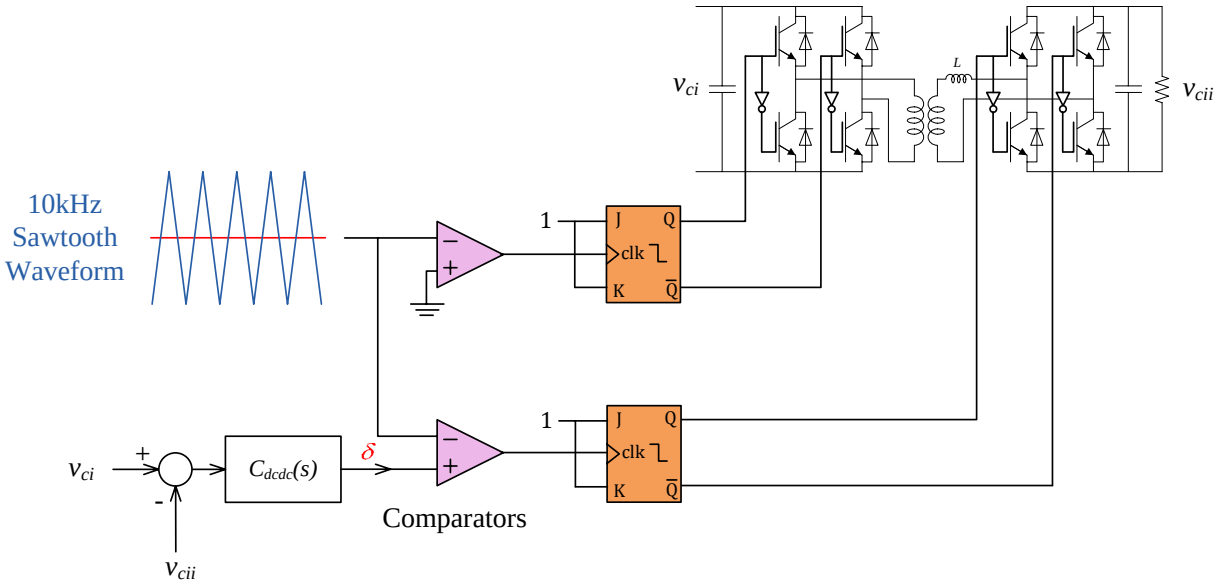


Figure 5.8: The circuit diagram for the DC-DC converter and controller.

Where v_{ci} and v_{cii} are the primary and secondary dc-link voltages across DC-DC converter.

A square wave generator circuit is used to generate a 10 kHz saw-tooth waveform, as shown in figure 5.9. Having an ideal op-amp with infinite slew rate, the output of the circuit in figure 5.9 would be a square wave but using a non-ideal LM741 op-amp with a limited slew rate of 0.5 $V/\mu s$, results a saw-tooth waveform at the output of the square wave generator circuit.

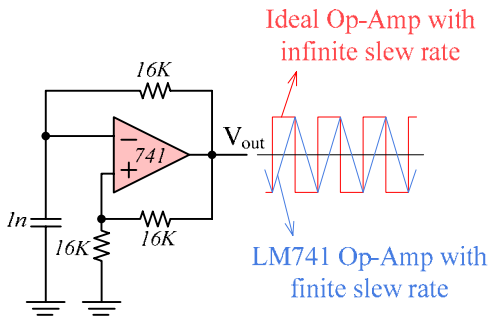


Figure 5.9: The saw-tooth waveform generator circuit.

The PI regulator is implemented using LM741 op-amps and passive elements. The practical PI regulator circuit is shown in figure 5.10. The relationship between the inputs and the output voltages of the PI controller in figure 5.10 is:

$$v_o(t) = \left(K_p + \frac{K_I}{S}\right)\left(v_{c1}(t) - v_{c11}(t)\right) \tag{5.3}$$

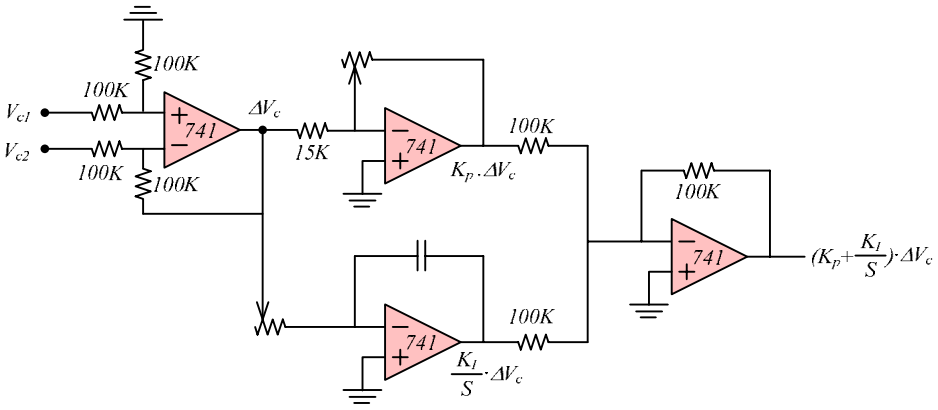


Figure 5.10: The practical PI regulator implementation.

The proposed controller is capable of bi-directional power flow control. The PI-regulator controls the phase shift between ac voltages across the transformer and the inductor. The DC-DC controller card is shown in figure 5.11.

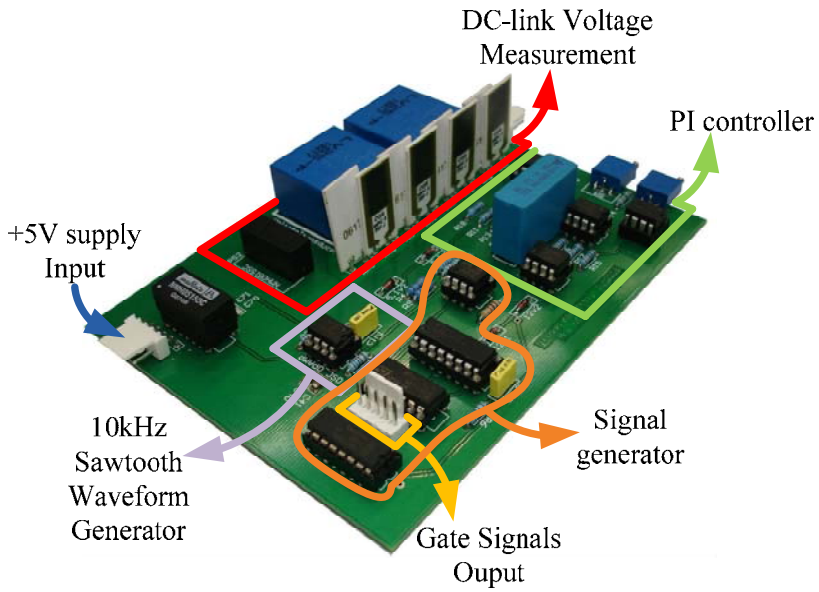


Figure 5.11: The DC-DC converter control card.

The leakage inductance of the transformer is not big enough to provide all the required inductance so an additional inductor is added in series with the transformer. An ETD59 ferrite core is used to build the medium-frequency transformer and inductor. The ETD59 ferrite core and the associated dynamic magnetization curve are shown in figures 5.12 and 5.13 respectively.

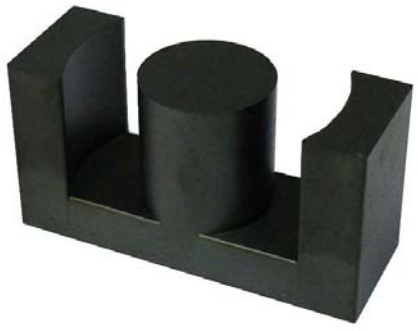


Figure 5.12: The ETD59 ferrite core.

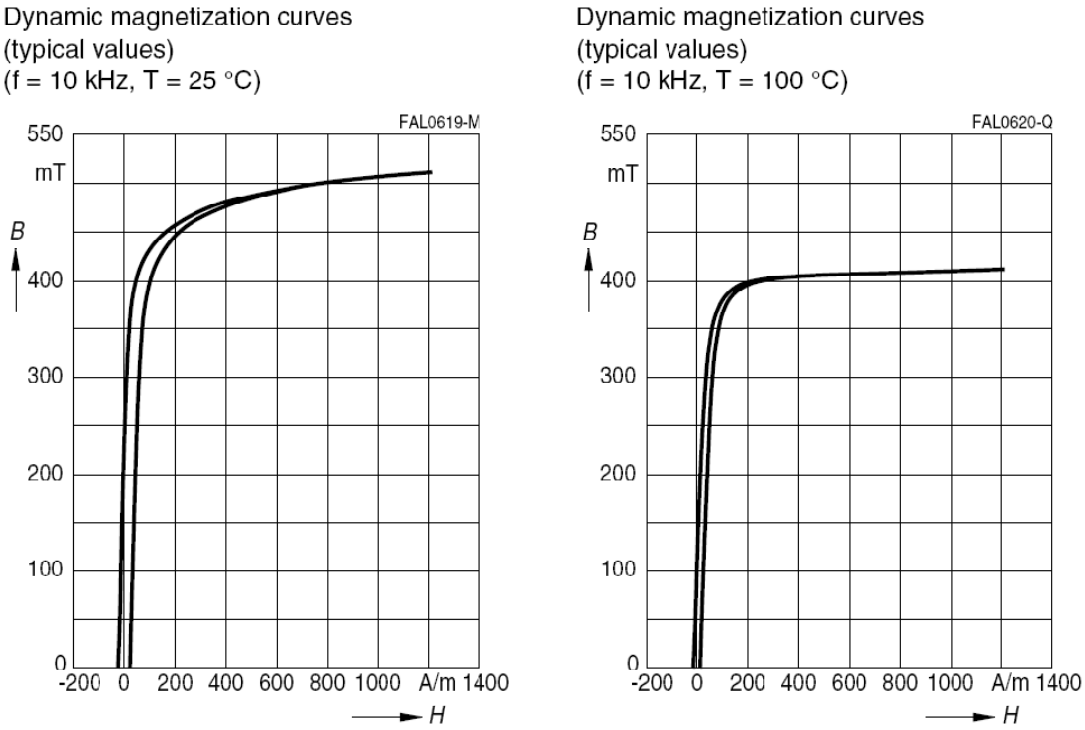


Figure 5.13: The ETD59 ferrite core dynamic magnetization curve.

According to figure 5.13 the maximum magnetic flux density, B_{max}, to avoid magnetic saturation should be less than $350mT$ and is set to $B = 200mT$. The *RMS* value of the applied voltage to the transformer is $V_{rms} = 100V$ with a frequency of $f = 5kHz$. The cross section area of the ETD59 ferrite core is $A_e = 368mm^2$. According to these design requirements the transformer windings number of turns can be calculated using equation 5.4.

$$N = \frac{V_{rms}}{4.44 \times f A_e B} = \frac{100}{4.44 \times 5000 \times (368 \times 10^{-6}) \times (200 \times 10^{-3})} = 62 \qquad (5.4)$$

The size of wire used for the transformer winding is 16 SWG, with a current rating of 2.74 A and a diameter of $1.5mm$. The skin depth for a copper wire carrying a current of 5 kHz at $100^{\circ}C$ and $25^{\circ}C$ are:

$$\delta_{100^{\circ}C} = \sqrt{\frac{2(\rho_{cu})_{100^{\circ}C}}{\omega \mu_r \mu_0}} = \sqrt{\frac{2 \times (23 \times 10^{-9})}{(2\pi \times 5000) \times (4\pi \times 10^{-7})}} = 1.079mm \qquad (5.5)$$

$$\delta_{25^{\circ}C} = \sqrt{\frac{2(\rho_{cu})_{25^{\circ}C}}{\omega\mu_r\mu_0}} = \sqrt{\frac{2 \times (17.3 \times 10^{-9})}{(2\pi \times 5000) \times (4\pi \times 10^{-7})}} = 0.936mm \quad (5.6)$$

Where ρ_{cu} is the resistivity of copper, ω is the angular frequency of current and $\mu_r\mu_0$ is the permeability of the copper. The skin depth is bigger than wire radius, which means that the selected wire diameter is suitable and there is no need to use litz wire.

Practical results from the DC-DC converter capacitor voltages are shown in figures 5.14 and 5.15. The steady state results in figure 5.14 confirm the correct operation of designed converter and controller. The response of DC-DC converter to a step change is shown in figure 5.15. Figure 5.15 confirms the good voltage tracking of DC-DC converter under step change condition.

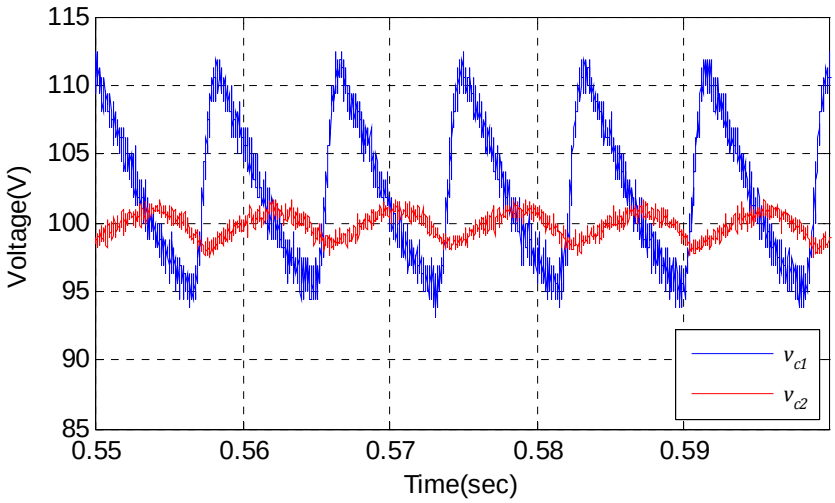


Figure 5.14: The DC-DC converter practical results in steady-state.

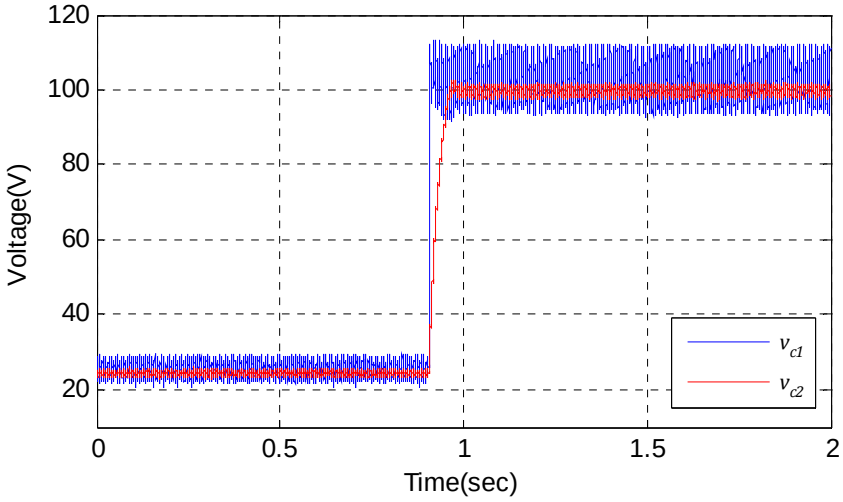


Figure 5.15: The DC-DC converter practical results for step-change condition.

The H-bridge converter uses a Semikron SK30GH123 H-bridge module with four IGBTs, diodes and the associated gate drive circuits. Each IGBT is rated at 1200V, 30A and is capable of switching at frequencies up to 20 KHz. The H-bridge converter is shown in figure 5.16.

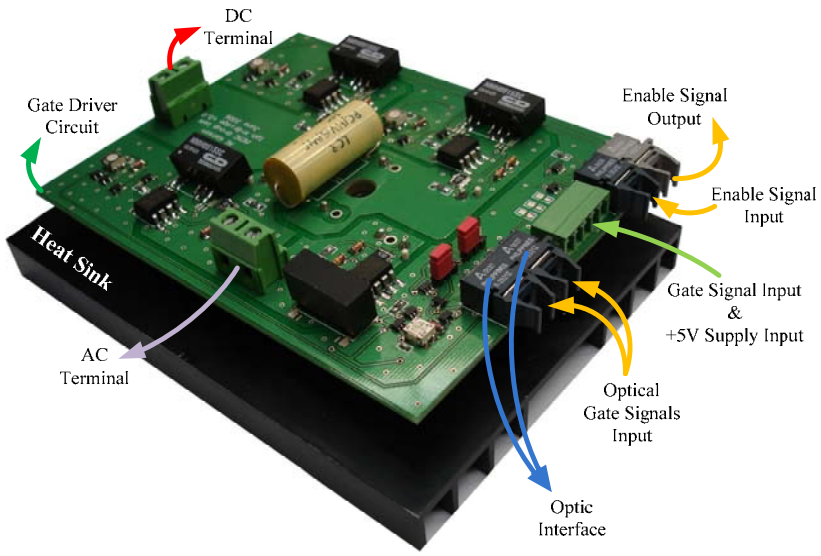


Figure 5.16: The H-bridge converter.

The Semikron SK30GH123 H-bridge module is shown in figure 5.17.

Figure 5.17: The Semikron SK30GH123 H-bridge module.

The simplified circuit diagram of a IGBT gate drive circuit is shown in figure 5.18. An *NMH0515SC* DC-DC converter rated at two watts is used to produce galvanic isolation between the +5V supply and IGBT gate drive. An HCPL-3102 IGBT gate drive optocoupler is used to produce galvanic isolation between gate signal and IGBT. The IGBT's gate is protected against overvoltage using two zener diodes. The diagram is presented in different colors to show the galvanic isolation between different parts of the circuit.

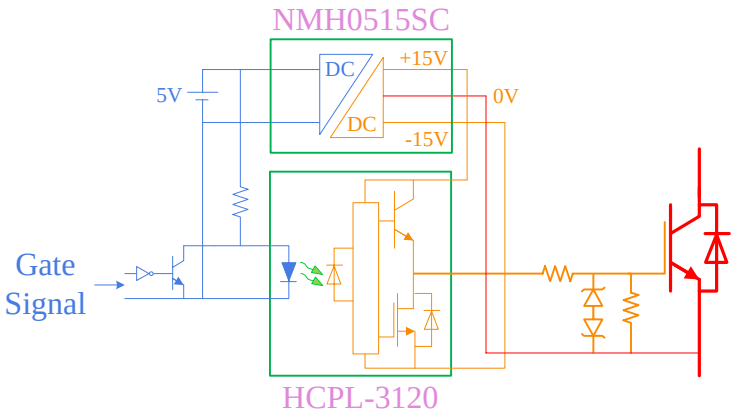


Figure 5.18: The simplified circuit diagram of the IGBT gate driver.

The H-bridge gate drive circuit is able to receive both electrical and optical gate signals. A HFBR-2521Z optical receiver by Avago Technologies receives the optical signals.

5.5. The digital control unit

The power flow control is implemented using a digital control unit. The digital control unit comprises of a high-performance floating-point TMS320C6713 DSP board, two ACTEL ProASIC3 FPGA cards with A/D converters (designed at the PEMC group at the University of Nottingham), a Host port interface (HPI) daughter card and a digital to optic interface board.

The voltage control loop, current control loop and capacitor voltage balancer equations are implemented on the DSP in discrete form. The DSP is programmed by C language. The Texas Instrument TMS320C6713 DSP operates at 225MHz. The DSP operations are performed using thirty two-bits floating point numbers. The digital equation time-step is set to 100µs with a 10KHz interrupt signal. The interrupt signal is generated by the FPGA unit. The TMS320C6713 DSP contains eight independent functional units including two fixed-point ALUs, four floating and fixed point ALUs and two floating and fixed point multipliers. The DSP communicates with the FPGA through a thirty two-bit External Memory Interface (EMIF). Also there is a sixteen-bit Host Port Interface (HPI) on a DSP to communicate with the host PC. The digital control platform is shown in figure 5.19 and a block diagram of DSP / FPGA structure is shown in figure 5.20.

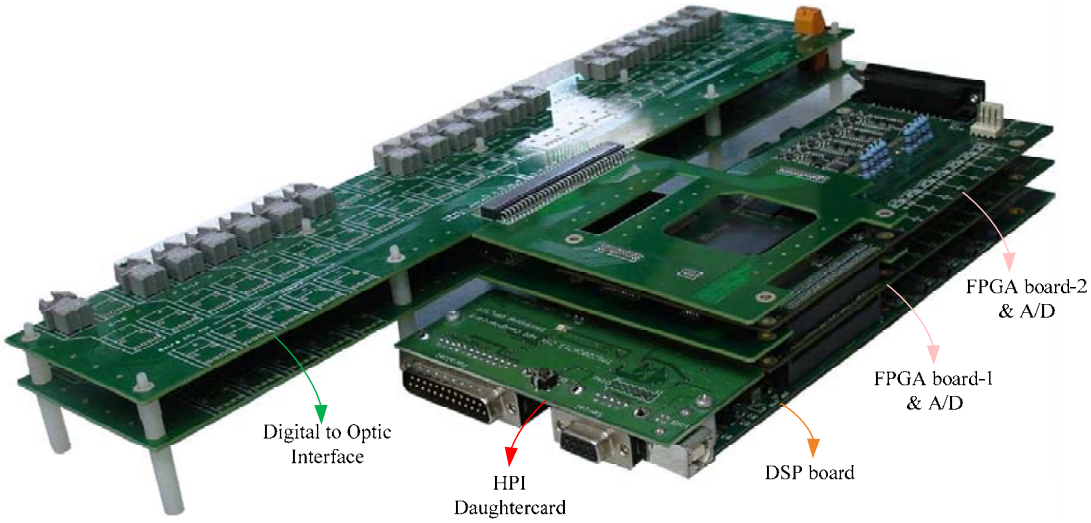


Figure 5.19: Digital control platform

The FPGA card is used as an interface between the DSP and the power converter. All measurements made by the transducers are converted to digital values using fourteen-bit A/Ds and transferred to DSP through FPGA. There are ten high-speed A/Ds on each FPGA card. An ACTEL ProASIC3 A3P1000 FPGA is used in this prototype. The A3P1000 FPGA contains 1,000,000 system gates or 24,576 D type flip-flops. The DSP communicates with the FPGA through a thirty two-bits data bus and a seven-bit address bus. The main units implemented on the FPGA are:

- Carrier generating unit for PWM
- Phase Shifted Cascaded PWM (PSCPWM) unit
- Fault Trip unit
- Watchdog timer
- Interrupt signal generator
- Multiplexer
- DSP memory interface
- Sliding mode observer unit

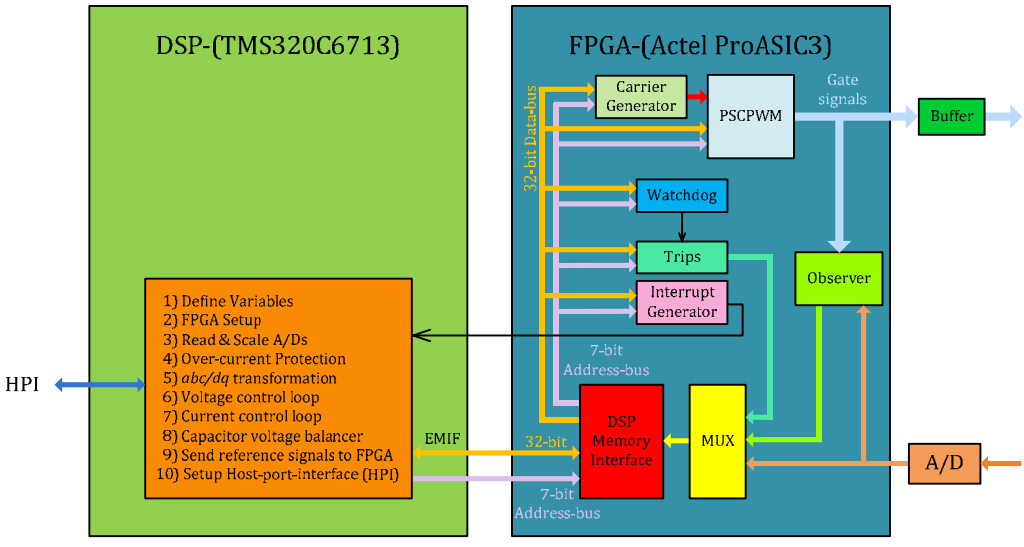


Figure 5.20: The block diagram of the DSP and the FPGA structure.

The carrier generator unit generates three triangle waveforms which are phase shifted by $\pi/3$ radians. Three sixteen-bit counters together with sequential logic circuits are used to generate

the triangle carrier signals. The sixteen-bit comparator and D flip-flops are used to generate the gate signals. The block diagram of the carrier signal generator is shown in figure 5.21

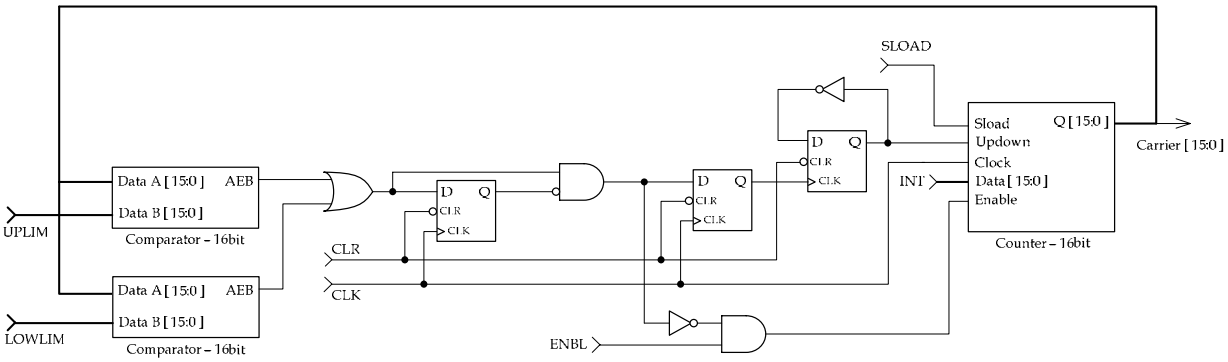


Figure 5.21: The block diagram of the carrier signal generator.

There are three carrier generator units in the FPGA, operating with a 10MHz clock signal. The value of "INT" input is different for each unit. The output of the carrier generator units are shown in figure 5.22.

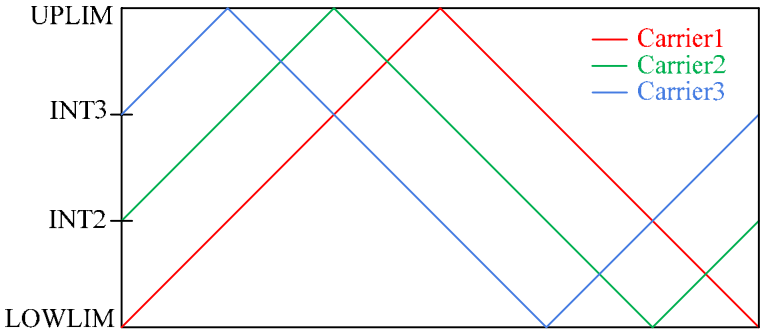


Figure 5.22: The block diagram of the carrier signal generator.

The values of $UPLIM$, $LOWLIM$, $INT1$, $INT2$ and $INT3$ are defined as:

$$UPLIM = \frac{f_{clk}}{2f_c}, \quad LOWLIM = 0 \tag{5.7}$$

$$INT3 = \frac{2}{3}UPLIM, \quad INT2 = \frac{1}{3}UPLIM, \quad INT1 = 0 \tag{5.8}$$

Where f_{clk} is the frequency of clock signal, which is 10MHz, and f_c is the frequency of carrier signal, which is set to 400Hz in this work.

The watchdog timer ensures that the DSP communicates well with the FPGA. If this communication is lost for any reason, the watchdog timer sends a signal to the trip unit and the trip unit trips the converter operation. The interrupt generator unit comprises a thirty two-bit counter and a sequential logic circuit that generates a 10 KHz pulse. This interrupt signal is sent to the DSP. The interrupt service routine operates by interrupt signal frequency. The outputs of the trip unit, sliding mode observer unit and A/D unit are connected to the DSP memory interface unit through thirty two-bit multiplexers. The DSP memory interface unit is connected directly to the FPGA pins. All data from the DSP to the FPGA and vice versa are transferred through the DSP memory interface unit. A photograph of the FPGA card is shown in figure 5.23.

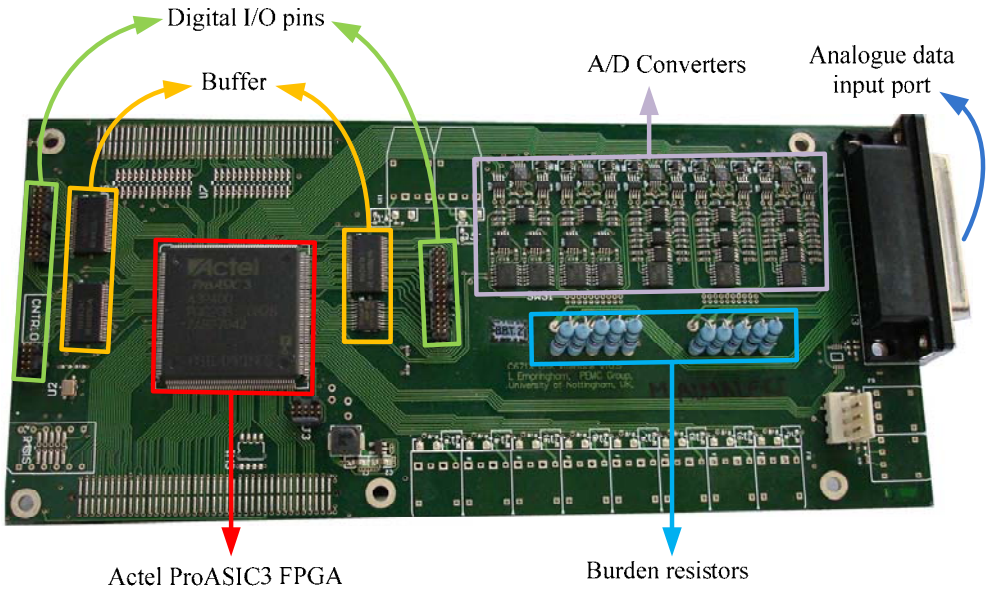


Figure 5.23: FPGA card (ACTEL ProASIC3 FPGA and A/D converters).

The FPGA card is stackable. Several FPGA cards can be stacked and connected to a single DSP. The FPGA card consists of an Actel FPGA, digital input and output ports, A/D converters and analog data input port, which is connected to the transducers outputs. The

output signals from the transducers are in current form, therefore the burden resistors on the FPGA board in order to transforming the current signals to voltage signals.

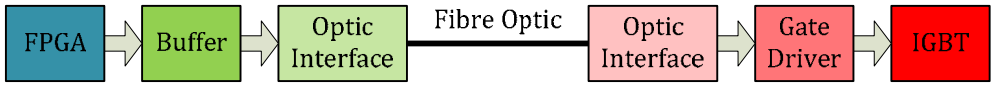


Figure 5.24 A block diagram of the gate signal path.

The gate signals generated by the PSCPWM in the FPGA are sent to an optical interface through the buffer unit. Figure 5.24 shows a block diagram of the gate signal path from the FPGA to the IGBT module. AVAGO HFBR-1521Z transmitters are used to convert the electrical gate drive signals to optical signals (the optic interface).

5.6. The Tustin method

The Tustin method is used to transform the voltage, current and capacitor voltage balancer equations to discrete form. The Tustin method is more precise than the Euler approximation method. In order to calculate an estimation of a function $f(t)$ at $t = (K+1)T_s$ by knowing its value at $t = KT_s$ and having the time derivative of function $f(t)$:

$$\frac{df(t)}{dt} = m(t) \tag{5.9}$$

The slope of $f(t)$ at $t = KT_s$ and $= (K+1)T_s$, which are $(\tan\alpha)$ and $(\tan\beta)$, are needed. An estimation of function $f(t)$ at $t = (K+1)T_s$ by using Tustin method is:

$$f[K+1] = f[K] + T_s.\tan\gamma \tag{5.10}$$

Where:

$$\tan\gamma = \frac{(\tan\alpha + \tan\beta)}{2}, \quad \tan\alpha = m[K], \quad \tan\beta = m[K+1] \tag{5.11}$$

Point “a” at figure 5.25 shows the estimation of function $f(t)$ at $t = (1 + K)T_s$ using the Euler approximation method, point “b” shows the estimation of $f(t)$ using the Tustin method and point “c” shows the real value of $f(t)$. It can be seen that Tustin method is more precise.

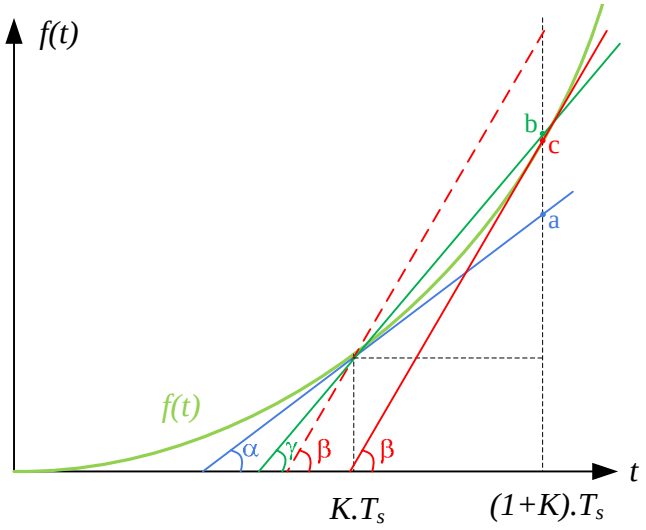


Figure 5.25: The graph demonstrating Tustin method.

The transformation of a PI controller to discrete form using the Tustin method is explained below. Consider a PI controller block:

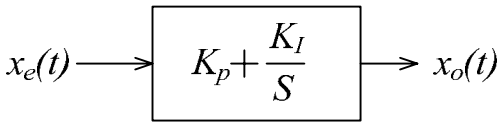


Figure 5.26: The PI controller block.

The PI controller equation is:

$$x_o(t) = \left(K_p + \frac{K_I}{S}\right)x_e(t) \Rightarrow \frac{d}{dt}\left(x_o(t) - K_p x_e(t)\right) = K_I x_e(t) \tag{5.12}$$

The discrete form of equation 5.12 using Tustin method is:

$$x_o[k+1] - K_p x_e[k+1] = x_o[k] - K_p x_e[k] + T_s\left(\frac{K_I x_e[k] + K_I x_e[k+1]}{2}\right) \tag{5.13}$$

Further simplification of equation 5.13 results:

$$x_o[k+1] = x_o[k] + \left(K_p + \frac{T_s K_I}{2}\right) x_e[k+1] - \left(K_p - \frac{T_s K_I}{2}\right) x_e[k] \tag{5.14}$$

Equation 5.14 has been used to transform all the PI controllers to discrete form in this work.

5.7. Practical results

The block diagram of the experimental power converter is shown in figure 5.27. The power converter is connected to a balanced three-phase supply. The line inductance is 11mH, the dc-link capacitance is 1000μF and the load resistances are 59Ω. The dc-link voltages are set to 45V and peak line current is 3A. The experimental converter voltage and current waveforms, as well as the dc-link voltages, are shown in figures 5.29 to 5.33 respectively.

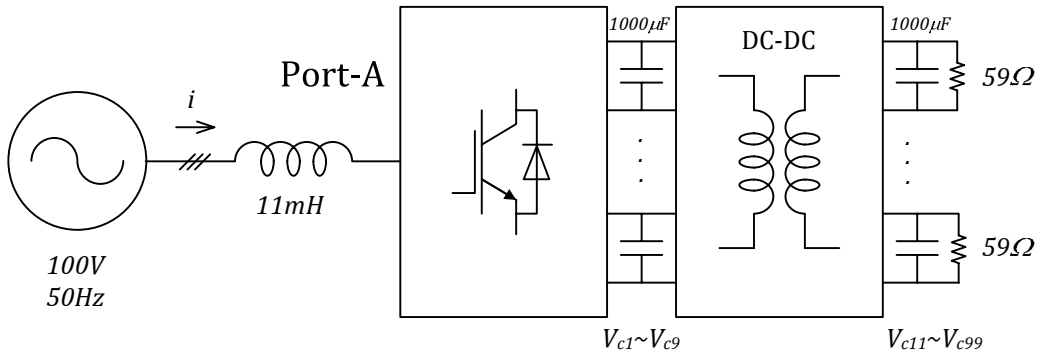


Figure 5.27 The block diagram of the experimental power converter.

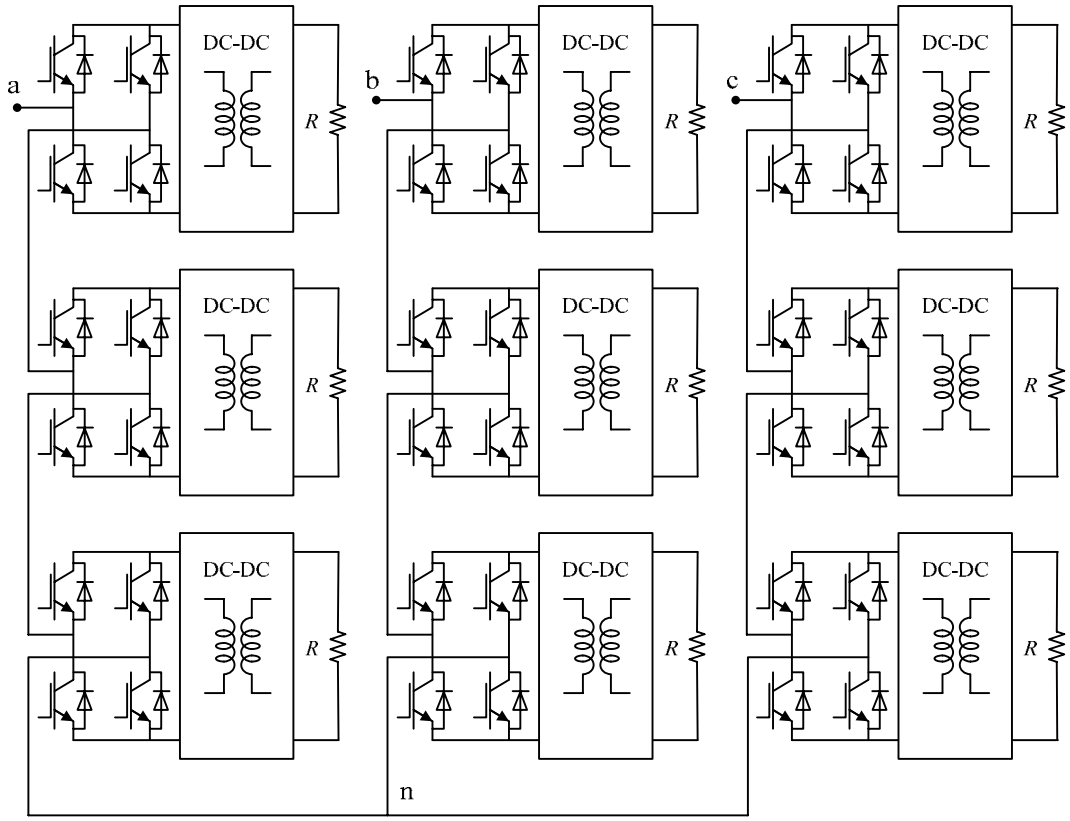


Figure 5.28 The experimental power converter topology.

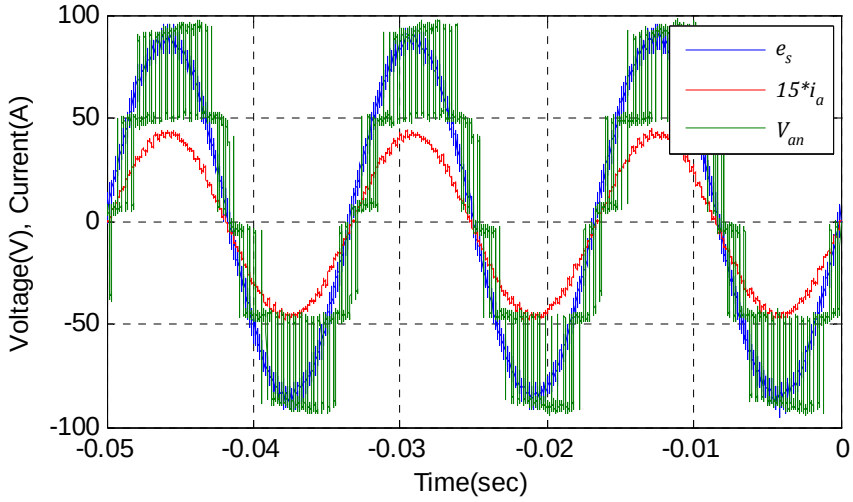


Figure 5.29 Phase-a supply voltage, converter voltage and line current.

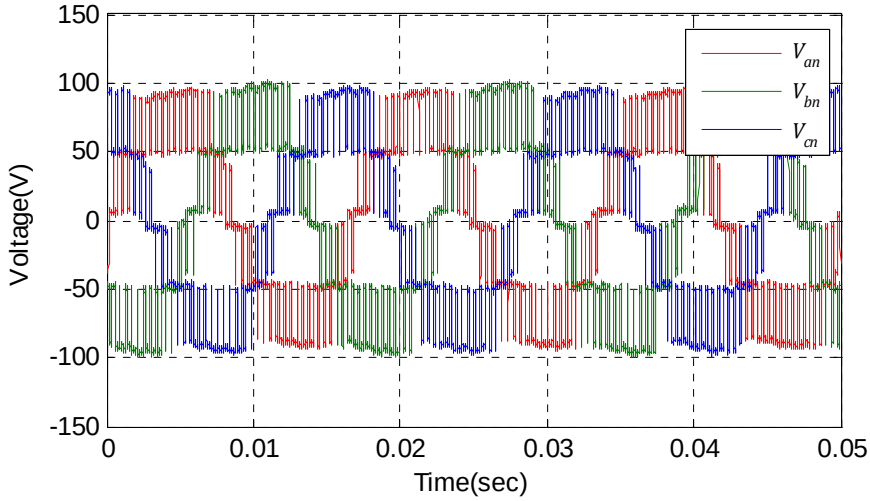


Figure 5.30 The three-phase converter voltages.

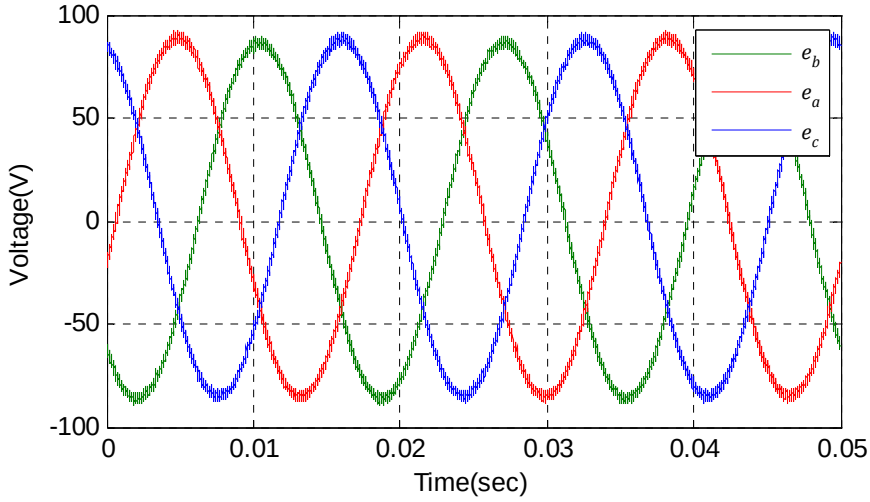


Figure 5.31 The three-phase supply voltages.

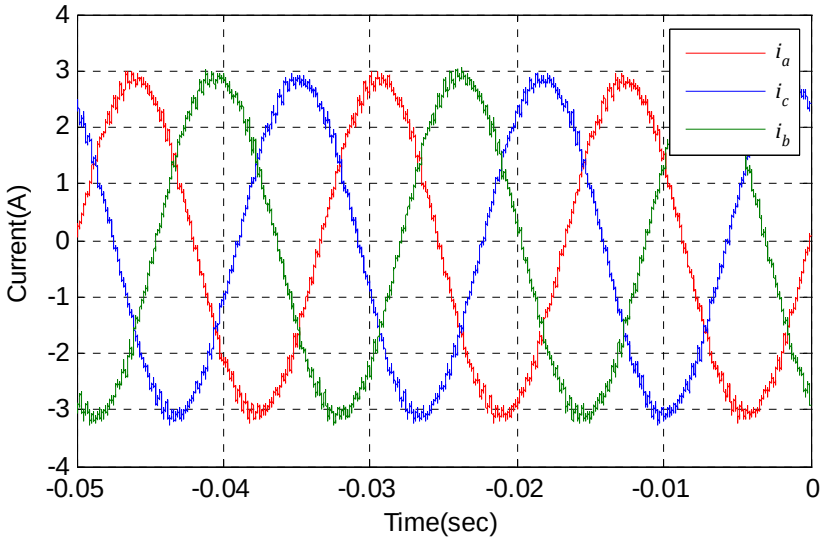


Figure 5.32 The three-phase line currents.

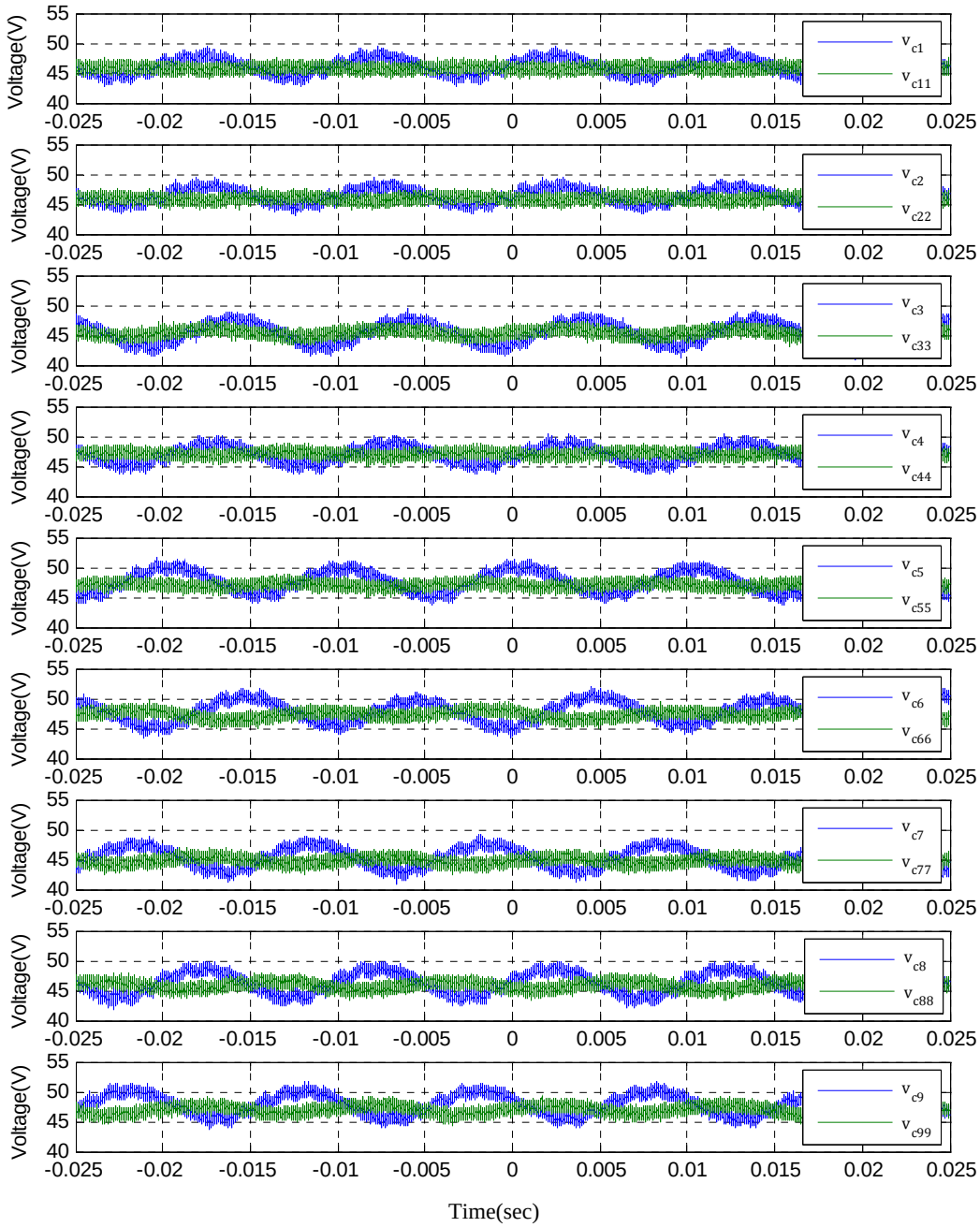


Figure 5.33: The dc-link voltages at DC-DC converter terminals.

The reference value for reactive power is set to zero. Figure 5.29 shows that the phase-a supply voltage and line current are in phase, which confirms the unity power operation condition. As figure 5.33 shows, the dc-link voltages across the DC-DC converter are equal and this confirms the correct operation of the DC-DC converters.

5.8. Summary

The design and structure of the experimental power converter has been described in this chapter. The one port power converter with a DC-DC converter is constructed to validate the proposed sliding mode observer. The design of an analog DC-DC controller card is described. The practical results confirm the correct design of the converter and associated control.

Chapter 6

Sliding Mode Observer-Practical Implementation

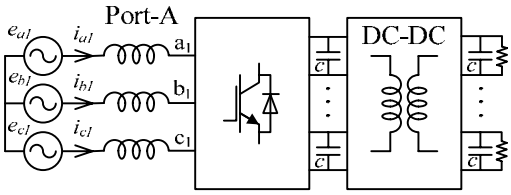
6.1 Introduction

This chapter presents the practical implementation of a sliding mode observer on an FPGA control platform. The sliding mode observer is implemented on FPGA in fixed-point system using VHDL programming language. First the observer equations are transformed to discrete form. Then the observer equations are implemented in fixed-point system on FPGA. Because of limited number of gates in FPGA, to be able to fit the observer equations on FPGA, they are simplified as much as possible. Because of FPGA gate limitation, only observer equations of v_{c1} and i_a are implemented.

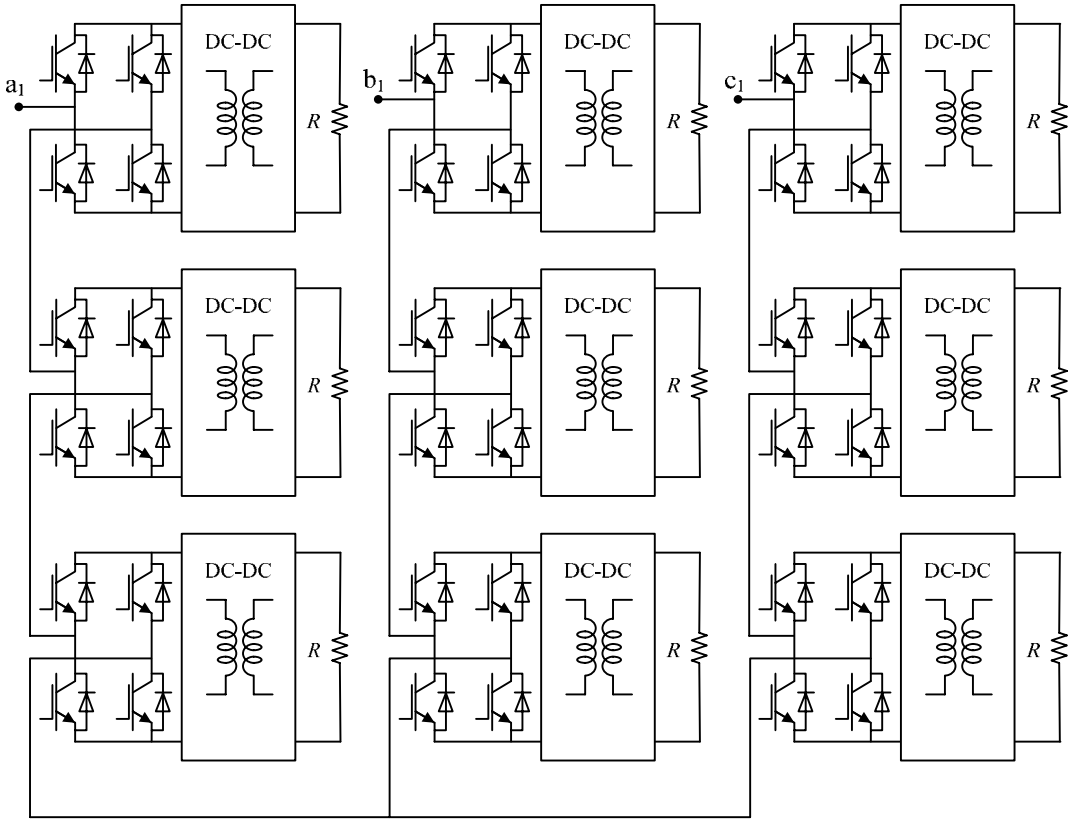
6.2 Observer equations for experimental power converter

The sliding mode observer equations for the three-phase, three-cell ideal power converter were derived in chapter 4. In an ideal power converter all the IGBT switches are assumed to

be ideal. However the IGBTs used in experimental power converter are not ideal switches. There is a voltage drop across a real IGBT during conduction. The voltage drop across IGBTs should be considered in the observer equations otherwise there will be an error in any observed values. The diagram and topology of the experimental power converter is shown in figure 6.1.



(a): The experimental power converter

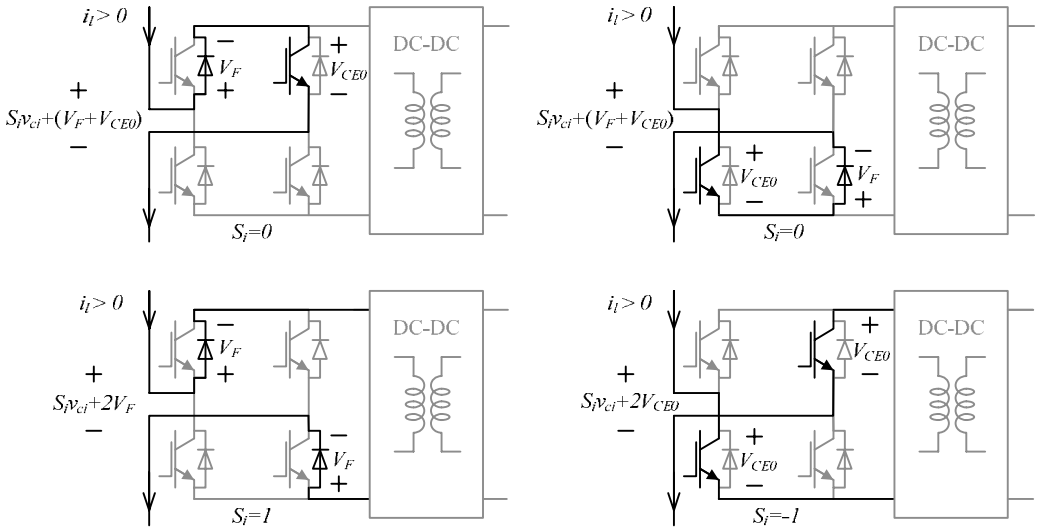


(b): Topology of the experimental power converter

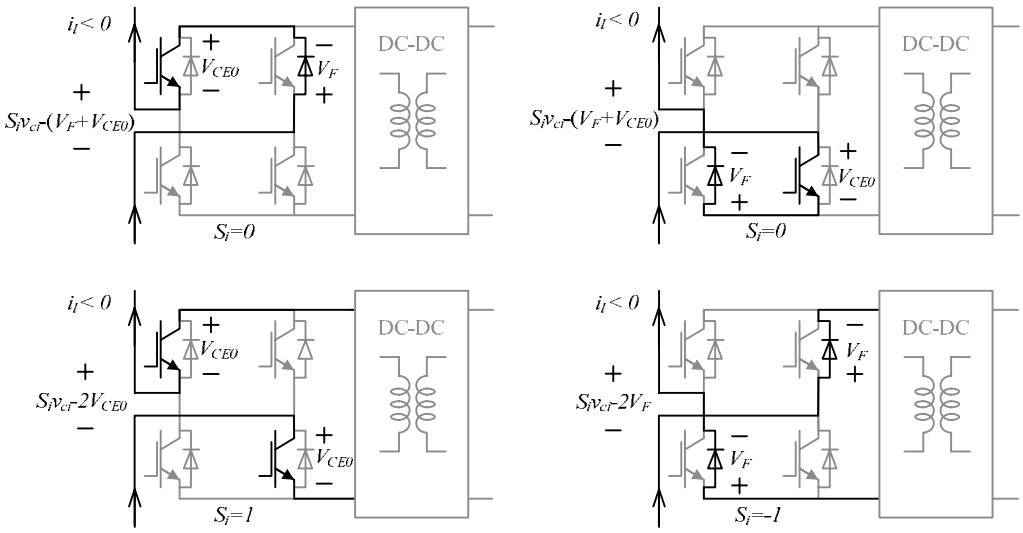
Figure 6.1: Experimental power converter

To consider the effect of non-ideal switches on observer equations, all possible states of the switches within an H-bridge are shown in figure 6.2. The voltage drops across the inverse

diode, V_F, and across the IGBT, V_{CE0}, during conduction mode are functions of conducted current. To keep the observer equations as simple as possible, both V_F and V_{CE0} are assumed to be constant and equal to $1V$. Based on this assumption and with reference to figure 6.2 the output voltage at ac-side of the H-bridge for positive values of line current is $(S_i v_{ci} + 2)$ and for negative values of line current is $(S_i v_{ci} - 2)$.



(a): Current path for positive line current



(b): Current path for negative line current

Figure 6.2: H-bridge switch status

Therefore the voltage at ac-side of H-bridge converter is:

$$S_i v_{ci} + 2sgn(i_l) \tag{6.1}$$

Figure 6.3 presents the switching model of the experimental power converter.

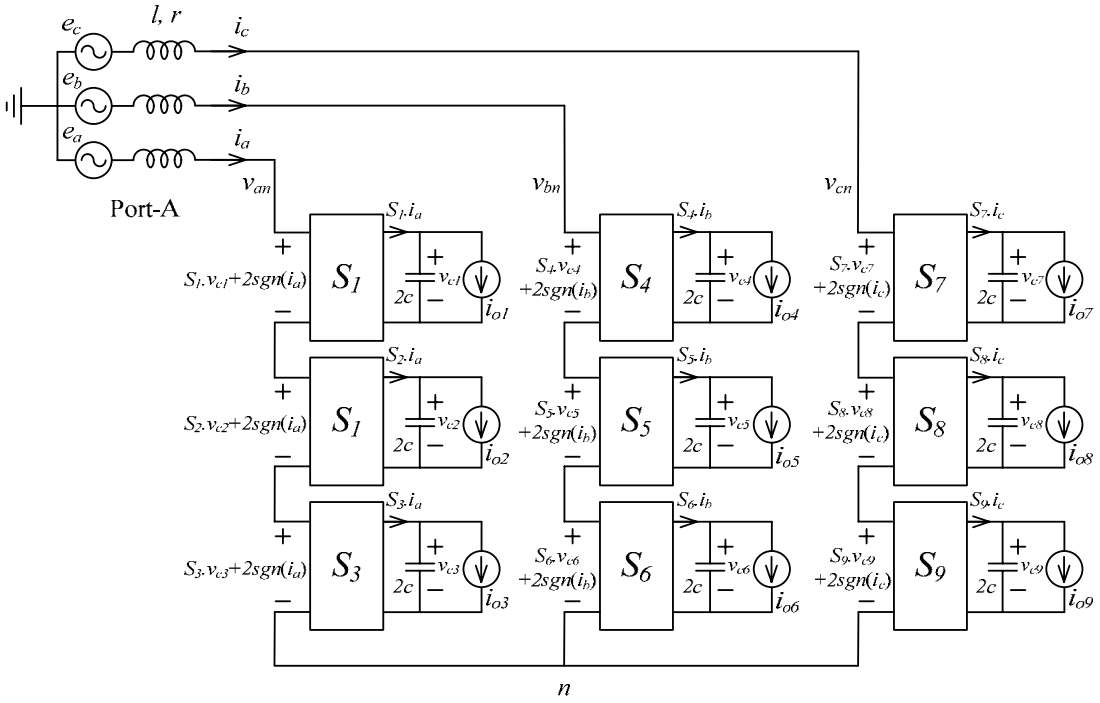


Figure 6.3: Switching model of the power converter

The three-phase voltage equations are:

$$\begin{cases} e_a = (r + l\,s)i_a + \sum_{i=1}^{3} S_i v_{ci} + 6sgn(i_a) + v_n \\ e_b = (r + l\,s)i_b + \sum_{i=4}^{6} S_i v_{ci} + 6sgn(i_b) + v_n \\ e_c = (r + l\,s)i_c + \sum_{i=7}^{9} S_i v_{ci} + 6sgn(i_c) + v_n \end{cases} \tag{6.2}$$

In a balanced three-phase system v_n can be derived from equation 6.2:

$$v_n = -\frac{1}{3}\sum_{i=1}^{9} S_i v_{ci} - 2sgn(i_a) - 2sgn(i_b) - 2sgn(i_c) \tag{6.3}$$

The phase-*a* equations in state-space form are presented in equation 6.4.

$$\begin{cases} \frac{d}{dt} i_a = -\frac{1}{l}\left(r i_a + \sum_{i=1}^{3} S_i v_{ci} + 6sgn(i_a) - e_a + v_n \right) \\ \frac{d}{dt} v_{c1} = \frac{1}{2c}(S_1 . i_a - i_{o1}) \\ \frac{d}{dt} v_{c2} = \frac{1}{2c}(S_2 . i_a - i_{o2}) \\ \frac{d}{dt} v_{c3} = \frac{1}{2c}(S_3 . i_a - i_{o3}) \end{cases} \tag{6.4}$$

The corresponding sliding mode observer equations for v_{c1} and i_a in phase-*a* are presented by equations 6.5 and 6.6.

During ($S_1 = \pm 1$ and $S_2 = 0$ and $S_3 = 0$) the observer equation is:

$$\begin{cases} \frac{d}{dt} \hat{\imath}_a = -\frac{1}{l}\left(r \hat{\imath}_a + \sum_{i=1}^{3} S_i \hat{v}_{ci} + 6sgn(i_a) - e_a + \hat{v}_n \right) - L_1 sat(\hat{\imath}_a - i_a) \\ \frac{d}{dt} \hat{v}_{c1} = \frac{1}{2c}(S_1 . \hat{\imath}_a - i_{o1}) - L_2 sat\left(-l S_1 L_1 sat(\hat{\imath}_a - i_a)\right) \end{cases} \tag{6.5}$$

For all the other modes:

$$\begin{cases} \frac{d}{dt} \hat{\imath}_a = -\frac{1}{l}\left(r \hat{\imath}_a + \sum_{i=1}^{3} S_i \hat{v}_{ci} + 6sgn(i_a) - e_a + \hat{v}_n \right) - L_1 sat(\hat{\imath}_a - i_a) \\ \frac{d}{dt} \hat{v}_{c1} = \frac{1}{2c}(S_1 . \hat{\imath}_a - i_{o1}) \end{cases} \tag{6.6}$$

Where $\hat{v}_{c1}$ and $\hat{\imath}_a$ are the observed values of v_{c1} and i_a and $\hat{v}_n$ is:

$$\hat{v}_n = -\frac{1}{3}\sum_{i=1}^{9} S_i \hat{v}_{ci} - (2sgn(i_a) + 2sgn(i_b) + 2sgn(i_c)) \tag{6.7}$$

6.3 Observer equations in discrete form

The Euler method is used to transforms the observer equations to the discrete form. The Euler equation is:

$$f(x + \Delta x) = f(x) + f'(x).\Delta x \tag{6.8}$$

Using equation 6.8, the discrete form of equation 6.5 is:

$$\begin{cases} \hat{\imath}_a[k+1] = \hat{\imath}_a[k] - \dfrac{T_s}{l}\left(r\hat{\imath}_a[k] + \sum_{i=1}^{3} S_i \hat{v}_{ci}[k] + 6sgn(i_a[k]) - e_a[k] + \hat{v}_n[k]\right) \\ \qquad\qquad -T_s L_1 sat(\hat{\imath}_a[k] - i_a[k]) \\ \hat{v}_{c1}[k+1] = \hat{v}_{c1}[k] + \dfrac{T_s}{2c}(S_1.\hat{\imath}_a[k] - i_{o1}[k]) \\ \qquad\qquad -T_s L_2 sat\big(-lS_1 L_1 sat(\hat{\imath}_a[k] - i_a[k])\big) \end{cases} \tag{6.9}$$

The discrete form of equation 6.6 is:

$$\begin{cases} \hat{\imath}_a[k+1] = \hat{\imath}_a[k] - \dfrac{T_s}{l}\left(r\hat{\imath}_a[k] + \sum_{i=1}^{3} S_i \hat{v}_{ci}[k] + 6sgn(i_a[k]) - e_a[k] + \hat{v}_n[k]\right) \\ \qquad\qquad -T_s L_1 sat(\hat{\imath}_a[k] - i_a[k]) \\ \hat{v}_{c1}[k+1] = \hat{v}_{c1}[k] + \dfrac{T_s}{2c}(S_1.\hat{\imath}_a[k] - i_{o1}[k]) \end{cases} \tag{6.10}$$

In equations 6.9 and 6.10, $\hat{\imath}_a[k]$ is the observed value of phase-a line current, $\hat{v}_{c1}[k]$ is the observed value of dc-link voltage v_{c1}, $i_a[k]$ is the measured phase-a line current, $e_a[k]$ is the measured phase-a supply voltage, T_s is the calculations time step and $i_{o1}[k]$ is the load current of v_{c1}. Equations 6.9 and 6.10 will be implemented in the FPGA using a fixed-point system. The FPGA has a limited number of gates therefore equations 6.9 and 6.10 should be

simplified as much as possible to occupy the minimum number of gates on FPGA. The multiplication and division of two numbers in fixed-point system needs lots of bits and gates, therefore it is desirable to minimise the number of multiplication and division actions.

First $\hat{v}_n$ in equation 6.9 is substituted with the expression in equation 6.7. Combining equations 6.7 and 6.9 results in:

$$\begin{cases} \hat{\imath}_a[k+1] = \hat{\imath}_a[k] - \dfrac{T_s}{l}\Bigg(r\hat{\imath}_a[k] + \displaystyle\sum_{i=1}^{3} S_i\hat{v}_{ci}[k] + 6sgn(i_a[k]) - e_a[k] \\ \qquad\qquad -\dfrac{1}{3}\displaystyle\sum_{i=1}^{9} S_i\hat{v}_{ci}[k] - 2sgn(i_a) - 2sgn(i_b) - 2sgn(i_c)\Bigg) \\ \qquad\qquad -T_sL_1sat(\hat{\imath}_a[k] - i_a[k]) \\ \\ \hat{v}_{c1}[k+1] = \hat{v}_{c1}[k] + \dfrac{T_s}{2c}(S_1.\hat{\imath}_a[k] - i_{o1}[k]) \\ \qquad\qquad -T_sL_2sat\big(-lS_1L_1sat(\hat{\imath}_a[k] - i_a[k])\big) \end{cases} \tag{6.11}$$

The first step toward simplification of equation 6.11 is to assume that all the dc-link voltages are equal.

$$v_{c1} = v_{c2} = \cdots = v_{c9} \tag{6.12}$$

Therefore equation 6.11 simplifies:

$$\begin{cases} \hat{\imath}_a[k+1] = \hat{\imath}_a[k] - \dfrac{T_s}{l}\{r\hat{\imath}_a[k] - e_a[k] \\ \qquad\qquad + \dfrac{\hat{v}_{c1}[k]}{3}.(2S_1 + 2S_2 + 2S_3 - S_4 - S_5 - S_6 - S_7 - S_8 - S_9) \\ \qquad\qquad +4sgn(i_a) - 2sgn(i_b) - 2sgn(i_c)\} - T_sL_1sat(\hat{\imath}_a[k] - i_a[k]) \\ \\ \hat{v}_{c1}[k+1] = \hat{v}_{c1}[k] + \dfrac{T_s}{2c}(S_1.\hat{\imath}_a[k] - i_{o1}[k]) \\ \qquad\qquad -T_sL_2sat\big(-lS_1L_1sat(\hat{\imath}_a[k] - i_a[k])\big) \end{cases} \tag{6.13}$$

The measurements $i_a[k]$, $i_{o1}[k]$ and $e_a[k]$ in FPGA are available through the A/D converters in binary form. The relationship between the real variable values and corresponding digital variable values are as follows:

$$\frac{adc_{i_a}[k]-8136}{-1401}=i_a[k],\frac{adc_{i_{o1}}[k]-8136}{1401}=i_{o1}[k],\frac{adc_{e_a}[k]-8200}{-14.815}=e_a[k] \quad (6.14)$$

Where $adc_{i_a}[k]$, $adc_{i_{o1}}[k]$ and $adc_{e_a}[k]$ are the digital equivalents of $i_a[k]$, $i_{o1}[k]$ and $e_a[k]$ respectively. This would take a lot of space on the FPGA to convert the digital numbers $adc_{i_a}[k]$, $adc_{i_{o1}}[k]$ and $adc_{e_a}[k]$ to $i_a[k]$, $i_{o1}[k]$ and $e_a[k]$. Also scaling numbers in a fixed-point system with a limited number of bits reduces accuracy. Therefore, in order to increase the accuracy of the calculations and reduce the required number of gates for the observer equations, equation 6.13 is modified to have $adc_{i_a}[k]$, $adc_{i_{o1}}[k]$ and $adc_{e_a}[k]$ instead of $i_a[k]$, $i_{o1}[k]$ and $e_a[k]$. Also a new variable $\hat{adc}_{i_a}[k]$ is defined:

$$\hat{i}_a[k]=\frac{\hat{adc}_{i_a}[k]-8136}{-1401} \quad (6.15)$$

The modified form of equation 6.13 is:

$$\begin{cases}\dfrac{\hat{adc}_{i_a}[k+1]-8136}{-1401}=\dfrac{\hat{adc}_{i_a}[k]-8136}{-1401}-\dfrac{T_s}{l}\{r\left(\dfrac{\hat{adc}_{i_a}[k]-8136}{-1401}\right)\\ \quad+\dfrac{\hat{v}_{c1}[k]}{3}.(2S_1+2S_2+2S_3-S_4-S_5-S_6-S_7-S_8-S_9)\\ \quad-\dfrac{adc_{e_a}[k]-8200}{-14.815}+4sgn(i_a)-2sgn(i_b)-2sgn(i_c)\}\\ \quad-T_sL_1sat\left(\dfrac{\hat{adc}_{i_a}[k]-8136}{-1401}-\dfrac{adc_{i_a}[k]-8136}{-1401}\right)\\ \hat{v}_{c1}[k+1]=\hat{v}_{c1}[k]+\dfrac{T_s}{2c}\left(S_1.\left(\dfrac{\hat{adc}_{i_a}[k]-8136}{-1401}\right)-\dfrac{adc_{i_{o1}}[k]-8136}{1401}\right)\\ \quad-T_sL_2sat\left(-lS_1L_1sat\left(\dfrac{\hat{adc}_{i_a}[k]-8136}{-1401}-\dfrac{adc_{i_a}[k]-8136}{-1401}\right)\right)\end{cases} \quad (6.16)$$

The simplified form of equation 6.16 is:

$$\begin{cases} a\hat{d}c_{i_a}[k+1] = a\hat{d}c_{i_a}[k] - \dfrac{T_s}{l}\{r\big(a\hat{d}c_{i_a}[k] - 8136\big) \\ \quad -467\hat{v}_{c1}[k].(2S_1 + 2S_2 + 2S_3 - S_4 - S_5 - S_6 - S_7 - S_8 - S_9) \\ \quad -94.56adc_{e_a}[k] + 775443 - 5604sgn(i_a) + 2802sgn(i_b) + 2808sgn(i_c)\} \\ \quad +1401T_sL_1sat\left(\dfrac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right) \\ \\ \hat{v}_{c1}[k+1] = \hat{v}_{c1}[k] - \dfrac{T_s}{2802c}\big(S_1.\big(a\hat{d}c_{i_a}[k] - 8136\big) + adc_{i_{o1}}[k] - 8136\big) \\ \qquad -T_sL_2sat\left(-lS_1L_1sat\left(\dfrac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)\right) \end{cases} \tag{6.17}$$

To further decrease the number of required multiplication actions a new variable $a\hat{d}c_{v_{c1}}[k]$ is defined as follows:

$$a\hat{d}c_{v_{c1}}[k] = (467\hat{v}_{c1}[k]) \tag{6.18}$$

Combining equations 6.17 and 6.18 results in:

$$\begin{cases} a\hat{d}c_{i_a}[k+1] = a\hat{d}c_{i_a}[k] - \dfrac{T_s}{l}\{r\big(a\hat{d}c_{i_a}[k] - 8136\big) \\ \quad -a\hat{d}c_{v_{c1}}[k].(2S_1 + 2S_2 + 2S_3 - S_4 - S_5 - S_6 - S_7 - S_8 - S_9) \\ \quad -94.56adc_{e_a}[k] + 775443 - 5604sgn(i_a) + 2802sgn(i_b) + 2808sgn(i_c)\} \\ \quad +1401T_sL_1sat\left(\dfrac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right) \\ \\ a\hat{d}c_{v_{c1}}[k+1] = a\hat{d}c_{v_{c1}}[k] - \dfrac{T_s}{6c}\big(S_1.\big(a\hat{d}c_{i_a}[k] - 8136\big) + adc_{i_{o1}}[k] - 8136\big) \\ \qquad -467T_sL_2sat\left(-lS_1L_1sat\left(\dfrac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)\right) \end{cases} \tag{6.19}$$

Calculations time step	T_s	$2\mu s$
Line inductance	l	$11mH$
Line resistance	r	1Ω
dc-link capacitance	c	$1000\mu F$
Sliding mode observer gain	L_1	1000
Sliding mode observer gain	L_2	1000

Table 6.1: The practical system parameters.

Replacing the variables with the corresponding values given in table 6.1 in observer equations results in equation 6.20.

$$\begin{cases} a\hat{dc}_{i_a}[k+1] = a\hat{dc}_{i_a}[k] - 0.00018\{a\hat{dc}_{i_a}[k] + \\ \quad -a\hat{dc}_{v_{c1}}[k].(2S_1 + 2S_2 + 2S_3 - S_4 - S_5 - S_6 - S_7 - S_8 - S_9) \\ \quad -94.56adc_{e_a}[k] + 767307 - 5604sgn(i_a) + 2802sgn(i_b) \\ \quad +2808sgn(i_c) - 15555sat\left(\dfrac{a\hat{dc}_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)\} \\ a\hat{dc}_{v_{c1}}[k+1] = a\hat{dc}_{v_{c1}}[k] - \dfrac{0.001}{3}\{S_1 a\hat{dc}_{i_a}[k] - S_1 8136 + adc_{i_{o1}}[k] - 8136 \\ \quad +2802sat\left(-11S_1 sat\left(\dfrac{a\hat{dc}_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)\right)\} \end{cases} \quad (6.20)$$

The observer equation 6.20 consists of several terms. Each term has different maximum and minimum values. It is important to know the minimum and maximum value of each term in order to assign proper number of bits to each term. The equation for $a\hat{dc}_{i_a}[k+1]$ consists of the following terms:

$$a\hat{dc}_{i_a}[k+1] = a\hat{dc}_{i_a}[k] - 0.00018\{A + B + C + D + E + F + G + H\} \quad (6.21)$$

Where:

$$A = a\hat{d}c_{i_a}[k], \qquad B = -a\hat{d}c_{v_{c1}}[k].(2S_1 + 2S_2 + 2S_3 - S_4 - S_5 - S_6 - S_7 - S_8 - S_9)$$
$$C = -94.56adc_{e_a}[k], \quad D = 767307, \quad E = -5604sgn(i_a), \quad F = +2802sgn(i_b),$$
$$G = +2808sgn(i_c), \quad H = -15555sat\left(\frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)$$

The equation for $a\hat{d}c_{v_{c1}}[k+1]$ consists of the following terms:

$$a\hat{d}c_{v_{c1}}[k+1] = a\hat{d}c_{v_{c1}}[k] - \frac{0.001}{3}\{I + J + K + L + M\} \tag{6.22}$$

Where:

$$I = S_1 a\hat{d}c_{i_a}[k], \quad J = -S_1 8136, \quad K = adc_{i_{o1}}[k], \quad L = -8136$$
$$M = 2802sat\left(-11S_1 sat\left(\frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)\right)$$

Each number has a sign, an integer part and a decimal part. In a fixed-point system one bit has been assigned for each number to represent the sign. The absolute maximum value of each number determines the number bits that have been assigned for integer part. The accuracy of number and calculation is related to the number of bits that have been assigned for the decimal part. The term E is redefined as follows:

$$\begin{aligned} E = -5604sgn(i_a) &= \begin{cases} -5604 & i_a > 0 \\ 5604 & i_a < 0 \end{cases} \\ &= \begin{cases} -5604 & \dfrac{adc_{i_a}[k] - 8136}{-1401} > 0 \\ 5604 & \dfrac{adc_{i_a}[k] - 8136}{-1401} < 0 \end{cases} \\ &= \begin{cases} -5604 & adc_{i_a}[k] < 8136 \\ 5604 & adc_{i_a}[k] > 8136 \end{cases} \end{aligned} \tag{6.23}$$

In order to define the terms H and M as digital variables, a new term H_1 is defined:

$$H_1 = -1401sat\left(\frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)$$

$$= \begin{cases} 1401 & \frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401} < -1 \\ -1401.\left(\frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right) & -1 < \frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401} < +1 \\ -1401 & \frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401} > +1 \end{cases}$$

$$= \begin{cases} 1401 & a\hat{d}c_{i_a}[k] - adc_{i_a}[k] > +1401 \\ a\hat{d}c_{i_a}[k] - adc_{i_a}[k] & -1401 < a\hat{d}c_{i_a}[k] - adc_{i_a}[k] < +1401 \\ -1401 & a\hat{d}c_{i_a}[k] - adc_{i_a}[k] < -1401 \end{cases} \quad (6.24)$$

Therefore the term H can be calculated as:

$$H = -15555sat\left(\frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right) = 11.1 \times H_1 \quad (6.25)$$

The term M as a digital variable can be calculated as:

$$M = 2802sat\left(-11S_1 sat\left(\frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)\right)$$

$$= 2802sat\left(S_1\frac{H_1}{127.36}\right)$$

$$= \begin{cases} -2802 & S_1\frac{H_1}{127.36} < -1 \\ 2802.\left(S_1\frac{H_1}{127.36}\right) & -1 < S_1\frac{H_1}{127.36} < +1 \\ 2802 & S_1\frac{H_1}{127.36} > +1 \end{cases}$$

$$= \begin{cases} -2802 & S_1H_1 < -127.36 \\ 22(S_1H_1) & -127.36 < S_1H_1 < +127.36 \\ 2802 & S_1H_1 > +127.36 \end{cases} \quad (6.26)$$

6.4 Observer equations in fixed-point

It is important to calculate the absolute maximum of each term in order to avoid any overflow in the calculations. In a binary system, shifting the number to left by one bit means multiplication by 2 and shifting the binary number to right by one bit means division by 2. The 2's complement system is used to do the mathematical operations in binary.

The digital numbers $adc_{i_a}[k], adc_{i_{o1}}[k]$ and $adc_{e_a}[k]$ are 14-bit integer numbers. The absolute maximum of the line current is assumed to be 5A. The absolute maximum of the supply voltage is 250V and the maximum value of the dc-link voltage is set to 120V. In order to have good accuracy of the observer equations in fixed-point system, fifty five-bits are assigned for the $\hat{adc}_{i_a}[k]$, where 14 bits are for integer part and 41 bits for decimal part. Also 55 bits are assigned for the digital variable $\hat{adc}_{v_{c1}}[k]$. The maximum value of $\hat{adc}_{v_{c1}}[k]$ is equal to $467 \times 120 = 56040$. Therefore 16 bits are used for integer part of $\hat{adc}_{v_{c1}}[k]$ and the other 39 bits are assigned for decimal part.

The relationship between the absolute maximum value of a number and the required number of bits in integer part of corresponding binary value is described in this part. By using n bits in integer part of a binary number, it is possible to have the equivalent decimal value up to $(2^n - 1)$. If the absolute maximum value exceeds $(2^n - 1)$, then $(n + 1)$ bits are required in integer part of a binary number. Therefore n bits are needed in integer part of a binary number with absolute maximum value bigger than $(2^{n-1} - 1)$ and smaller or equal to $(2^n - 1)$.

Figure 6.4 to 6.22 shows the formation of these variables. The sign bit is shown in green, the integer bits are displayed in white and decimal bits are displayed in orange. The digital variables $adc_{i_a}[k]$, $adc_{i_{o1}}[k]$, $adc_{e_a}[k]$, $A = a\hat{d}c_{i_a}[k]$ and $a\hat{d}c_{v_{c1}}[k]$ are defined in previous section of this chapter.

$adc_{i_a}[k]$

13	12	11	10	09	08	07	06	05	04	03	02	01	00
a	a	a	a	a	a	a	a	a	a	a	a	a	a

$adc_{i_{o1}}[k]$

13	12	11	10	09	08	07	06	05	04	03	02	01	00
a	A	a	a	a	a	a	a	a	a	a	a	a	a

$adc_{e_a}[k]$

13	12	11	10	09	08	07	06	05	04	03	02	01	00
a	A	a	a	a	a	a	a	a	a	a	a	a	a

$A = a\hat{d}c_{i_a}[k]$

55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

$a\hat{d}c_{v_{c1}}[k]$

55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.4: The binary representation of digital variables $adc_{i_a}[k]$, $adc_{i_{o1}}[k]$, $adc_{e_a}[k]$, $A = a\hat{d}c_{i_a}[k]$ and $a\hat{d}c_{v_{c1}}[k]$

As variable B could be either positive or negative, one bit is assigned to show the sign, 20 bits are used for integer part and 35 bit are used for decimal part of B. The formation of variable B is shown in figure 6.5.

$$B = -a\hat{d}c_{v_{c1}}[k].(2S_1 + 2S_2 + 2S_3 - S_4 - S_5 - S_6 - S_7 - S_8 - S_9) \tag{6.27}$$

$$0 < a\hat{d}c_{v_{c1}}[k] < 56040 \Rightarrow -672480 < B < +672480 \tag{6.28}$$

$B = -a\hat{d}c_{v_{c1}}[k].(2S_1 + 2S_2 + 2S_3 - S_4 - S_5 - S_6 - S_7 - S_8 - S_9)$

55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
s	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.5: The binary representation of digital variable B

As variable C could be either positive or negative, one bit is assigned to show the sign, 21 bits are used for integer part and 34 bits are used for decimal part of C. Variable C is shown in figure 6.6.

$$C = -94.56adc_{e_a}[k] \tag{6.29}$$

$$(94.56)_{10} = (1011110.100011110101110000010)_2 \tag{6.30}$$

$$-250 < e_a < 250 \Rightarrow 4496 < adc_{e_a}[k] < 11904 \Rightarrow -1125643 < C < -425141 \tag{6.31}$$

$C = -94.56adc_{e_a}[k]$

55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
s	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.6: The binary representation of digital variable C

$$D = 767307 \tag{6.32}$$

$$(767307)_{10} = (10111011010101001011)_2 \tag{6.33}$$

$D = 767307$

19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	1	1	1	0	1	1	0	1	0	1	0	1	0	0	1	1	0	0

Figure 6.7: The binary representation of D

Variable E could be either +5604 or -5604 therefore one bit is assigned to show the sign and 13 bits are used for integer part. Variable E is shown in figure 6.8.

$$E = -5604sgn(i_a) \tag{6.34}$$

$$(5604)_{10} = (1010111100100)_2 \tag{6.35}$$

$E = -5604sgn(i_a)$

13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	1	0	1	0	1	1	1	1	0	0	1	0	0

Figure 6.8: The binary representation of digital variable E

Variables F and G could be either +2802 or -2802, therefore one bit is assigned to show the sign and 12 bits are used for integer part.

$$F = +2802sgn(i_b), \qquad G = +2802sgn(i_c) \tag{6.36}$$

$$(2802)_{10} = (101011110010)_2 \tag{6.37}$$

$F = +2802sgn(i_b),\ \ G = +2802sgn(i_c)$

12	11	10	09	08	07	06	05	04	03	02	01	00
S	1	0	1	0	1	1	1	1	0	0	1	0

Figure 6.9: The binary representation of F and G

$$H_1 = -1401sat\left(\frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right) = \begin{cases} 1401 & a\hat{d}c_{i_a}[k] - adc_{i_a}[k] > +1401 \\ a\hat{d}c_{i_a}[k] - adc_{i_a}[k] & -1401 < a\hat{d}c_{i_a}[k] - adc_{i_a}[k] < +1401 \\ -1401 & a\hat{d}c_{i_a}[k] - adc_{i_a}[k] < -1401 \end{cases} \tag{6.38}$$

The 56-bit variable H_1 could be either positive or negative. Therefore, one bit is assigned to show the sign.

$a\hat{d}c_{i_a}[k],\ \ adc_{i_a}[k]$

55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a
															13	12	11	10	09	08	07	06	05	04	03	02	01	00																																
															a	a	a	a	a	a	a	a	a	a	a	a	a	a																																

H_1

55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	A	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.10: The binary representation of digital variable H_1

$$H = 11.1 \times H_1 \tag{6.39}$$

$$(11.1)_{10} = (1011.0001100110)_2 \tag{6.40}$$

$$-1401 < H_1 < 1401 \;\Rightarrow\; -14010 < H < 14010 \tag{6.41}$$

As variable H could be either positive or negative, one bit is assigned to show the sign, 14 bits are used for integer part and 38 bits are used for decimal part.

$$H = -15555sat\left(\frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right) = 11.1 \times H_1$$

			52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
			S	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.11: The binary representation of digital variable H

$$\left\{\begin{array}{c} -16383 < A < 16383 \\ -672480 < B < +672480 \\ -1125643 < C < -425141 \\ D = 767307 \\ E = -5604sgn(i_a) \\ F = +2802sgn(i_b) \\ G = +2802sgn(i_c) \\ -14010 < H < 14010 \end{array}\right\} \Rightarrow\; -1072417 < (A + B + C + D + E + F + G + H) < 1056247 \tag{6.42}$$

The absolute maximum of $(A+B+C+D+E+F+G+H)$ is equal to 1072417, therefore 21 bits are required in integer part, 41bits are used in decimal part and one bit is used for sign. The digital variable $(A+B+C+D+E+F+G+H)$ is shown in figure 6.12.

A, B, C, D, E, F, G, H

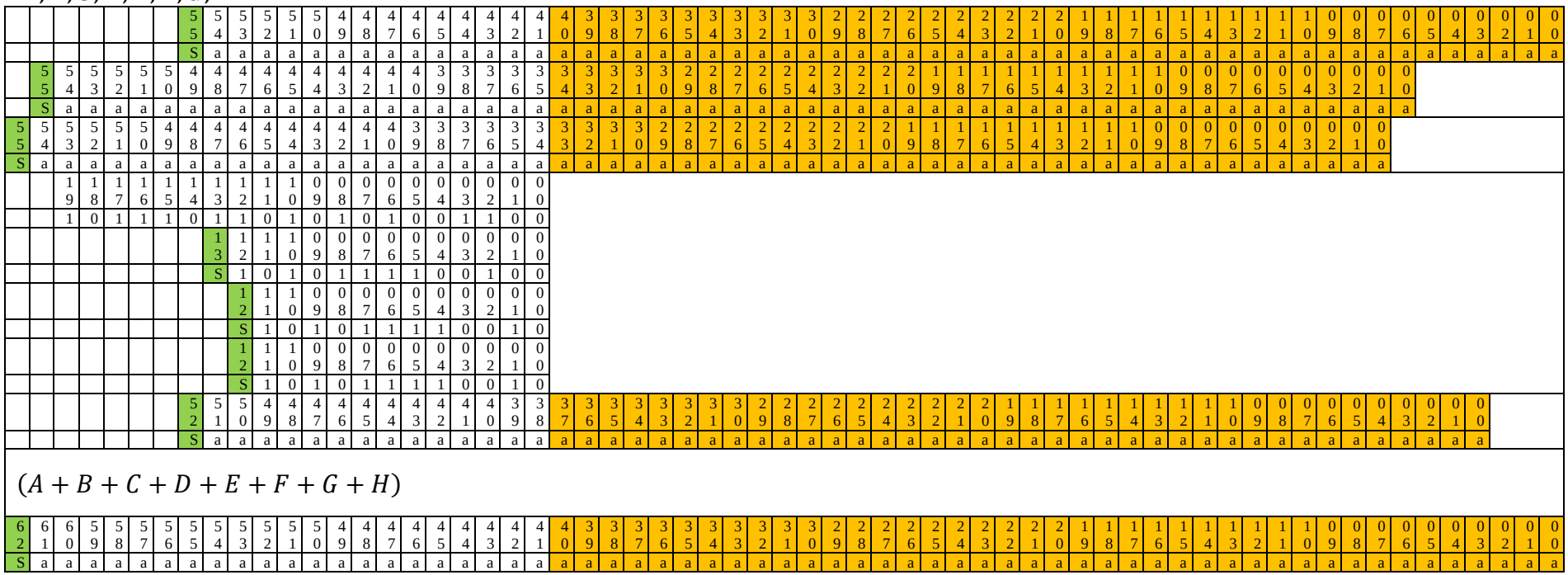


Figure 6.12: The binary representation of digital variable $(A+B+C+D+E+F+G+H)$

$$(0.00018)_{10} = (0.0000000000000101111)_2 \tag{6.43}$$

$$-190 < \left(-0.00018 \times (A + B + C + D + E + F + G + H)\right) < 193 \tag{6.44}$$

The absolute maximum of $\left(-0.00018 \times (A + B + C + D + E + F + G + H)\right)$ is equal to 193, therefore 8 bits are required in integer part, 41bits are used in decimal part and one bit is used for sign.

$-0.00018 \times (A + B + C + D + E + F + G + H)$

49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.13: The binary representation of digital variable $-0.00018 \times (A + B + C + D + E + F + G + H)$

$$a\hat{d}c_{i_a}[k+1] = a\hat{d}c_{i_a}[k] - 0.00018\{A + B + C + D + E + F + G + H\} \tag{6.45}$$

$-0.00018\{A + B + C + D + E + F + G + H\}$, $a\hat{d}c_{i_a}[k]$

						49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
						s	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a
55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
s	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

$a\hat{d}c_{i_a}[k+1] = a\hat{d}c_{i_a}[k] - 0.00018\{A + B + C + D + E + F + G + H\}$

55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
s	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.14: The binary representation of digital variable $a\hat{d}c_{i_a}[k+1] = a\hat{d}c_{i_a}[k] - 0.00018\{A + B + C + D + E + F + G + H\}$

$I = S_1 a\hat{d}c_{i_a}[k]$

55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.15: The binary representation of digital variable $I = S_1 a\hat{d}c_{i_a}[k]$

The variable J could be zero, +8136 or -8136 therefore one bit is assigned to show the sign and 13 bits are used for integer part. The digital variable J is shown in figure 6.16.

$$J = -S_1 8136 \tag{6.46}$$

$J = -S_1 8136$

13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	1	1	1	1	1	1	1	0	0	1	0	0	0

Figure 6.16: The binary representation of $J = -S_1 8136$

The variable K is a positive integer with an absolute maximum of equal to 12339. Therefore 14 bits are required for integer part of its binary representation which is shown in figure 6.17

$$K = adc_{i_{o1}}[k] \tag{6.47}$$

$$0 < i_{o1}[k] < +3 \;\Rightarrow\; +8136 < adc_{i_{o1}}[k] < +12339 \tag{6.48}$$

$K = adc_{i_{o1}}[k]$

13	12	11	10	09	08	07	06	05	04	03	02	01	00
a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.17: The binary representation of $K = adc_{i_{o1}}[k]$

The variable L is a negative integer with an absolute maximum of equal to 8136. Therefore one bit is need as sign bit and thirteen bits are required for integer part of its binary representation which is shown in figure 6.18.

$$L = -8136 \tag{6.49}$$

$L = -8136$

13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	1	1	1	1	0	0	1	0	0	0

Figure 6.18: The binary representation of L

The absolute maximum of M is equal to 2802, therefore twelve bits are required in integer part, forty-one bits are used in decimal part and one bit is used for sign.

$$M = 2802sat\left(-11S_1 sat\left(\frac{\hat{adc}_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)\right) = \begin{cases} -2802 & S_1H_1 < -127.36 \\ 22(S_1H_1) & -127.36 < S_1H_1 < +127.36 \\ 2802 & S_1H_1 > +127.36 \end{cases} \tag{6.50}$$

$$(22)_{10} = (10110)_2 \tag{6.51}$$

Where H_1 is presented in equation 6.38. The binary representation of the digital variable M is shown in figure 6.19.

H_1

55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

$$M = 2802sat\left(-11S_1 sat\left(\frac{a\hat{d}c_{i_a}[k] - adc_{i_a}[k]}{-1401}\right)\right)$$

	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a

Figure 6.19: The binary representation of digital variable H_1 and M.

The absolute maximum of $(I + J + K + L + M)$ is equal to 31524, therefore fifteen bits are required in integer part, forty one bits are used in decimal part and one bit is used for sign.

$$\left\{\begin{matrix} -16383 < I < +16383 \\ -8136 < J < +8136 \\ +8136 < K < +12339 \\ L = -8136 \\ -2802 < M < +2802 \end{matrix}\right\} \Rightarrow -27321 < (I + J + K + L + M) < 31524 \qquad (6.52)$$

The binary representation of the digital variable $(I + J + K + L + M)$is shown in figure 6.20.

I, J, K, L, M

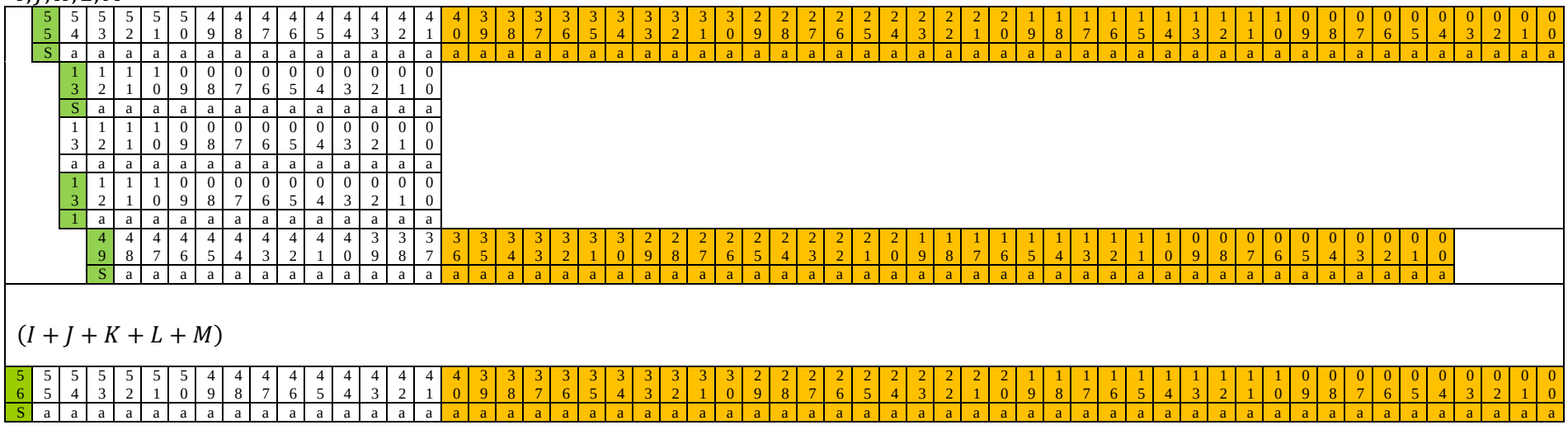


Figure 6.20: The binary representation of digital variable $(I + J + K + L + M)$

According to equation 6.52 the absolute maximum of $(I + J + K + L + M)$ is equal to 31524, therefore the absolute maximum of $(-0.000333 \times I+J+K+L+M$ is equal to 11. So four bits are required in integer part, forty one bits are used in decimal part and one bit is used for sign. The binary representation of the digital variable $\left(-0.000333 \times (I + J + K + L + M)\right)$ is shown in figure 6.21.

$$(0.000333)_{10} = (0.00000000000101011101)_2 \tag{6.53}$$

$$-11 < \left(-0.000333 \times (I + J + K + L + M)\right) < 10 \tag{6.54}$$

$\left(-0.000333 \times (I + J + K + L + M)\right)$

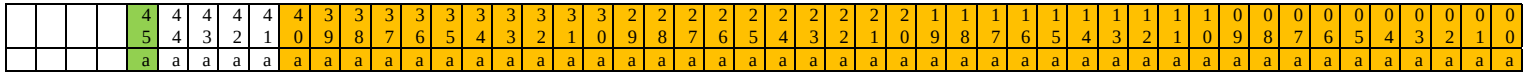


Figure 6.21: The binary representation of digital variable $\left(-0.000333 \times (I + J + K + L + M)\right)$

The binary representation of the digital variable $a\hat{d}c_{v_{c1}}[k+1]$ is shown in figure 6.22.

$$a\hat{d}c_{v_{c1}}[k+1] = a\hat{d}c_{v_{c1}}[k] - 0.000333(I + J + K + L + M) \tag{6.55}$$

$-0.000333(I + J + K + L + M)$, $a\hat{d}c_{v_{c1}}[k]$

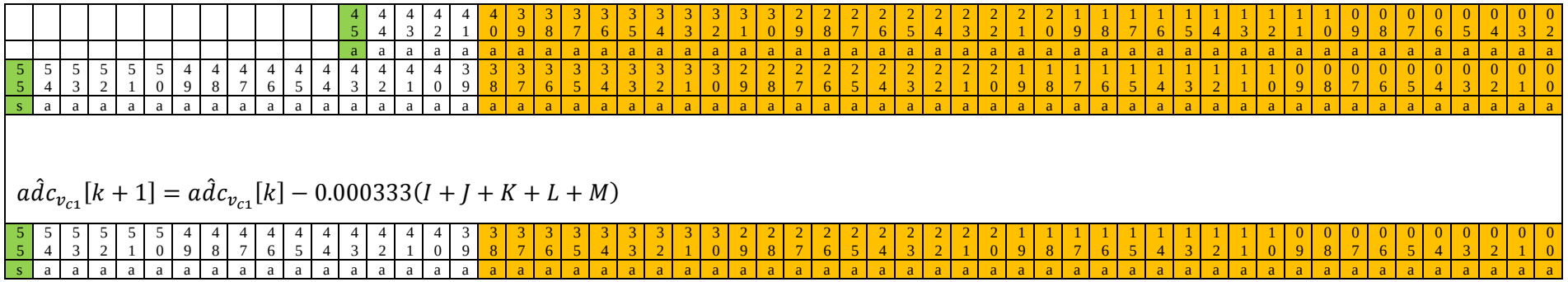


Figure 6.22: The binary representation of digital variable $a\hat{d}c_{v_{c1}}[k+1] = a\hat{d}c_{v_{c1}}[k] - 0.000333(I + J + K + L + M)$

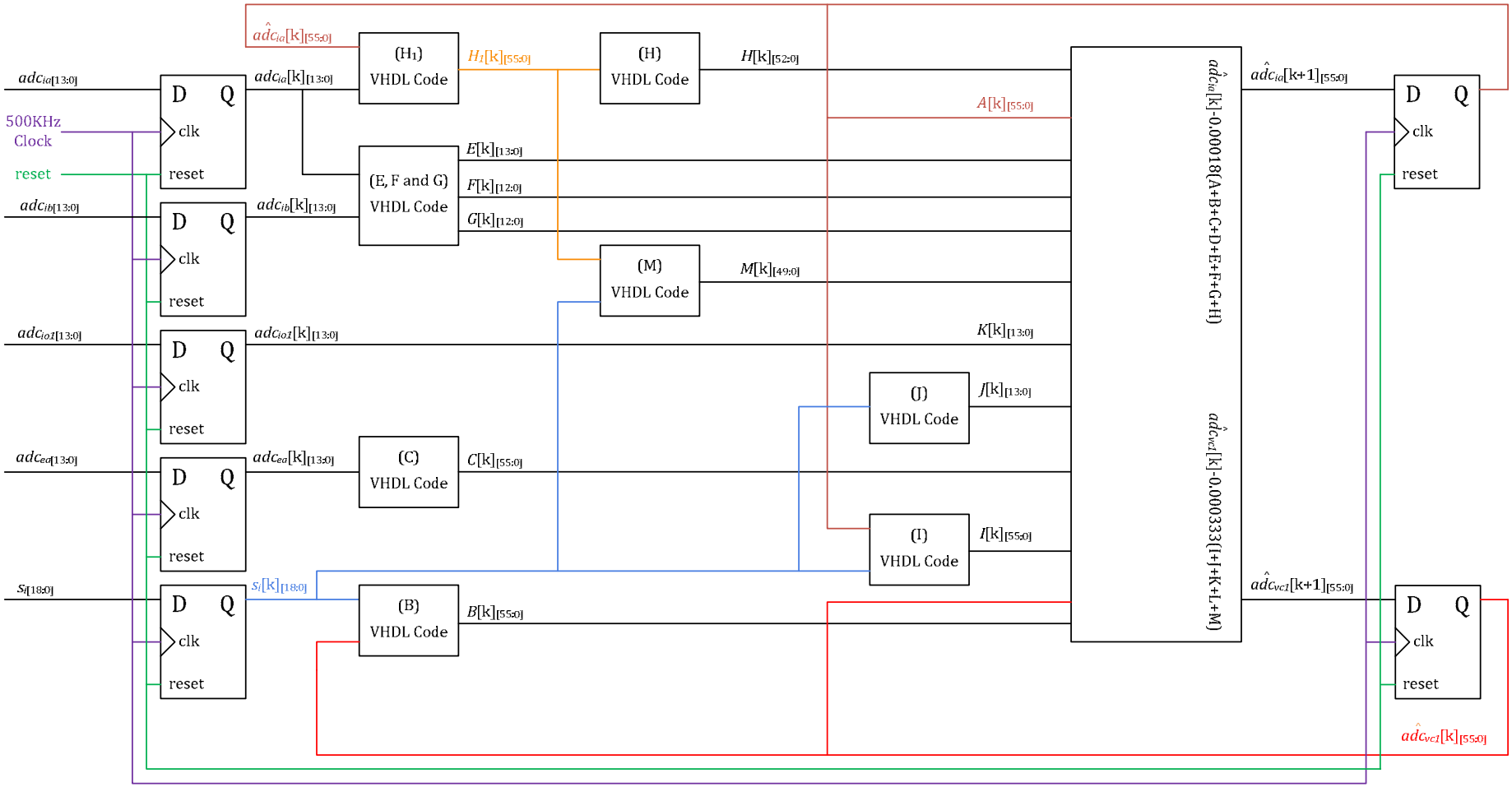


Figure 6.23: Practical implementation of the observer equation in FPGA.

The block diagram of the practical implementation of the observer in FPGA is presented in figure 6.23. The calculation time-step is controlled by a $500KHz$ clock. This is relatively a high clock frequency. As mentioned earlier the duration of the observable states within a period are very limited and decreases as the number of cascaded H-bridges increases. In order to have precise observed values it is necessary to have enough number of calculation steps within an observable state. For a multilevel inverter, having three cascaded H-bridge a $500KHz$ clock gives acceptable results. Obviously the clock frequency should be increased for a multilevel inverter with more cascaded H-bridges.

The 14-bit D type flip-flops are used to sample the digital variables with a frequency of $500KHz$ to be used in observer equations. There are eighteen switching states produced by PWM unit in the FPGA platform. Two switching states are sent to each H-bridge converter. Therefore 18-bit D type flip-flops are used to sample the switching states with a frequency of $500KHz$ to be used in observer equations. Also two 55-bit D type flip-flops are used to converter the observer output at step $K+1$ to observer output at step K.

6.5 Practical results of observer

The practical results of the observer are presented in figures 6.24 – 6.26. In figure 6.24 the measured and observed values of v_{c1} and i_a under steady state conditions are presented.

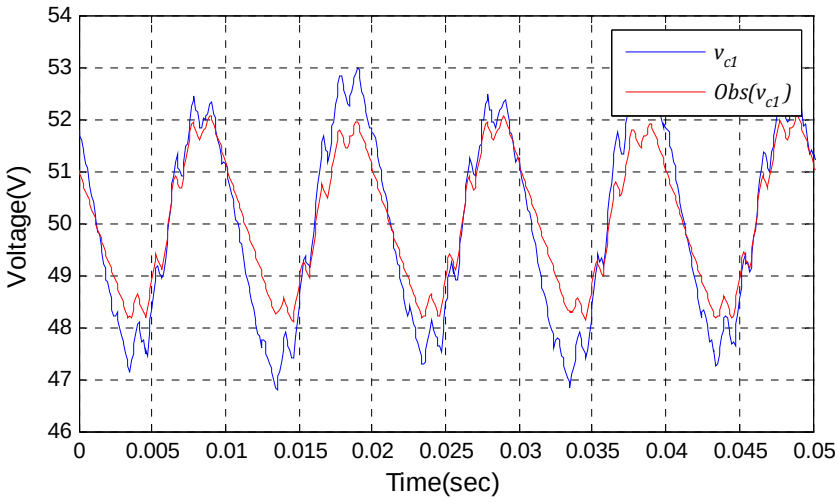


Figure 6.24 a) Practical results of observer under steady state conditions, v_{c1} and $\hat{v}_{c1}$

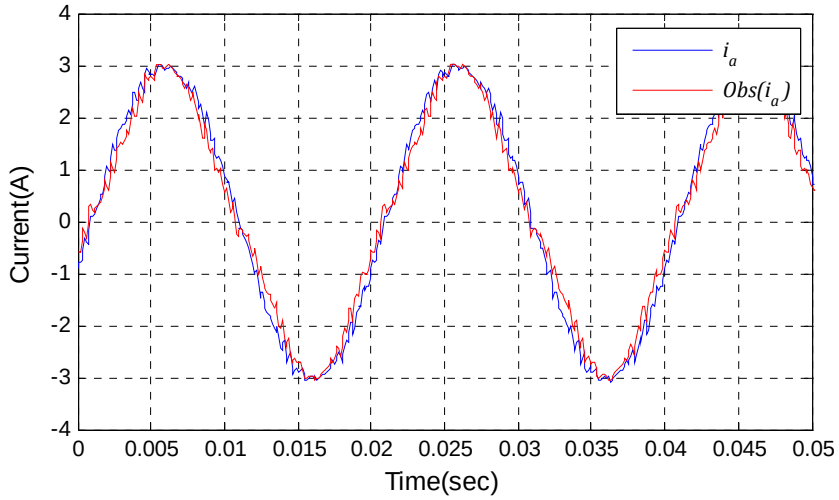


Figure 6.24 b) Practical results of observer under steady state conditions, i_a and $\hat{\imath}_a$

In order to verify the proposed observer performance under step change condition, two step changes are applied in input power at $t = 0.68\,sec$ and $t = 2.78\,sec$. The dc-link voltages are shown in figures 6.25 and 6.26.

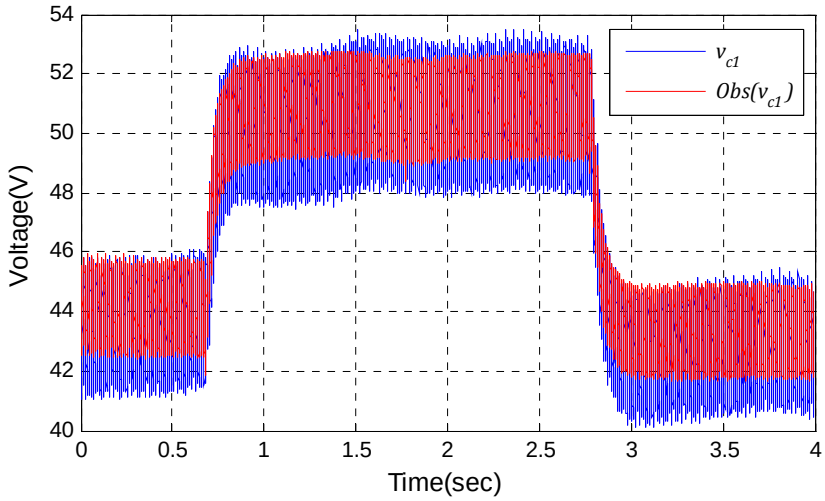


Figure 6.25: Practical results of observer under step change in input power

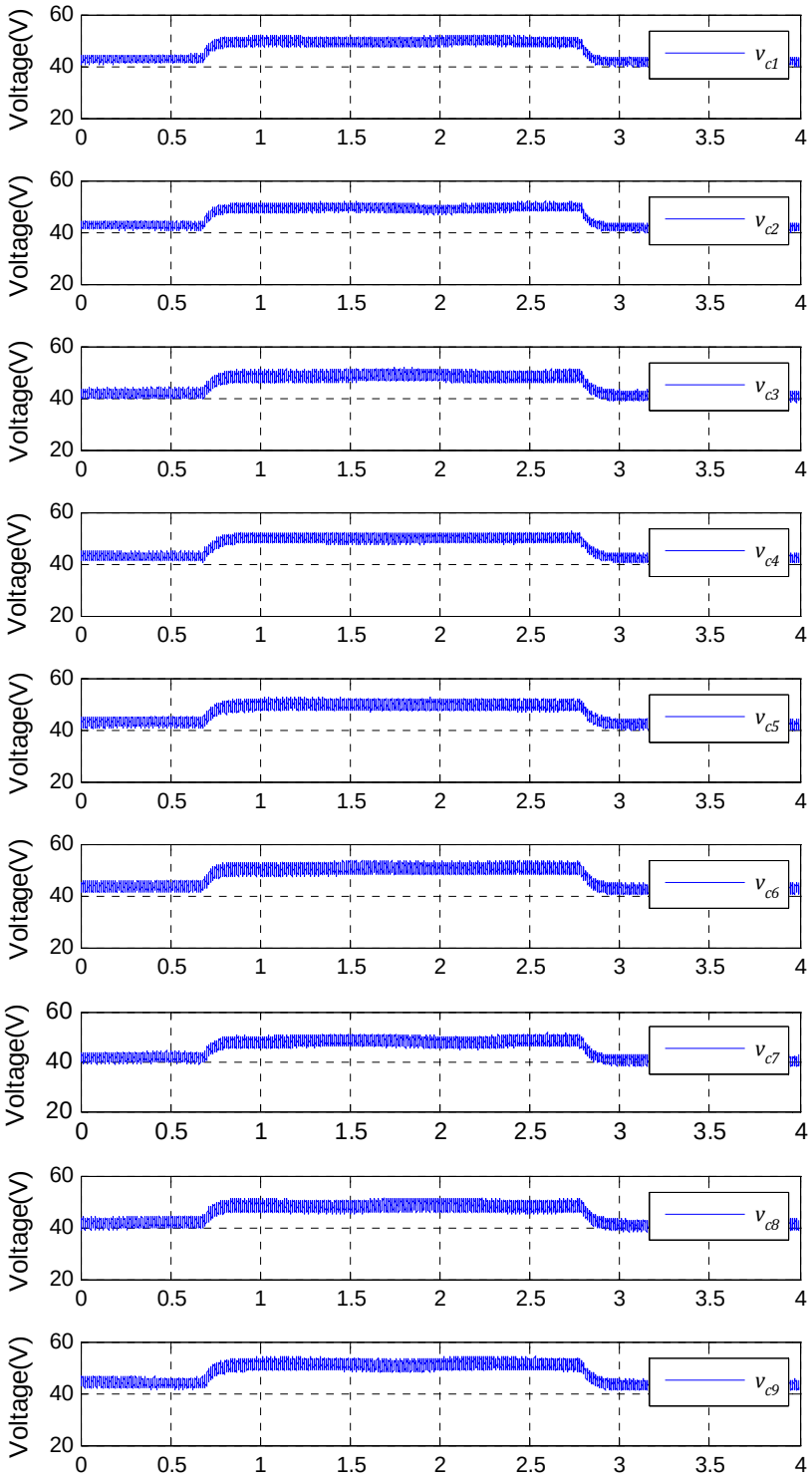


Figure 6.26: Practical results of $v_{c1} - v_{c9}$ under step change in input power

All the dc-link voltages have the same change. The observer result is shown in figure 6.25. The practical results confirm that the observer work well under step change condition.

6.6 Summary

In this chapter the sliding mode observers based on equivalent control method have been implemented practically on FPGA using VHDL programming language in fixed point system. The 2's complement method has been used to perform mathematical operations in binary. The switching model of practical power converter considering the effect of real IGBTs is presented. In order to increase the accuracy of calculations and to reduce the required gates for observer implementations, the observer equations are modified in way to have digital variables instead of real variables. Finally practical results of observer on three-phase and three-cell prototype power converter are presented. Practical results confirm the efficiency of proposed observer in power converter applications.

Chapter 7

Conclusion

Multilevel power converters are widely used in medium voltage applications. There are several topologies for multilevel power converters. The cascaded H-bridge converter is one of multilevel power converter topologies with modular structure. The three-phase cascaded H-bridge converter is the possible topology for the power electronic substation and is considered in this work. The power electronic substation could be capable of providing Voltage ratio adjustment, Frequency changing, Phase changing, Asymmetric load current cancellation, Voltage asymmetry cancellation, Reactive power control, Active power control and Harmonic cancellation in a power network. To achieve any of these functions, a number of control loops are required.

Three control loops include a current control loop, voltage control loop and capacitor balancing loop have been implemented at port-A and a current control loop has been implemented at port-B. The dq transformation has been used to decouple the system equations. The control loops are designed based on the “root locus method”. Phase-Shifted-Cascaded PWM has been selected and implemented as the power converter modulation technique.

In order to increase the control system reliability, a capacitor voltage observer is implemented on the power converter to have redundant knowledge of dc-link voltages. Several observation methods have been considered for this application. A sliding mode observer (SMO) based on the equivalent control method has been chosen and implemented on a two-port power converter. The selected SMO is easy to implement practically and is robust against some of uncertainties in system model or system parameters. In order to avoid chattering and high frequency discontinuous signals a piecewise linear approximation of the $sgn()$ function has been used in observer equation.

The first step in observer design procedure is to check the system observability. In the multilevel cascaded H-bridge converter, system observability depends on the system switching states. It has been shown that only a small percentage of a switching period is fully observable and the observable states decrease as the number of cascaded H-bridge cells increases. During unobservable modes the voltage observer tracks the voltage ripples without trying to decrease the offset between observed and measured values. During unobservable modes, any uncertainty in capacitance value or any measurement error in currents will result in voltage drift.

In order to have precise observed values it is necessary to have enough number of calculation steps within an observable state. For a multilevel inverter, having three cascaded H-bridge a $500KHz$ clock gives acceptable results. Obviously the clock frequency should be increased for a multilevel inverter with higher number of cascaded H-bridges.

In the two-port power converter, the selected SMO is robust only against variation in capacitance value and measurement error in output current. The measurement error in output current is caused by the DC-DC converters. Any other variation in parameter values or any simplification in system model will result in voltage drift in observer output. In practical power converter the voltage drop across IGBT switches should be modeled in observer equations. Application of the SMO without considering the small voltage drop across the IGBT switches will cause offset in observer results.

To validate the proposed observer a three-phase three-cell power converter has been constructed. The sliding mode observers based on the equivalent control method has been implemented practically on the FPGA using a VHDL programming language with fixed point numbers. The voltage drop on the IGBT switches during conduction mode is considered in observer equations to improve the accuracy of the observer equations. The calculation time-step is controlled by a $500KHz$ clock. Practical results confirm the correct operation of the proposed observer in this power converter application. The following section summarizes the achievements and contributions of thesis.

7.1. Achievements and new contributions

The achievement and new contributions related to the challenges and difficulties of the dc-link voltage observation in the two-port power converter are presented in this section. The main challenges which have been discussed in section 1.1 are listed below.

- Complex structure of the power converter doesn't allow having exact mathematical model of the system hence an approximated model of system has been used to construct the observer equations.

- The magnetizing and core loss currents in the medium frequency transformers of the DC-DC converters introduce error in the output current measurements.

- In practical cases the capacitance value are different from the nominal value and there is always uncertainty in capacitance.

- The system observability depends on the power converter switching states. The dc-link voltages are observable during a very small fraction of a switching period. The duration of observable states decreases as the number of cascaded H-bridges increases.

The solution for each challenge and also the new achievements of thesis are listed as follows:

- Since the presence of the DC-DC converter in each module of the power converter increases the system model complexity, a simplified model has been presented in section 4.6. Based on this model the observer equations have been constructed.

- An observer has been designed which is robust to output current measurement error caused by magnetizing and core loss currents in the medium-frequency transformers.

- An observer has been designed which is robust to capacitance value changes.

- The challenge of observability has been addressed. This has entailed the calculation being controlled by a $500KHz$ clock. For a multilevel inverter, having three cascaded H-bridge a $500KHz$ clock gives acceptable results. As observable states are only a small fraction of a switching period, such a high frequency is necessary.

- The SMO using the equivalent control method has no robustness to model mismatch because of the voltage drop across IGBT switches. An improved mathematical model that considers the voltage drops across switches has been developed in section 6.3.

It has been shown that the selected observer is suitable for the two-port power converter. However some further work is needed to be done. A list of possible further work is listed in the following section.

7.2. Further work

- Observing all dc-link voltages using an FPGA with bigger number of gates or may be using several FPGAs or combination of both solutions.

- Implementation of observer to a multilevel inverter with higher number of cells to prove its applicability for multilevel inverters having more than three cells.

- Choosing optimum sampling frequency for observer equations in multilevel inverters with different number of cells.

- Using the dc-link observed values instead of measured values in feedback loops to validate the practical applicability of the proposed observation method in closed loop applications.

- Applying observer at both ports of power converter and using the observed values in DC-DC converters as well as voltage control loop and capacitor voltage balancers.

Appendix A

Published Papers

I. Almaleki, M., P. Wheeler, and J. Clare. *Sliding mode observer design for universal flexible power management (Uniflex-PM) structure*. in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*. 2008.

II. Almaleki, M., P. Wheeler, and J. Clare. *Sliding Mode Observation of capacitor voltage in multilevel power converters*. in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*.

Submitted Journal Papers

III. Almaleki, M., P. Wheeler, and J. Clare, *Sliding Mode Observation of capacitor voltage in multilevel power converters*. Industry Electronics, IEEE Transactions on

IV. Almaleki, M., P. Wheeler, and J. Clare, *Comparison of sliding mode observers and their application for multilevel power converters.* IET Power Electronics.

References

[1] Farhangi, H., *The path of the smart grid. Power and Energy Magazine*, IEEE. 8(1): p. 18-28.

[2] Puttgen, H.B., P.R. MacGregor, and F.C. Lambert, *Distributed generation: Semantic hype or the dawn of a new era?* Power and Energy Magazine, IEEE, 2003. 1(1): p. 22-29.

[3] Lopes, J.A., et al., *Integrating distributed generation into electric power systems: A review of drivers, challenges and opportunities*. Electric Power Systems Research, 2007. 77(9): p. 1189-1203.

[4] Bull, S.R., *Renewable energy today and tomorrow.* Proceedings of the IEEE, 2001. 89(8): p. 1216-1226.

[5] Atwa, Y.M., et al., *Optimal Renewable Resources Mix for Distribution System Energy Loss Minimization.* Power Systems, IEEE Transactions on. 25(1): p. 360-370.

[6] Bueno, E.J., et al., *A DSP- and FPGA-Based Industrial Control With High-Speed Communication Interfaces for Grid Converters Applied to Distributed Power Generation Systems.* Industrial Electronics, IEEE Transactions on, 2009. 56(3): p. 654-669.

[7] Carrasco, J.M., et al., *Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey*. Industrial Electronics, IEEE Transactions on, 2006. 53(4): p. 1002-1016.

[8] Bifaretti, S., et al. *Predictive current control of a 7-level AC-DC back-to-back converter for Universal and Flexible Power Management system. in Power Electronics and Motion Control Conference,* 2008. EPE-PEMC 2008. 13th. 2008.

[9] Roberts, B., *Capturing grid power*. Power and Energy Magazine, IEEE, 2009. 7(4): p. 32-41.

[10] http://www.eee.nottingham.ac.uk/uniflex/

[11] Clare, J. *Advanced power converters for universal and flexible power management in future electricity networks*. in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*. 2009.

[12] Rodriguez, J., L. Jih-Sheng, and P. Fang Zheng, *Multilevel inverters: a survey of topologies, controls, and applications.* Industrial Electronics, IEEE Transactions on, 2002. **49**(4): p. 724-738.

[13] McGrath, B.P. and D.G. Holmes. *Sinusoidal PWM of multilevel inverters in the overmodulation region*. in *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*. 2002.

[14] Jih-Sheng, L. and P. Fang Zheng, *Multilevel converters-a new breed of power converters.* Industry Applications, IEEE Transactions on, 1996. **32**(3): p. 509-517.

[15] Malinowski, M., et al., *A Survey on Cascaded Multilevel Inverters.* Industrial Electronics, IEEE Transactions on. **57**(7): p. 2197-2206.

[16] Holmes, D.G. and T.A. Lipo, *Pulse width modulation for power converters: principles and practice*. 2003: Wiley-IEEE Press.

[17] Mohan, N., T.M. Undeland, and W.P. Robbins, *Power electronics*. 1995: Wiley New York.

[18] http://www.mathworks.com

[19] Maharjan, L., S. Inoue, and H. Akagi, *A Transformerless Energy Storage System Based on a Cascade Multilevel PWM Converter With Star Configuration.* Industry Applications, IEEE Transactions on, 2008. **44**(5): p. 1621-1630.

[20] Akagi, H., S. Inoue, and T. Yoshii, *Control and Performance of a Transformerless Cascade PWM STATCOM With Star Configuration.* Industry Applications, IEEE Transactions on, 2007. **43**(4): p. 1041-1049.

[21] Akagi, H., Y. Kanazawa, and A. Nabae, *Instantaneous Reactive Power Compensators Comprising Switching Devices without Energy Storage Components.* Industry Applications, IEEE Transactions on, 1984. **IA-20**(3): p. 625-630.

[22] Rim, C.T., D.Y. Hu, and G.H. Cho, *Transformers as equivalent circuits for switches: general proofs and D/Q transformation-based analyses.* Industry Applications, IEEE Transactions on, 1990. **26**(4): p. 777-785.

[23] Soo-Bin, H., et al., *Modeling and analysis of static and dynamic characteristics for buck-type three-phase PWM rectifier by circuit DQ transformation.* Power Electronics, IEEE Transactions on, 1998. **13**(2): p. 323-336.

[24] Ogata, K., *Modern control engineering*. 2009: Prentice Hall.

[25] Inoue, S. and H. Akagi, *A Bidirectional DC/DC Converter for an Energy Storage System With Galvanic Isolation.* Power Electronics, IEEE Transactions on, 2007. **22**(6): p. 2299-2306.

[26] Luenberger, D.G., *Observing the State of a Linear System.* Military Electronics, IEEE Transactions on, 1964. **8**(2): p. 74-80.

[27] Luenberger, D., *An introduction to observers.* Automatic Control, IEEE Transactions on, 1971. **16**(6): p. 596-602.

[28] Boiko, I., *Frequency Domain Analysis of Accuracy of Sliding Mode Observers Under Imperfect Knowledge of Model Parameters.* Automatic Control, IEEE Transactions on, 2009. **54**(10): p. 2446-2450.

[29] Luenberger, D., *Observers for multivariable systems.* Automatic Control, IEEE Transactions on, 1966. **11**(2): p. 190-197.

[30] Price, M.G. and G. Cook, *Identification/Observation Using an Extended Luenberger Observer.* Industrial Electronics, IEEE Transactions on, 1982. **IE-29**(4): p. 279-287.

[31] Kaynak, O. and I.J. Rudas. *The fusion of computational intelligence methodologies in sliding mode control*. in *Industrial Electronics Society, 1998. IECON '98. Proceedings of the 24th Annual Conference of the IEEE*. 1998.

[32] Hung, J.Y., W. Gao, and J.C. Hung, *Variable structure control: a survey.* Industrial Electronics, IEEE Transactions on, 1993. **40**(1): p. 2-22.

[33] Madani-Esfahani, S.M., M. Hached, and S.H. Zak, *Estimation of sliding mode domains of uncertain variable structure systems with bounded controllers.* Automatic Control, IEEE Transactions on, 1990. **35**(4): p. 446-449.

[34] Young, K.-K.D., *Controller Design for a Manipulator Using Theory of Variable Structure Systems.* Systems, Man and Cybernetics, IEEE Transactions on, 1978. **8**(2): p. 101-109.

[35] Utkin, V., *Variable structure systems with sliding modes.* Automatic Control, IEEE Transactions on, 1977. **22**(2): p. 212-222.

[36] Young, K.D. and U. Ozguner. *Sliding mode: control engineering in practice*. in *American Control Conference, 1999. Proceedings of the 1999*. 1999.

[37] DeCarlo, R.A., S.H. Zak, and G.P. Matthews, *Variable structure control of nonlinear multivariable systems: a tutorial.* Proceedings of the IEEE, 1988. **76**(3): p. 212-232.

[38] Zak, S.H. and S. Hui, *On variable structure output feedback controllers for uncertain dynamic systems.* Automatic Control, IEEE Transactions on, 1993. **38**(10): p. 1509-1512.

[39] Walcott, B.L. and S.H. Zak, *Combined observer-controller synthesis for uncertain dynamical systems with applications.* Systems, Man and Cybernetics, IEEE Transactions on, 1988. **18**(1): p. 88-104.

[40] Slotine, J.J.E., J.K. Hedrick and E.A. Misawa, *On sliding observers for nonlinear systems.* Journal of Dynamic Systems, Measurement, and Control, 1987. **109**: p. 245-252.

[41] Utkin, V.I. *Application oriented trends in sliding mode control theory*. in *Industrial Electronics, Control, and Instrumentation, 1993. Proceedings of the IECON '93., International Conference on*. 1993.

[42] Utkin, V.I. and H. Lee. *The Chattering Analysis*. in *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*. 2006.

[43] Slotine, J.J.E., J.K. Hedrick, and E.A. Misawa. *On Sliding Observers for Nonlinear Systems*. in *American Control Conference, 1986.* 1986.

[44] Fridman, L.M., *Singularly perturbed analysis of chattering in relay control systems.* Automatic Control, IEEE Transactions on, 2002. **47**(12): p. 2079-2084.

[45] Slotine, J.J. and S.S. Sastry, *Tracking control of non-linear systems using sliding surfaces, with application to robot manipulators†*. International Journal of Control, 1983. **38**(2): p. 465-492.

[46] Lee, H. and V.I. Utkin, *Chattering suppression methods in sliding mode control systems.* Annual Reviews in Control, 2007. **31**(2): p. 179-188.

[47] Utkin, V., J. Guldner, and J. Shi, *Sliding Mode Control in Electromechanical Systems. 1999.* Taylar & Francis Ltd.

[48] Misawa, E.A. and J.K. Hedrick, *Nonlinear observers—A state-of-the-art survey*. Journal of dynamic systems, measurement, and control, 1989. **111**: p. 344-351.

[49] Haskara, I., *On sliding mode observers via equivalent control approach.* International Journal of Control, 1998. **71**(6): p. 1051-1067.

[50] Slotine, J.J.E., J.K. Hedrick, and E.A. Misawa. *Nonlinear state estimation using sliding observers*. in *Decision and Control, 1986 25th IEEE Conference on*. 1986.

[51] Yi, X. and M. Saif, *Sliding mode observer for nonlinear uncertain systems.* Automatic Control, IEEE Transactions on, 2001. **46**(12): p. 2012-2017.

[52] Ji, X., S. Hongye, and C. Jian. *On the design of Walcott-Zak sliding mode observer*. in *American Control Conference, 2005. Proceedings of the 2005*. 2005.

[53] Zak, S.H. and B.L. Walcott. *Variable structure observers*. in *Control and Applications, 1989. Proceedings. ICCON '89. IEEE International Conference on*. 1989.

[54] Walcott, B. and S. Zak, *State observation of nonlinear uncertain dynamical systems.* Automatic Control, IEEE Transactions on, 1987. **32**(2): p. 166-170.

[55] Walcott, B.L. and S.H. Zak, *Combined observer-controller synthesis for uncertain dynamical systems with applications.* Systems, Man and Cybernetics, IEEE Transactions on, 1988. **18**(1): p. 88-104.

[56] Walcott, B.L. and S.H. Zak. *Observation of dynamical systems in the presence of bounded nonlinearities/uncertainties*. *Decision and Control, 1986 25th IEEE Conference on*. 1986.

[57] Edwards, C. and S.K. Spurgeon, *Sliding mode control: theory and applications*. 1998: CRC.

[58] Koshkouei, A.J. and A.S.I. Zinober. *Sliding mode observers for a class of nonlinear systems*. in *American Control Conference, 2002. Proceedings of the 2002*. 2002.

[59] Drakunov, S. and V. Utkin. *Sliding mode observers. Tutorial*. in *Decision and Control, 1995., Proceedings of the 34th IEEE Conference on*. 1995.

[60] Drakunov, S.V. *Sliding-mode observers based on equivalent control method*. in *Decision and Control, 1992., Proceedings of the 31st IEEE Conference on*. 1992.

[61] Hashimoto, H., et al. *VSS observer for linear time varying system*. in *Industrial Electronics Society, 1990. IECON '90., 16th Annual Conference of IEEE*. 1990.

[62] Haskara, I., U. Ozguner, and V. Utkin. *On variable structure observers*. in *Variable Structure Systems, 1996. VSS '96. Proceedings., 1996 IEEE International Workshop on*. 1996.

[63] Slotine, J.J.E., *Sliding controller design for non-linear systems.* International Journal of Control, 1984. **40**(2): p. 421-434.

[64] Rohner, S.; Bernet, S.; Hiller, M.; Sommer, R.; , "*Modelling, simulation and analysis of a Modular Multilevel Converter for medium voltage applications*," *Industrial Technology (ICIT), 2010 IEEE International Conference on* , vol., no., pp.775-782, 14-17 March.

[65] Antonopoulos, A.; Ilves, K.; Ängquist, L.; Nee, H.-P.; , "*On interaction between internal converter dynamics and current control of high-performance high-power AC motor drives with modular multilevel converters*," *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE* , vol., no., pp.4293-4298, 12-16 Sept. 2010

[66] Rohner, S.; Bernet, S.; Hiller, M.; Sommer, R.; , "*Analysis and Simulation of a 6 kV, 6 MVA Modular Multilevel Converter*," *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE* , vol., no., pp.225-230, 3-5 Nov. 2009

[67] Antonopoulos, A.; Angquist, L.; Nee, H.-P.; , "*On dynamics and voltage control of the Modular Multilevel Converter*," *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on* , vol., no., pp.1-10, 8-10 Sept. 2009

[68] Lienhardt, A.-M.; Gateau, G.; Meynard, T.A.; , "*Digital Sliding-Mode Observer Implementation Using FPGA*," *Industrial Electronics, IEEE Transactions on* , vol.54, no.4, pp.1865-1875, Aug. 2007

[69] Chen, F.; Dunnigan, M.W.; , "*Comparative study of a sliding-mode observer and Kalman filters for full state estimation in an induction machine*," *Electric Power Applications, IEE Proceedings* - , vol.149, no.1, pp. 53- 64, Jan. 2002