Three-level Neutral-point-clamped Matrix Converter Topology

By

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Abstract

Matrix converter is a direct AC-AC converter topology that is able to directly convert energy from an AC source to an AC load without the need of a bulky and limited lifetime energy storage element. Due to the significant advantages offered by matrix converter, such as adjustable power factor, capability of regeneration and high quality sinusoidal input/output waveforms, matrix converter has been one of the AC – AC topologies that receive extensive research attention for being an alternative to replace traditional AC-DC-AC converters in the variable voltage and variable frequency AC drive applications.

Multilevel matrix converter is an emerging topology that integrates the multilevel concept into the matrix converter topology. Having the ability to generate multilevel output voltages, the multilevel matrix converter is able to produce better quality output waveforms than conventional matrix converter in terms of harmonic content, but at the cost of higher number of power semiconductor device requirement and more complicated modulation strategy.

In this research work an indirect three-level sparse matrix converter is proposed. The proposed converter is a hybrid combination between a simplified three-level neutral-point-clamped voltage source inverter concept and an indirect matrix converter topology. This multilevel matrix converter topology has a simpler circuit configuration and is able to generate three-level output voltages, making this topology an attractive option in industrial applications.

In this work a comprehensive simulation study is carried out to investigate the operation of the proposed converter. The performance of the proposed converter is compared to the conventional indirect matrix converter topology and a multilevel neutral-point-clamped matrix converter in order to identify the advantages and disadvantages offered by the proposed converter. A study of the semiconductor losses in the indirect three-level sparse matrix converter is also included. Finally, the operation of the proposed converter is experimentally validated using a laboratory prototype.

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Chapter 1

Introduction

1.1 Power Electronics

Power electronics is a technology that facilitates electrical energy conversion between source and load based on the combined knowledge of energy systems, electronics and control. Due to the different in nature of supply voltage and frequency (source) and the varying requirements of modern applications (loads), power conversion is essential in order to ensure a proper and energy efficient operation of equipment. As shown in Figure 1.1, a power electronic interface consists of a converter and a controller. The converter is an electronic circuit that is formed with high power handling semiconductor devices, energy storage elements and magnetic transformer. The conversion process begins when the controller, which is a low-power digital or analog electronic circuit, operates the switching devices in the converter according to a strategy that is specifically derived to control the stability and response characteristics of the overall system.

The development of power electronics has been closely related to the development of power semiconductor devices that capable of handling higher powers. The invention of the thyristor or silicon-controlled rectifier (SCR) by Bell laboratory in 1956, which was later commercially introduced by General Electric in 1958, marked the beginning of the modern power electronic era [3]. The rapid development of solid-state devices in terms of power rating, improved performance, cost and size has triggered the transition of power electronic from a ‘device-driven’ field to an ‘application-driven’ field [1]. This transition facilitates the extensive use of power electronics in a variety of electrical applications in industrial, commercial, residential, aerospace, military, utility, communication and transportation environments.

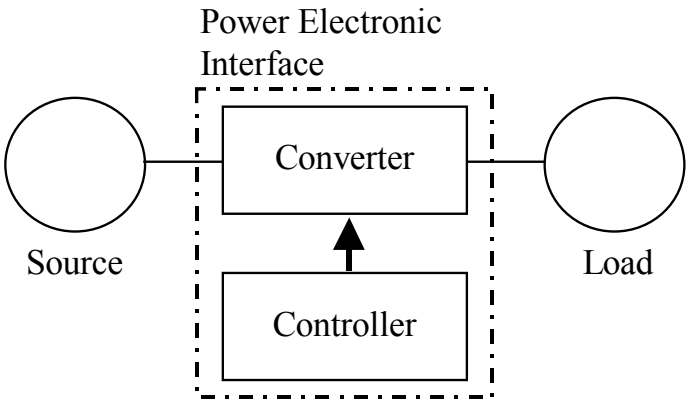


Figure 1.1: The power electronic interface between the source and the load [2]

Power conversions can be classified into four types, according to the input and output characteristics:

- DC – DC power conversion
  - ❖ for example, to convert an unregulated DC input voltage to a regulated variable DC output voltage.
- AC – DC power conversion (referred to as a rectifier)
  - ❖ for example, to convert an AC input voltage to a regulated, variable DC voltage.
- DC – AC power conversion (referred to as an inverter)
  - ❖ for example, to convert a fixed DC input voltage to a regulated AC voltage with variable amplitude and frequency.
- AC – AC power conversion
  - ❖ for example, to convert an AC input voltage to a regulated AC voltage with variable amplitude and frequency

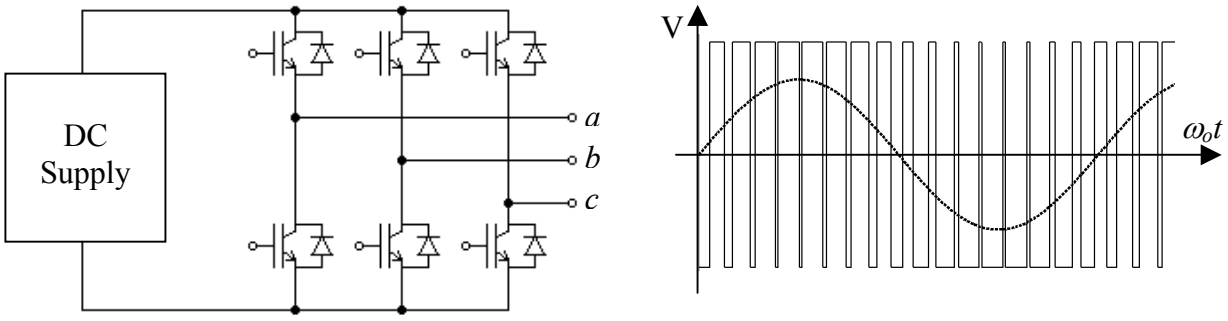
To achieve a high energy efficiency and high power density, modern power electronic systems often requires hybrid conversion; such as AC – DC – AC, DC – AC – DC, AC – AC – AC etc. Since the DC – AC and AC – AC power conversions constitute the foundation of this work, the following sections describe the concepts of these conversion techniques before discussing the motivation and objectives of this project.

1.2 DC – AC Power Conversion

As discussed earlier, a DC – AC power converter is referred to as an inverter. The distinctive feature of this converter is the ability to produce controllable sinusoidal AC output waveforms in terms of magnitude, frequency and phase from a DC power supply. Figure 1.2(a) shows the schematic diagram of a conventional three-phase two-level inverter. According to the type of DC power supply, the inverters can be classified into two types: voltage source inverter (VSI) and current source inverter (CSI). The power supply for a VSI is a voltage source while a CSI is supplied with a current source.

To generate AC output waveforms from a DC supply, switches of the inverter are turned on and off according to a sequence specified by a modulation strategy; such as carrier-based pulse-width modulation, space vector modulation or selective-harmonic-elimination modulation [1]. The output waveforms generated by the inverter are composed of discrete values with fast transition, as shown in Figure 1.2(b). Even though the output waveform is not sinusoidal, the fundamental component of the output waveform behaves as such. In order to generate sinusoidal output waveforms, the load characteristic for the inverter is a vital criterion. As an example, a VSI generates the output voltage waveforms composed of discrete values with fast transitions of *dv/dt*. To generate sinusoidal output currents, the loads for the VSI must be inductive. Capacitive loads should not be directly applied to the VSI because the fast transition of *dv/dt* can cause unwanted large current spikes.

The use of inverters is widely seen in medium voltage industrial applications; such as adjustable speed drives (ASD), uninterrupted power supplies and induction heating, where high quality output waveforms are required. In high voltage and high power applications, inverters can also be used to control reactive power and improve system

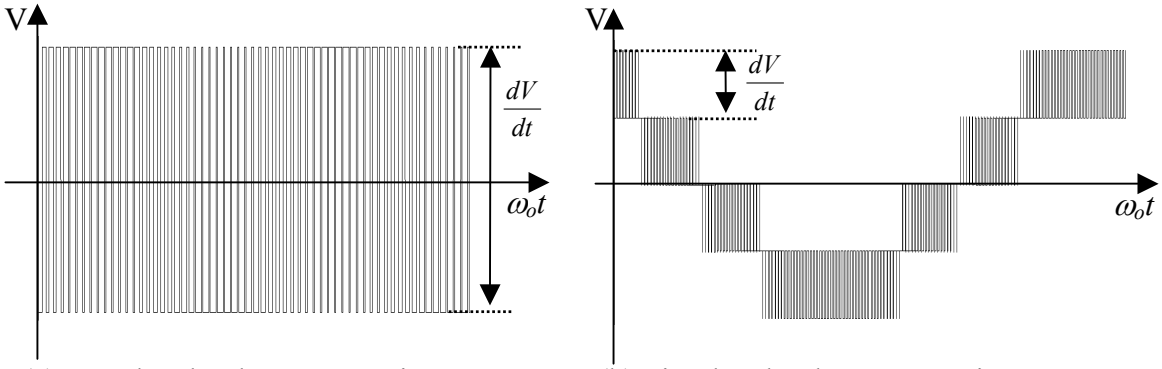


(a) (b)

Figure 1.2: (a) A conventional three-phase two-level inverter (b) The output voltage waveform generated by a voltage source inverter based on a pulse-width modulation (sinusoidal reference voltage is included)

stability [6]. However, the fast transition of *dv/dt* in the output voltage waveforms generated by the VSI has been reported causing motor bearing and winding isolation breakdown problems in ASD applications [4, 5]. Furthermore, due to the lack of semiconductor device with suitable power ratings, devices have to be series-connected in order to achieve the required high voltage operation. This connection creates difficulties in obtaining static and dynamic sharing of voltage stress across the semiconductor switches [9].

As a result, multilevel converter topologies have been developed to overcome the deficiencies of two-level VSI in medium and high voltage applications [6,7,8]. Multilevel converters are able to construct the output voltage waveforms with smaller voltage steps. Figure 1.3 shows the output voltage waveforms from a conventional two-level VSI and a five-level VSI. The output voltage waveform generated by a five-level VSI consists of multiple voltage steps with lower ΔV, which obviously imposes a lower stress than a two-level VSI on motor bearing and winding isolation. Besides that, by constructing the output waveforms with multiple voltage steps, the output waveforms clearly resemble the desired sinusoidal waveforms, the output harmonic distortion is improved. Multilevel converter structures enable the voltage stress across the power semiconductor devices to be decreased with the increase number of voltage levels, enabling the use of medium voltage rated semiconductor devices to construct the converters for high voltage, high power applications.



(a) Two-level voltage source inverter (b) Five-level voltage source inverter

Figure 1.3: Output terminal voltage waveforms

Nevertheless, multilevel converter topologies have some drawbacks: the high number of power semiconductor devices, complicated modulation strategies and the difficulty in balancing the capacitor voltages. Despite these drawbacks, multilevel converter topologies still receive extensive research attentions. The cost reductions in power semiconductor devices and the advancement in digital computation technology have enabled multilevel converter topologies to be more practical to implement. There are three types of multilevel converter topologies have been extensively published in the literature:

- ❖ Diode clamped multilevel converter [10,11]
- ❖ Flying capacitor multilevel converter [9]
- ❖ Cascaded H-bridge multilevel converter [12]

The concept of diode clamped multilevel converter topology provides the inspiration for this work, so the following section gives a brief overview of this topology.

1.2.1 Diode Clamped Multilevel Converter

The early interest in this multilevel power converter was triggered by the work of Nabae et al. in 1981 with the introduction of the three-level neutral-point-clamped inverter (NPC) topology [10]. The ability of the NPC topology to generate better output

performance in terms of harmonic content prompted the development of multilevel topology to higher number of voltage levels using the similar principle of clamping the intermittent levels with diodes [11]. Such multilevel structures are known as 'diode clamped multilevel inverters'. As shown in Figure 1.4, a *m*-level diode clamped inverter requires (*m*-1) series-connected capacitors in the DC-link, where each capacitor is charged to an equal potential. For a DC-link voltage, V_{DC}, the voltage level of each capacitor is $V_{DC}/2$ for a NPC and $V_{DC}/4$ for a five-level diode clamped inverter. Due to the connections of the clamping diodes, the voltage stress across the switching devices is limited to one capacitor voltage level. Therefore, by increasing the number of voltage levels, the voltage stress across the semiconductor switches in this multilevel structure can be reduced significantly.

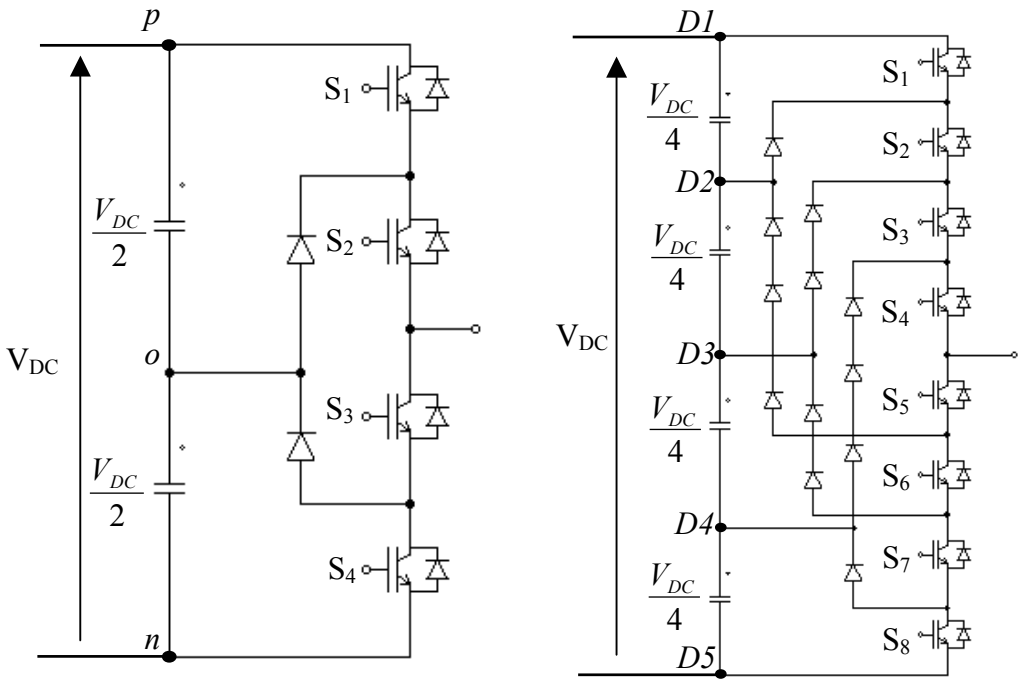
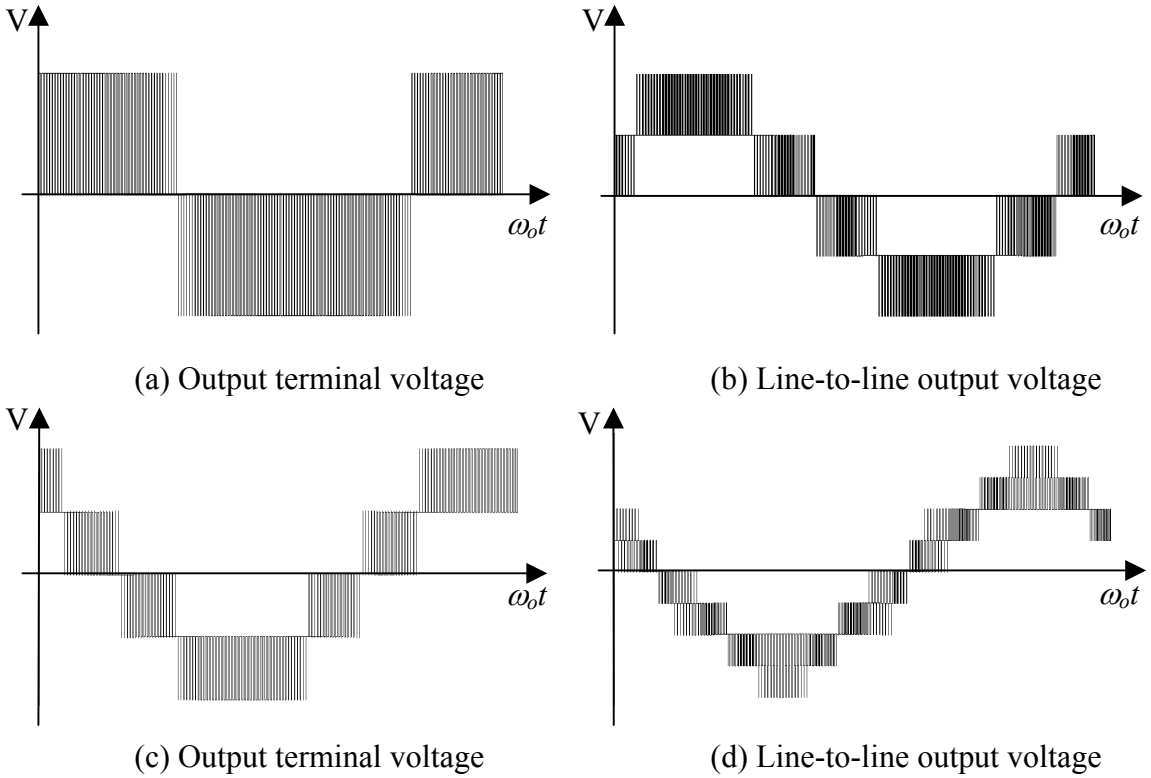


Figure 1.4: One output phase leg of a three-level neutral-point-clamped voltage source inverter (a) and a five-level diode-clamped inverter (b).

A *m*-level diode clamped inverter is able to generate *m*-level at the output terminals and (2*m* – 1)-level in the line-to-line output voltages. As shown in Figure 1.5, the increasing number of voltage levels clearly enables the output waveforms to resemble the desired sinusoidal waveform, which can reach a stage where the harmonic content is low enough to avoid the need for filters. Even though the converter has good harmonic distortion and low voltage stress across the power semiconductor switches, the diode clamped multilevel inverter is impractical when the number of voltage levels is higher than six [7]. This is because the required blocking capability of the clamping diodes increases proportionally to the number of voltage levels, requiring multiple series-connected clamping diodes in order to achieve the desired reverse voltage blocking [7,8]. The capacitor-balancing problem for the multilevel diode clamped converter also becomes more complicated with the increasing number of voltage levels, leading to system complexity and cost penalties [7,8].



(a) Output terminal voltage (b) Line-to-line output voltage

(c) Output terminal voltage (d) Line-to-line output voltage

Figure 1.5: The output voltage waveforms generated using carrier based multilevel pulse-width modulation (a)(b) three-level NPC (c)(d) five-level diode-clamped VSI

1.3 AC – AC Power Conversion

As discussed in Section 1.1, an AC – AC power converter is able to generate controllable sinusoidal AC outputs in terms of magnitude and frequency from an AC supply. Due to the increasing popularity of AC motors in industrial and commercial applications, AC – AC converters are used in the adjustable speed drive applications to control the rotation speed and torque of the AC motors. AC – AC converters can be divided into two types: indirect AC – AC converters and direct AC – AC converters.

1.3.1 Indirect AC – AC converter

Indirect AC – AC converter (also referred to as AC – DC – AC converter) is the most common approach for AC – AC power conversion. As shown in Figure 1.6, an indirect AC – AC converter topology consists of a rectifier at supply side and an inverter at the load side. The distinctive feature of this converter topology is the need of energy storage element in the intermediate DC-link: a capacitor (for a VSI) or an inductor (for a CSI). Due to low cost and control simplicity, the indirect AC – AC converter has been extensively used in industrial applications.

The most common design for an indirect AC – AC converter is the use of diode bridge rectifier at the supply side, as shown in Figure 1.6(a). The control of this converter is simple because of the naturally commutated characteristic of the diode bridge rectifier. However, this converter topology is notorious for high distortion in the input currents, which can cause detrimental effects to other electrical equipments using the same electrical supply [14]. In addition, the converter is not usable in applications requiring regenerative operation.

For applications that require regenerative operation, an active PWM rectifier (also known as an active front-end) is used to replace the diode bridge rectifier, as shown in Figure 1.6(b). The active PWM rectifier offers advantages of improved input current waveforms, improved total input power factor and bi-directional power flow [15]. However, by using the active PWM rectifier, the overall control of this indirect AC – AC converter is more complicated, when comparing this converter topology to the

diode bridge. The use of active devices also increases the losses, converter volume and cost.

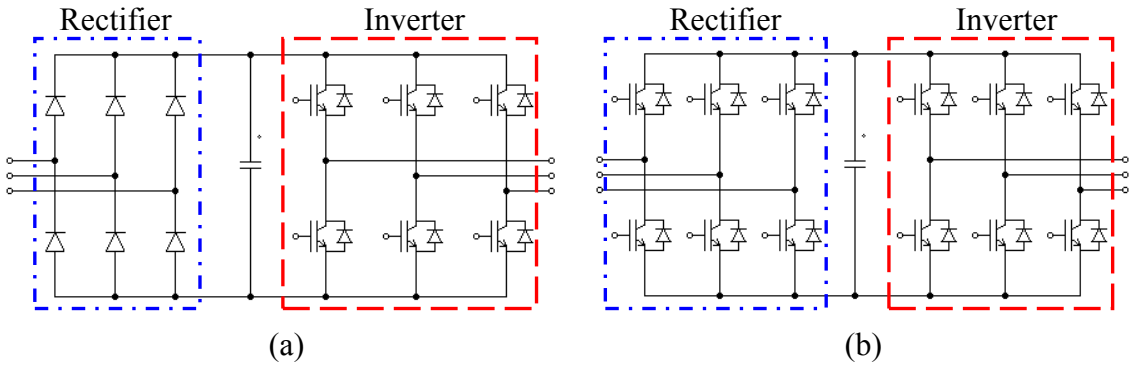


Figure 1.6: The indirect AC – AC converter (a) The diode bridge rectifier and a voltage source inverter (b) The back-to-back voltage source inverter

The main disadvantage of the indirect AC – AC converter topology is the need for a large energy storage element (e.g. electrolytic capacitor) in the DC-link. Compared to other electronic components, electrolytic capacitors have a shorter lifetime. As a result, the overall lifetime of the converter is reduced, leading to the increased maintenance cost. Also, the energy storage elements are bulky and unreliable at extreme temperatures, causing this converter topology to be inappropriate for some applications, such as aerospace applications where size, weight and system reliability are critical considerations. Even though the amount of DC-link energy storage can be reduced, as suggested in [16], the converter will become more susceptible to grid disturbances. In order to eliminate the need for DC-link energy storage, the direct AC – AC power conversion technology has gained significant research interest.

1.3.2 Direct AC – AC converter

The key feature of a direct AC – AC converter is the ability to directly perform AC – AC power conversion without the need of energy storage elements. The cycloconverter was the first direct AC – AC converter, this circuit is able to construct low frequency AC output voltage waveforms from successive segments of an AC supply of a higher frequency. However, due to the naturally commutated device characteristic, this

converter topology has limited output frequency range, poor input power factor and high distortion in input and output waveforms [17].

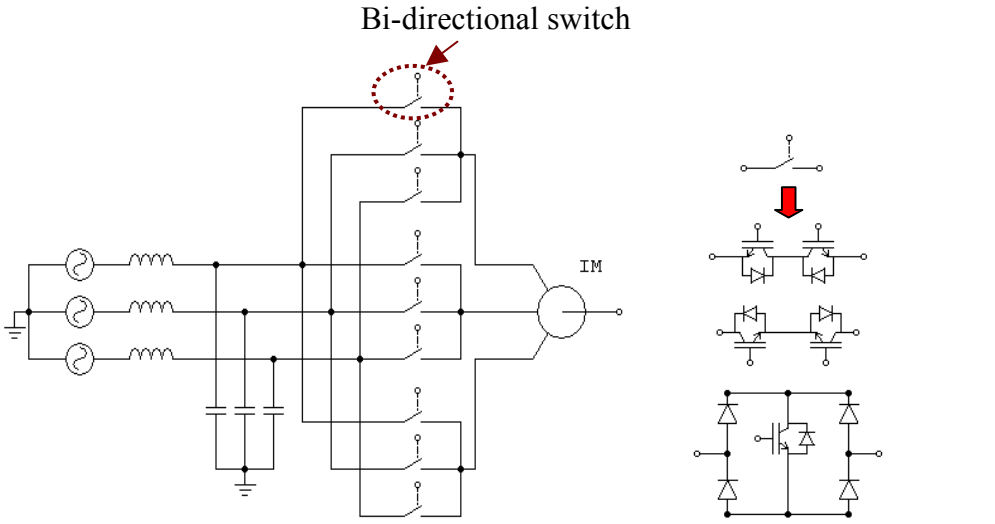
With the rapid development of fully controlled power semiconductor devices, a force-commutated cycloconverter or 'matrix converter' was developed as a promising technique for direct AC – AC power conversion [18]. Using the fully controlled bi-directional switches to directly connect the inputs to the outputs, the matrix converter topology is able to generate variable output voltages with unrestricted frequency from an AC voltage supply. The matrix converter is also able to generate sinusoidal supply currents and adjustable input power factor irrespective of the load. Most importantly, the removal of the DC-link energy storage element enables the matrix converter topology to have a more compact design, which is an advantage in applications such as aerospace [19].

Matrix converter topologies can be divided into two types: the direct matrix converter and the indirect matrix converter (also referred to as "dual bridge matrix converter [30]", "sparse matrix converter" [28] or "two-stage matrix converter [29]"). The circuit configuration of a conventional direct matrix converter with an array of 3 x 3 bi-directional switches is shown in Figure 1.7(a). By applying appropriate modulation strategy, such as Venturini method [21] or space vector modulation [22 – 26], the direct matrix converter is able to generate high quality sinusoidal input and output waveforms. The indirect matrix converter topology is the physical implementation of the indirect modulation method [27, 28]. As shown in Figure 1.7(c), the indirect matrix converter consists of a four-quadrant current source rectifier and a two-level voltage source inverter. This converter topology is able to produce input and output waveforms with the same quality as the direct matrix converter. In some applications, the indirect matrix converter may be preferred to the direct matrix converter due to simpler and safer commutation of switches [27], the possibility of further reducing the required number of power semiconductor switches [28,30] and the possibility to construct complex converter topology with multiple input and output ports [29].

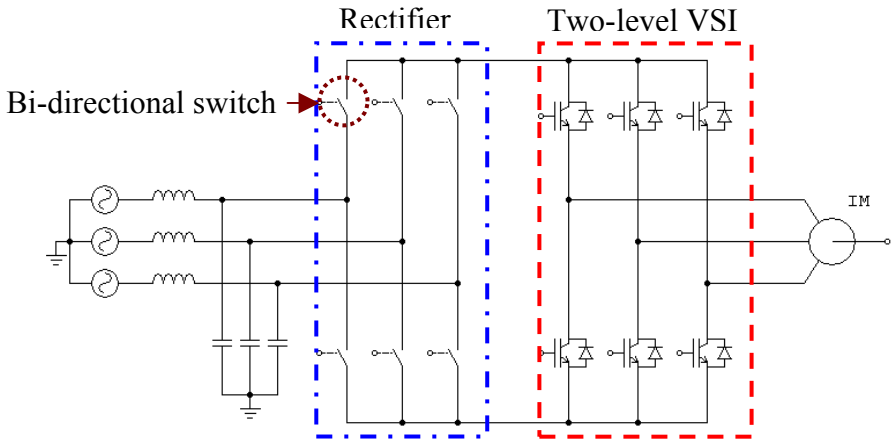
However, matrix converter topologies have some drawbacks. Besides requiring a high number of power semiconductor devices, the maximum load voltage of the matrix converter is limited to 86% of the supply voltage [21]. Having no energy storage element, the load side of the matrix converter is susceptible to supply side disturbances;

such as unbalanced supply voltages, voltage sags, dips, harmonics etc, leading to output voltage distortion and a reduction in the voltage transfer ratio.

Despite these drawbacks, the significant advantages of the matrix converter have encouraged extensive research into implementing the topology. Different techniques have been proposed [31 – 34] to maintain the load voltage quality and maximum voltage transfer ratio of the matrix converter topology even during the supply side disturbances. To overcome the voltage transfer ratio limitation, motors can be designed to reach nominal flux at the maximum voltage transfer ratio of the matrix converter [35].



(a) Direct matrix converter (b) Typical bi-directional switches



(c) Indirect matrix converter

Figure 1.7: Matrix converter topologies

1.4 Motivation and objectives of the project

The attractive features of the matrix converter have not only encouraged extensive research into solving the practical difficulties in the implementation of the topology but also generated interest in applying multilevel converter concepts to improve the output waveform quality. There are several types of multilevel matrix converter topologies have been proposed [36 – 42]. Having the ability to generate multilevel output voltages, the multilevel matrix converter is able to produce better quality output waveforms in terms of harmonic content; impose lower stress on motor bearings and winding isolation in adjustable speed drive applications as well as reducing the voltage stress across the devices in the converter. However, these benefits are achieved at the cost of more complicated circuit configurations and modulation strategies.

In order to make the multilevel matrix converter concept attractive in industrial applications, a simpler three-level matrix converter topology has been proposed in this work: the indirect three-level sparse matrix converter [44]. This multilevel matrix converter topology is a hybrid combination of a simplified three-level neutral-point-clamped voltage source inverter concept [43,44] and an indirect matrix converter topology. The indirect three-level sparse matrix converter has a simpler circuit configuration than the multilevel matrix converter topologies proposed in [36 – 42], but is still able to generate multilevel output waveforms.

In this work, the performance of the indirect three-level sparse matrix converter is compared with the conventional indirect matrix converter topology in order to show the advantages of applying multilevel concept. To investigate the extent of quality achievable by the converter, the indirect three-level sparse matrix converter is compared to another multilevel matrix converter topology: the three-level-output-stage matrix converter. The three-level-output-stage matrix converter is a multilevel matrix converter topology that applies a conventional three-level neutral-point-clamped voltage source inverter concept, shown in Figure 1.4(a), to the inversion stage of an indirect matrix converter topology [39]. This multilevel matrix converter topology has a much more complicated circuit configuration but is able to generate switching states that are not achievable by the indirect three-level sparse matrix converter. Due to concept similarity,

the performance of the three-level-output-stage matrix converter provides a benchmark used to evaluate the indirect three-level sparse matrix converter.

The main objectives of this project are to:

- derive modulation strategies for the three-level matrix converter topologies.
- investigate the output quality improvement offered by the three-level matrix converters when compared to the indirect matrix converter topology.
- compare the performance of the three-level matrix converters
- evaluate the efficiency of the three-level matrix converters.

1.5 Thesis plan

This thesis contains nine chapters, which addresses different aspects of the project objectives:

Chapter 1 is the introduction to the thesis. This chapter introduces the research motivation and outlines the main objectives of the project.

Chapter 2 gives a technology overview of the matrix converter topologies. This chapter discusses, in detail, the concept of the indirect matrix converter topology, the principles of the bi-directional switch, the switching commutation methods, the modulation techniques, the design of the input filter and the protection issues.

Chapter 3 gives a technology overview of the three-level neutral-point-clamped voltage source inverter. The operating principles and space vector modulations for the three-level neutral-point-clamped voltage source inverter are reviewed in this chapter. The neutral-point balancing problem of the converter and associated control methods are also discussed.

Chapter 4 discusses the operating principles and space vector modulation of the simplified three-level neutral-point-clamped voltage source inverter in order to provide

the foundation for the proposed modulation strategy for the indirect three-level sparse matrix converter.

Chapter 5 discusses the operating principles and modulation strategy for the three-level-output-stage matrix converter. Simulation results are presented to show the effectiveness of modulation strategy in controlling the converter. An output performance comparison between the three-level-output-stage matrix converter and the indirect matrix converter is shown to prove that the multilevel matrix converter topology is able to generate better quality output waveforms.

Chapter 6 discusses the operating principles and modulation strategy for the indirect three-level sparse matrix converter. Simulation results are shown to confirm the ability of the indirect three-level sparse matrix converter to generate multilevel output voltages. The performance of the indirect three-level sparse matrix converter is compared with the indirect matrix converter and the three-level-output-stage matrix converter to show that the indirect three-level sparse matrix converter has the advantages over these other topologies

Chapter 7 presents the hardware implementation and the experimental results from the three-level matrix converters. This chapter describes the overall structure of the prototype converter and explains the design of each circuit in detail. Then, experimental results from the prototypes of three-level matrix converters are shown to validate the simulation results.

Chapter 8 investigates the semiconductor losses in the three-level matrix converter topologies. Simulation models to calculate the conduction and switching losses in each multilevel matrix converter topology are described. Finally, the efficiency of the indirect three-level sparse matrix converter is determined and compared with the indirect matrix converter and three-level-output-stage matrix converter.

Chapter 9 contains the conclusion of the thesis. This chapter summarizes the work done and the main findings of the PhD research work. Possibilities for improving the investigated topologies are outlined for future work.

Chapter 2

Matrix Converter Topologies

2.1 Introduction

This chapter reviews current indirect matrix converter technology from converter topology derivation to hardware implementation. As discussed in Chapter 1, the indirect matrix converter is a physical implementation of the indirect modulation model applied to a conventional matrix converter. Hence, the matrix converter technology constitutes the foundation of this chapter and will be reviewed first. The operating principles and space vector modulation scheme for the indirect matrix converter are described. Details about the hardware implementation of the indirect matrix converter, such as bi-directional switches, commutation techniques and protection issues, are also discussed. The advantages of the indirect matrix converter over the direct matrix converter will be reviewed at the end of this chapter.

2.2 Direct Matrix Converter

2.2.1 Overview

Firstly introduced in 1976 [45], the matrix converter is a direct AC – AC converter that uses an array of m x n controlled bi-directional switches to directly connect m-phase inputs to n-phase outputs. The abilities of the bi-directional switch to conduct current in both directions and block voltage of both polarities enable a m x n phase ideal matrix converter to generate n-phase variable output voltages with unrestricted frequency from m-phase AC supply voltages. Figure 2.1 shows the circuit configuration of a conventional matrix converter with an array of 3 x 3 bi-directional switches. The three-phase to three-phase matrix converter has been extensively researched due to its potential as a replacement for the traditional AC-DC-AC converter in AC motor drives,

especially in aerospace applications [19]. Compared to a traditional AC-DC-AC converter, the matrix converter offers the following benefits:

- Adjustable input displacement factor, irrespective of the load
- The capability of regeneration (Four-quadrant operation)
- High quality input and output waveforms
- The lack of bulky and limited lifetime energy storage components, such as electrolytic capacitors.

Even though matrix converters have the disadvantage of limited voltage transfer ratio (0.86) and have a high number of power semiconductor devices requirement, these significant advantages have encouraged extensive research into solving the practical difficulties in the implementation of the matrix converter in industrial applications. In this chapter, only the operating principles and modulation schemes for the three-phase to three-phase direct matrix converter are reviewed, which is sufficient to understand the derivation of the indirect matrix converter topology.

As shown in Figure 2.1, the matrix converter allows any input line to be connected to any output line for any given length of time. Due to the direct connection with voltage sources, the input lines must never be shorted. If the switches cause a short circuit between the input voltage sources, infinite current flows through the switches and damages the circuit. Also, due to the inductive nature of typical loads, the output terminals must not be open-circuited. If any output terminal is open-circuited, the voltage across the inductor (and consequently across the switches) is infinite and switches will be damaged due to the over-voltage. As a result, switches for each output phase must be controlled based on the following expression:

$$S_{jA} + S_{jB} + S_{jC} = 1, \quad j \in \{a, b, c,\} \tag{2.1}$$

where S_{jk} is the switching function of a bi-directional switch, which is defined as:

$$S_{jk} \begin{cases} 1 & S_{jk} closed \\ 0 & S_{jk} opened \end{cases} \quad j \in \{a, b, c,\}\ ,\ k \in \{A, B, C\} \tag{2.2}$$

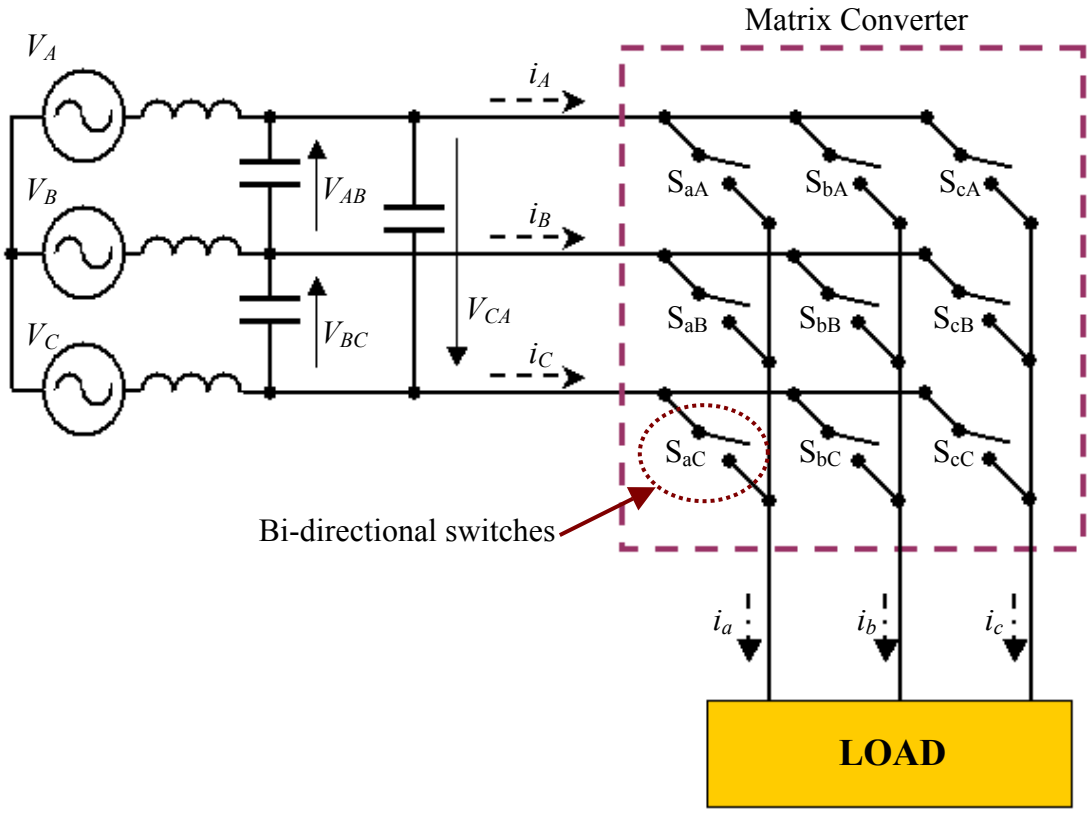


Figure 2.1 : Conventional three-phase to three-phase direct matrix converter

For a three-phase to three-phase matrix converter there are twenty-seven valid switching combinations available for generating specific input phase currents and output voltages that are presented in Table 2.1. The instantaneous values of the output voltages and the input currents generated by each switching combination can be determined using the instantaneous transfer matrices (2.3), where T_{LL} is the instantaneous input phase to output line-to-line transfer matrix and T_{Ph} is the instantaneous input phase to output phase matrix [25].

$$T_{LL} = \begin{bmatrix} S_{aA} - S_{bA} & S_{aB} - S_{bB} & S_{aC} - S_{bC} \\ S_{bA} - S_{cA} & S_{bB} - S_{cB} & S_{bC} - S_{cC} \\ S_{cA} - S_{aA} & S_{cB} - S_{aB} & S_{cC} - S_{aC} \end{bmatrix}, \quad T_{Ph} = \begin{bmatrix} S_{aA} & S_{aB} & S_{aC} \\ S_{bA} & S_{bB} & S_{bC} \\ S_{cA} & S_{cB} & S_{cC} \end{bmatrix} \tag{2.3}$$

Group	Switches On			Output line-to-supply neutral voltages			Line-to-line output voltages			Input phase currents		
	S_{ak}	S_{bk}	S_{ck}	V_a	V_b	V_c	V_{ab}	V_{bc}	V_{ca}	i_A	i_B	i_C
I	S_{aA}	S_{bB}	S_{cC}	V_A	V_B	V_C	V_{AB}	V_{BC}	V_{CA}	i_a	i_b	i_c
	S_{aA}	S_{bC}	S_{cB}	V_A	V_C	V_B	$-V_{CA}$	$-V_{BC}$	$-V_{AB}$	i_a	i_c	i_b
	S_{aB}	S_{bA}	S_{cC}	V_B	V_A	V_C	$-V_{AB}$	$-V_{CA}$	$-V_{BC}$	i_b	i_a	i_c
	S_{aB}	S_{bC}	S_{cA}	V_B	V_C	V_A	V_{BC}	V_{CA}	V_{AB}	i_c	i_a	i_b
	S_{aC}	S_{bA}	S_{cB}	V_C	V_A	V_B	V_{CA}	V_{AB}	V_{BC}	i_b	i_c	i_a
	S_{aC}	S_{bB}	S_{cA}	V_C	V_B	V_A	$-V_{BC}$	$-V_{AB}$	$-V_{CA}$	i_c	i_b	i_a
II $V_{ab} = 0$	S_{aA}	S_{bA}	S_{cB}	V_A	V_A	V_B	0	V_{AB}	$-V_{AB}$	$-i_c$	i_c	0
	S_{aA}	S_{bA}	S_{cC}	V_A	V_A	V_C	0	$-V_{CA}$	V_{CA}	$-i_c$	0	i_c
	S_{aB}	S_{bB}	S_{cA}	V_B	V_B	V_A	0	$-V_{AB}$	V_{AB}	i_c	$-i_c$	0
	S_{aB}	S_{bB}	S_{cC}	V_B	V_B	V_C	0	V_{BC}	$-V_{BC}$	0	$-i_c$	i_c
	S_{aC}	S_{bC}	S_{cA}	V_C	V_C	V_A	0	V_{CA}	$-V_{CA}$	i_c	0	$-i_c$
	S_{aC}	S_{bC}	S_{cB}	V_C	V_C	V_B	0	$-V_{BC}$	V_{BC}	0	i_c	$-i_c$
II $V_{bc} = 0$	S_{aB}	S_{bA}	S_{cA}	V_B	V_A	V_A	$-V_{AB}$	0	V_{AB}	$-i_a$	i_a	0
	S_{aC}	S_{bA}	S_{cA}	V_C	V_A	V_A	V_{CA}	0	$-V_{CA}$	$-i_a$	0	i_a
	S_{aA}	S_{bB}	S_{cB}	V_A	V_B	V_B	V_{AB}	0	$-V_{AB}$	i_a	$-i_a$	0
	S_{aC}	S_{bB}	S_{cB}	V_C	V_B	V_B	$-V_{BC}$	0	V_{BC}	0	$-i_a$	i_a
	S_{aA}	S_{bC}	S_{cC}	V_A	V_C	V_C	$-V_{CA}$	0	V_{CA}	i_a	0	$-i_a$
	S_{aB}	S_{bC}	S_{cC}	V_B	V_C	V_C	V_{BC}	0	$-V_{BC}$	0	i_a	$-i_a$
II $V_{ca} = 0$	S_{aA}	S_{bB}	S_{cA}	V_A	V_B	V_A	V_{AB}	$-V_{AB}$	0	$-i_b$	i_b	0
	S_{aA}	S_{bC}	S_{cA}	V_A	V_C	V_A	$-V_{CA}$	V_{CA}	0	$-i_b$	0	i_b
	S_{aB}	S_{bA}	S_{cB}	V_B	V_A	V_B	$-V_{AB}$	V_{AB}	0	i_b	$-i_b$	0
	S_{aB}	S_{bC}	S_{cB}	V_B	V_C	V_B	V_{BC}	$-V_{BC}$	0	0	$-i_b$	i_b
	S_{aC}	S_{bA}	S_{cC}	V_C	V_A	V_C	V_{CA}	$-V_{CA}$	0	i_b	0	$-i_b$
	S_{aC}	S_{bB}	S_{cC}	V_C	V_B	V_C	$-V_{BC}$	V_{BC}	0	0	i_b	$-i_b$
III	S_{aA}	S_{bA}	S_{cA}	V_A	V_A	V_A	0	0	0	0	0	0
	S_{aB}	S_{bB}	S_{cB}	V_B	V_B	V_B	0	0	0	0	0	0
	S_{aC}	S_{bC}	S_{cC}	V_C	V_C	V_C	0	0	0	0	0	0

Table 2.1: Valid switching combinations for a matrix converter

Based on the transfer matrix T_{LL}, the instantaneous output line-to-line voltages and the input phase currents can be determined, as given below:

$$V_{oll} = \begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = T_{LL} \cdot \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = T_{LL} \cdot V_i , \quad i_{iph} = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = {T_{LL}}^T \cdot \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} = {T_{LL}}^T \cdot i_{oll} \tag{2.4}$$

where ${T_{LL}}^T$ is the transpose of T_{LL}; V_{ab}, V_{bc} and V_{ca} are the output line-to-line voltages; V_A, V_B and V_C are the input phase voltages; i_{ab}, i_{bc} and i_{ca} are the output line-to-line currents; i_A, i_B and i_C are the input phase currents. Alternatively, by using the transfer matrix T_{Ph}, the instantaneous output line-to-supply neutral voltages (V_a, V_b and V_c) and the input phase currents can be found.

$$V_{oPh} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = T_{Ph} \cdot \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = T_{ph} \cdot V_i , \quad i_{iph} = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = {T_{Ph}}^T \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = {T_{Ph}}^T \cdot i_{oPh} \tag{2.5}$$

In order to generate a set of balanced, sinusoidal input and output waveforms, the matrix converter is controlled using the high frequency synthesis methodology, in which switches are operated at a high switching frequency (much higher than the input and output frequencies). Over each switching period, the modulation strategy modulates the duty cycles of the switches so that the input voltages and output currents are effectively applied to the output and input terminals, respectively, to generate the input and output waveforms which, on average, resemble the references. The switching function of each switch in (2.3) can then be replaced by a low frequency modulation function to achieve the required transformations.

$$0 \leq m_{jk} = \frac{t_{jk}}{T_{SW}} \leq 1, \quad j \in \{a, b, c\}, k \in \{A, B, C\} \tag{2.6}$$

where t_{jk} is the on time of switch S_{jk} and T_{SW} is the switching period. The low-frequency transfer matrices can be expressed as:

$$M_{LL} = \begin{bmatrix} m_{aA} - m_{bA} & m_{aB} - m_{bB} & m_{aC} - m_{bC} \\ m_{bA} - m_{cA} & m_{bB} - m_{cB} & m_{bC} - m_{cC} \\ m_{cA} - m_{aA} & m_{cB} - m_{aB} & m_{cC} - m_{aC} \end{bmatrix}, \; M_{ph} = \begin{bmatrix} m_{aA} & m_{aB} & m_{aC} \\ m_{bA} & m_{bB} & m_{bC} \\ m_{cA} & m_{cB} & m_{cC} \end{bmatrix} \quad (2.7)$$

The low-frequency components of the output voltages and the input phase currents can then be determined as:

$$\overline{V}_{oll} = M_{LL} \cdot V_i \qquad \overline{i}_{iph} = M_{LL}{}^{T} \cdot i_{oll}$$

$$\overline{V}_{oPh} = M_{Ph} \cdot V_i \qquad \overline{i}_{iph} = M_{Ph}{}^{T} \cdot i_{oPh} \quad (2.8)$$

Various modulation strategies have been proposed and each derived modulation strategy defines the value of each element (m_{jk}) within (2.7) differently. In the following section, the popular modulation strategies that have been proposed for the conventional matrix converter will be briefly reviewed in order to facilitate an explanation of the derivation of the indirect matrix converter topology.

2.2.2 Modulation strategies for the direct matrix converter

Since the matrix converter topology was first proposed, various modulation strategies have been suggested. In 1980, through detail mathematical analysis of the low-frequency behavior of a matrix converter, Alesina and Venturini proposed the first modulation strategy that determined the duty cycles for the switches, based on the derived mathematical solutions [20]. This strategy, also known as the direct transfer function approach, enables the converter to generate sinusoidal output voltages by sequentially applying the input voltages to respective output terminals for a calculated time during each switching period. However, the voltage transfer ratio achieved by this strategy is limited to 0.5 and the input displacement factor control depends on the output displacement factor. In [21], the Alesina and Venturini modulation strategy was optimized and the voltage transfer ratio is improved to 0.866, which is the intrinsic maximum of the matrix converter, by adding the third harmonics of the supply frequency and the output frequency to the reference output voltages.

Besides the Alesina and Venturini method, the scalar modulation technique proposed by Roy [46] is a conceptually different modulation technique that uses the measurements of supply voltages to calculate the 'on' intervals of the switches. Nevertheless, common mode addition is still required with this method in order to achieve the intrinsic maximum voltage transfer ratio of 0.866. Even though both modulation schemes are conceptually different, the performance of the scalar modulation strategy is similar to the optimized Alesina and Venturini method.

A modulation strategy proposed in [17,47] divides the modulation process of the matrix converter into two steps: rectification and inversion. Based on this technique (2.9), the input voltages V_i are 'rectified' (M_{REC}) to build up a constant virtual DC-link voltage. Then, based on this virtual DC-link voltage, the 'inversion' step (M_{INV}) generates the desired output voltages. This concept is known as indirect transfer function approach [48]. To maximize the voltage transfer ratio, the 'rectification' stage continuously selects the most positive and most negative input voltages in order to supply a maximum virtual DC-link voltage to the 'inversion' stage. A maximum voltage transfer ratio of 1.05 is achievable by this technique, but at the expense of low frequency distortion at both the input and output.

$$\overline{V_o} = M_{INV} \cdot \left(M_{REC} \cdot V_i \right) \tag{2.9}$$

Finally, space vector modulation (SVM) is probably the most popular technique due to its low complexity and high efficiency when implemented with modern digital technology. Since the introduction of space vectors in the analysis and control of the matrix converters in [49], a series of papers [22 – 26] about the SVM for the matrix converter have been published. The proposed SVM enables the matrix converters to have full control of the output voltages and the input displacement factor irrespective of the output displacement factor. SVM is a pulse-width modulation strategy that uses the concept of space vectors to compute the duty cycle for the switches. To implement this modulation strategy, the output voltages and input currents generated by each switching combination of the matrix converter, presented in Table 2.1, are converted into space vectors using the following transformation, where x_1, x_2 and x_3 are variables that represent the output voltages or input currents.

$$\bar{x} = \frac{2}{3}\left(x_1 + x_2 e^{j\frac{2}{3}\pi} + x_3 e^{-j\frac{2}{3}\pi} \right) \tag{2.10}$$

Among twenty-seven switching combinations for a three-phase matrix converter, only twenty-one switching combinations (Groups II and III) can be suitably applied in SVM. Table 2.2 shows the space vectors for the output line-to-supply neutral voltages (V_a, V_b and V_c) and the input phase currents (i_A, i_B and i_C) generated by the Groups II and III switching combinations. The Group I switching combinations cannot be used because each switching combination generates an output voltage vector and an input current vector that has variable directions, which are difficult to be applied for synthesizing the reference vectors. On the other hand, each switching combination from Group II can be transformed into an output voltage vector and an input current vector with fixed directions, as shown in Figures 2.2(a) and 2.2(b). These vectors are referred to as the 'active switching configurations' [26] and their magnitude depends upon the instantaneous values of the input line-to-line voltage and output phase current. For the Group III switching combinations, zero input current and zero output voltage vectors are formed and positioned at the origins of the space vector diagrams.

Based on the SVM for the matrix converter, the output voltage vector, $\bar{V}_{out}$, and the input current vector, $\bar{I}_{in}$, (for the input displacement factor control) are the reference space vectors, which are obtained by converting a set of sinusoidal and balanced output voltages and input currents using the space vector transformation (2.10). Until now, there have been two types of SVM proposed for the matrix converter: direct SVM [22 – 24] and indirect SVM [25]. Based on the direct SVM, the active switching configurations that can simultaneously synthesize the reference vectors, $\bar{V}_{out}$ and $\bar{I}_{in}$, are initially selected. Let us consider an example that the vectors $\bar{V}_{out}$ and $\bar{I}_{in}$ are located in sector 1, the selected active switching configurations are $\pm$1, $\pm$3, $\pm$7, $\pm$9. To synthesize the reference vectors, only four are required among these switching configurations. By using the duty cycle equations [26], the selection of either the positive or negative switching configuration from each pair and its respective duty cycle can be determined. For each switching period, $T_{SW,}$ the selected active switching configurations are applied for calculated intervals and then the zero vectors are used to complete the $T_{SW.}$

Alternatively, based on the indirect transfer function approach, the matrix converter is considered as a combination of a voltage source rectifier and a voltage source inverter [25]. SVM is applied to each stage independently, which produces a combination of vectors (two active vectors and a zero vector) to synthesize the reference vector ($\overline{V}_{out}$ for the inverter and $\bar{I}_{in}$ for the rectifier) of various amplitudes and angles. Based on the combinations of selected switching states from both stages, the equivalent switching state combinations, shown in Table 2.2, are applied to generate the desired input and output waveforms. This concept is known as indirect SVM. The results generated by this strategy are identical to the direct SVM but the modulation concept is simpler.

The indirect transfer function approach is the model that is used to derive the indirect matrix converter topology. The hardware implementation of the indirect matrix converter topology has been presented in [27,28]. Due to high efficiency when implemented with digital technology, SVM has been applied to the indirect matrix converter topology.

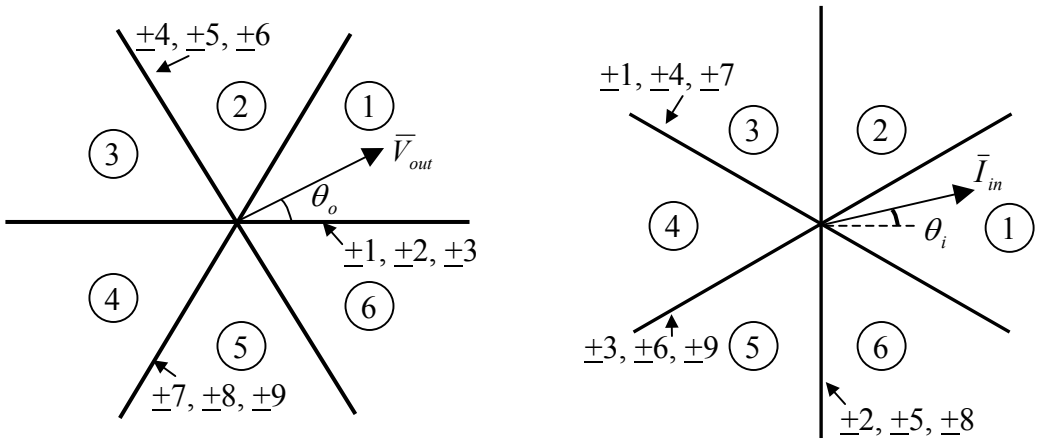
2.3 Indirect Matrix Converter

2.3.1 Overview

Derived from the indirect transfer function approach, the indirect matrix converter consists of a current source rectification stage and a voltage source inversion stage [50]. As shown in Figure 2.3, the rectification stage is a three-phase to two-phase matrix converter formed with six bi-directional switches so that the indirect matrix converter topology is able to perform the four-quadrant operation as the direct matrix converter. When the converter is in operation, the rectification stage sequentially connects the positive input voltage to the *p*-terminal and negative input voltage to the *n*-terminal of the DC-link to build a switching "DC-link voltage V_{pn}" for the inversion stage. Based on this "DC-link voltage", the inversion stage, which is a conventional two-level voltage source inverter, is modulated to generate the desired output voltages.

Switching Configuration	Switches On			Output Voltage Vector		Input Current Vector	
	S_{ak}	S_{bk}	S_{ck}	Magnitude	Angle	Magnitude	Angle
+1	S_{aA}	S_{bB}	S_{cB}	$(2/3)\ V_{AB}$	0	$(2/\sqrt{3})\ i_a$	$-\pi/6$
-1	S_{aB}	S_{bA}	S_{cA}	$-(2/3)\ V_{AB}$	0	$-(2/\sqrt{3})\ i_a$	$-\pi/6$
+2	S_{aB}	S_{bC}	S_{cC}	$(2/3)\ V_{BC}$	0	$(2/\sqrt{3})\ i_a$	$\pi/2$
-2	S_{aC}	S_{bB}	S_{cB}	$-(2/3)\ V_{BC}$	0	$-(2/\sqrt{3})\ i_a$	$\pi/2$
+3	S_{aC}	S_{bA}	S_{cA}	$(2/3)\ V_{CA}$	0	$(2/\sqrt{3})\ i_a$	$7\pi/6$
-3	S_{aA}	S_{bC}	S_{cC}	$-(2/3)\ V_{CA}$	0	$-(2/\sqrt{3})\ i_a$	$7\pi/6$
+4	S_{aB}	S_{bA}	S_{cB}	$(2/3)\ V_{AB}$	$2\pi/3$	$(2/\sqrt{3})\ i_b$	$-\pi/6$
-4	S_{aA}	S_{bB}	S_{cA}	$-(2/3)\ V_{AB}$	$2\pi/3$	$-(2/\sqrt{3})\ i_b$	$-\pi/6$
+5	S_{aC}	S_{bB}	S_{cC}	$(2/3)\ V_{BC}$	$2\pi/3$	$(2/\sqrt{3})\ i_b$	$\pi/2$
-5	S_{aB}	S_{bC}	S_{cB}	$-(2/3)\ V_{BC}$	$2\pi/3$	$-(2/\sqrt{3})\ i_b$	$\pi/2$
+6	S_{aA}	S_{bC}	S_{cA}	$(2/3)\ V_{CA}$	$2\pi/3$	$(2/\sqrt{3})\ i_b$	$7\pi/6$
-6	S_{aC}	S_{bA}	S_{cC}	$-(2/3)\ V_{CA}$	$2\pi/3$	$-(2/\sqrt{3})\ i_b$	$7\pi/6$
+7	S_{aB}	S_{bB}	S_{cA}	$(2/3)\ V_{AB}$	$4\pi/3$	$(2/\sqrt{3})\ i_c$	$-\pi/6$
-7	S_{aA}	S_{bA}	S_{cB}	$-(2/3)\ V_{AB}$	$4\pi/3$	$-(2/\sqrt{3})\ i_c$	$-\pi/6$
+8	S_{aC}	S_{bC}	S_{cB}	$(2/3)\ V_{BC}$	$4\pi/3$	$(2/\sqrt{3})\ i_c$	$\pi/2$
-8	S_{aB}	S_{bB}	S_{cC}	$-(2/3)\ V_{BC}$	$4\pi/3$	$-(2/\sqrt{3})\ i_c$	$\pi/2$
+9	S_{aA}	S_{bA}	S_{cC}	$(2/3)\ V_{CA}$	$4\pi/3$	$(2/\sqrt{3})\ i_c$	$7\pi/6$
-9	S_{aC}	S_{bC}	S_{cA}	$-(2/3)\ V_{CA}$	$4\pi/3$	$-(2/\sqrt{3})\ i_c$	$7\pi/6$
0_1	S_{aA}	S_{bA}	S_{cA}	0	-	0	-
0_2	S_{aB}	S_{bB}	S_{cB}	0	-	0	-
0_3	S_{aC}	S_{bC}	S_{cC}	0	-	0	-

Table 2.2: Switching combinations used in the space vector modulation [26]



(a) (b)

Figure 2.2: (a) Output line-to-supply neutral voltage vectors generated by the active switching configurations (b) The input line current vectors generated by the active switching configurations [26].

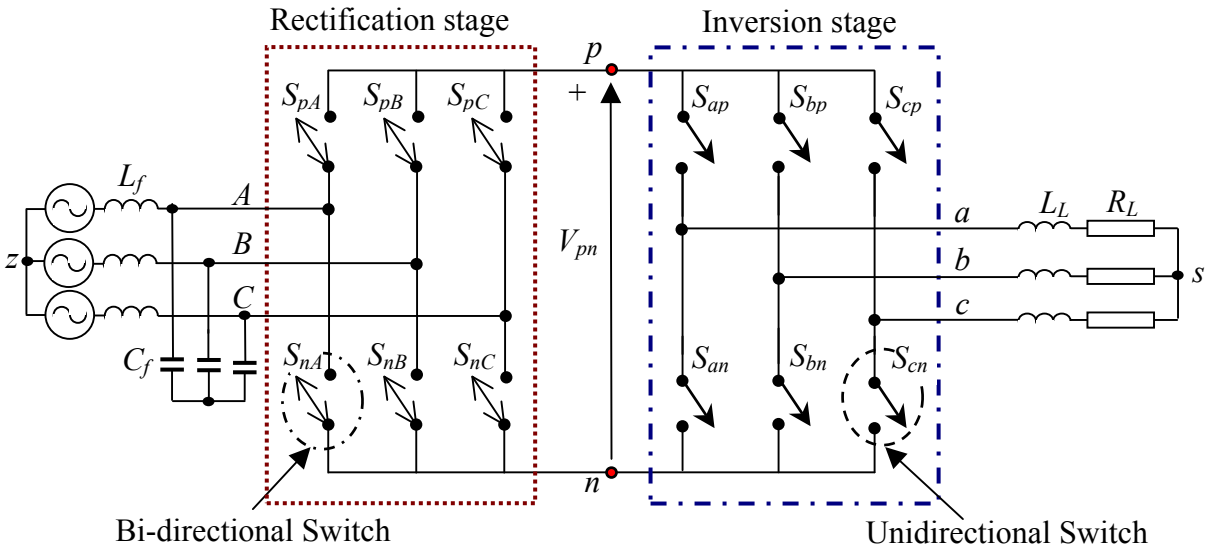


Figure 2.3: The schematic diagram of the indirect matrix converter topology

In [25], based on the mathematical analysis of the indirect transfer function approach, the ability of the indirect matrix converter to generate input and output waveforms with the same quality as those of a direct matrix converter has been demonstrated. This ability can also be explained with the instantaneous transfer matrix [51]. For instance, the instantaneous output phase voltages generated by the indirect matrix converter based on any switching combination can be determined using the instantaneous transfer matrix presented below:

$$V_{oPh} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} s_{ap} & s_{an} \\ s_{bp} & s_{bn} \\ s_{cp} & s_{cn} \end{bmatrix} * \begin{bmatrix} s_{pA} & s_{pB} & s_{pC} \\ s_{nA} & s_{nB} & s_{nC} \end{bmatrix} * \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = T_{INV} * T_{REC} * V_i \qquad (2.11)$$

where T_{INV} is the instantaneous transfer matrix of the inversion stage and T_{REC} is the instantaneous transfer matrix of the rectification stage. Let us consider an example based on the switching states given below:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} * \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}$$

According to T_{REC}, the rectification stage connects the input phase voltage V_A to the *p*-terminal while V_B is connected to the *n*-terminal of the DC-link, which generates a DC-link voltage $V_{pn} = V_{AB}$. Then, based on T_{INV}, the inversion stage applies the voltage V_A to the output terminals '*a*' and '*b*' and the voltage V_B to the terminal '*c*'. This switching combination generates the output voltages equivalent to the switching combinations of the direct matrix converter presented below (highlighted in Table 2.1):

$$\begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$$

As a result, any valid switching combination of the indirect matrix converter is actually equivalent to one of the Group II or Group III switching combinations presented in Table 2.1. By applying the SVM on each stage to synthesize the reference vector identical to the direct matrix converter, the generated input and output waveforms are equal to the direct matrix converter that is modulated using SVM.

2.3.2 Space vector modulation for the indirect matrix converter topology

In order to generate a set of balanced and sinusoidal input and output waveforms, the indirect matrix converter is modulated in such a way that the rectification stage and inversion stage are individually modulated using SVM. In each stage, SVM produces a combination of vectors to synthesize a reference vector. After determining the vectors and their duty cycles, the modulation pattern of the indirect matrix converter topology then combines the switching states from both stages uniformly so that a correct balance of the input currents and the output voltages is obtained for each switching period.

2.3.2.1 The rectification stage

To facilitate explanation, the rectification stage of the indirect matrix converter is firstly considered as a stand-alone current source rectifier. Due to the inductive nature of typical load and the high switching frequency operation, the output current, i_p, is assumed constant for each switching period. As a result, as shown in Figure 2.4, the

load of the rectifier can be assumed to be a DC current generator with a current of $i_p = I_{DC}$. At any instant, the switches of the rectifier are controlled so that the input lines must never be short-circuited:

$$S_{qA} + S_{qB} + S_{qC} = 1, \quad q \in \{p, n\} \tag{2.12}$$

where S_{qk} is the switching function of a bi-directional switch identical to (2.2). Table 2.4 presents all valid switching combinations of the rectifier and their generated voltages and currents. In order to generate input waveforms identical to the direct matrix converter, the rectifier not only generates the DC-link voltage V_{pn} but also has to maintain a set of sinusoidal and balanced input currents with controllable displacement angle with respect to the input voltages.

As mentioned earlier, SVM is applied to control the rectifier. By using the space vector transformation (2.10), the input currents generated by the first six switching combinations are transformed into six distinctive input current space vectors with fixed directions, as shown in Figure 2.5(a). Each current vector refers to the connections of the input phase voltages to the DC-link. For example, the current vector I_1 (AC) represents the connection of the input phase voltage V_A to the p-terminal and V_C to the n-terminal of the DC link. The magnitudes of the current vectors depend on the instantaneous value of the current i_p. For the last three switching combinations, the zero current vectors, I_0, are formed and positioned at the origin of the space vector diagram.

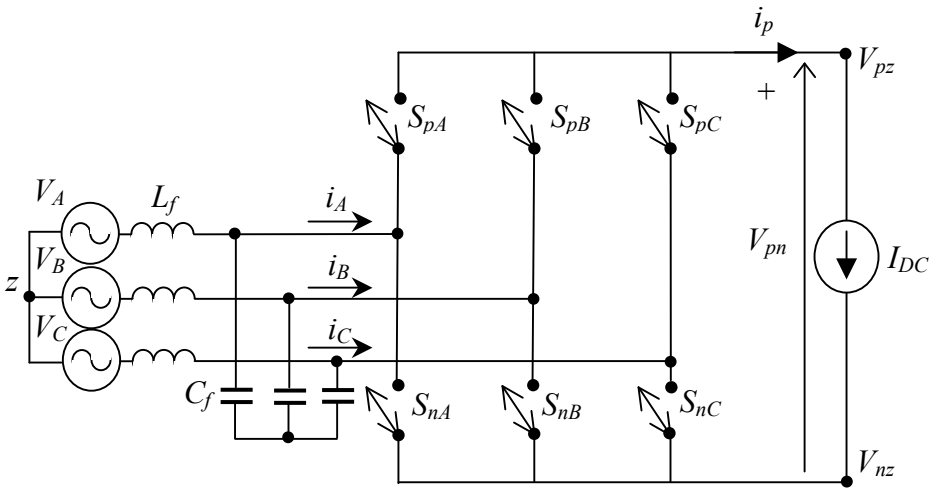


Figure 2.4: The current source rectifier loaded by a DC current generator

Switching State						Output Voltages			Input currents		
S_{pA}	S_{pB}	S_{pC}	S_{nA}	S_{nB}	S_{nC}	V_{pz}	V_{nz}	V_{pn}	i_A	i_B	i_C
1	0	0	0	0	1	V_A	V_C	V_{AC}	i_p	0	$-i_p$
0	1	0	0	0	1	V_B	V_C	V_{BC}	0	i_p	$-i_p$
0	1	0	1	0	0	V_B	V_A	V_{BA}	$-i_p$	i_p	0
0	0	1	1	0	0	V_C	V_A	V_{CA}	$-i_p$	0	i_p
0	0	1	0	1	0	V_C	V_B	V_{CB}	0	$-i_p$	i_p
1	0	0	0	1	0	V_A	V_B	V_{AB}	i_p	$-i_p$	0
1	0	0	1	0	0	V_A	V_A	0	0	0	0
0	1	0	0	1	0	V_B	V_B	0	0	0	0
0	0	1	0	0	1	V_C	V_C	0	0	0	0

Table 2.3: Valid switching combinations for the current source rectifier and its respective generated voltages and input currents (1 = ON and 0 = OFF)

To maintain a set of input currents with controllable displacement angle with respect to the input voltages, the input currents have to be synchronised with the input voltages. By using the space vector transformation, this set of input currents can be transformed into a reference input current space vector, $\bar{I}_{in}$, which can be expressed as:

$$\bar{I}_{in} = I_{im} e^{j(\omega_i t - \varphi_i)} = I_{im} \angle \theta_i \tag{2.13}$$

where I_{im} is the magnitude and θ_i is the direction of the reference vector. The variable, θ_i, is equal to $\omega_i t$ - φ_i, where $\omega_i t$ is the angle of the input voltages and φ_i is the displacement angle of the input currents with respect to the input voltages.

The space vector diagram of the rectifier, shown in Figure 2.5(a), is divided into six sectors. Based on SVM, the reference vector can be synthesized by two adjacent space vectors (I_γ and I_δ) and the zero-current vector, I_0, in a given sector demonstrated in Figure 2.5(b). The proportion between two adjacent vectors gives the direction and the zero vector controls the magnitude of the reference vector. For a switching period, T_{SW}, the reference vector can be synthesized as below:

$$\bar{I}_{in} = d_\gamma I_\gamma + d_\delta I_\delta \tag{2.14}$$

where d_γ and d_δ are the duty cycles for applying the vector I_γ and I_δ within the switching period. These duty cycles are calculated using the equations given below:

$$\begin{aligned} d_\gamma &= m_R \sin\left(\frac{\pi}{3} - \theta_{in}\right) \\ d_\delta &= m_R \sin\theta_{in} \end{aligned} \tag{2.15}$$

where m_R is the modulation index of the rectifier:

$$0 \le m_R = I_{im}/i_p \le 1 \tag{2.16}$$

and θ_{in} is the angle of the reference vector, $\bar{I}_{in}$, within the sector. By determining the duty cycles d_γ and d_δ, the duty cycle of the zero current vector, I_0, can be determined as

$$d_0 = 1 - d_\gamma - d_\delta \tag{2.17}$$

By applying SVM, the input currents generated by the current source rectifier consist of discrete values with fast transition of *di/dt*, as shown in Figure 2.6(a). The distortion of the input currents is high, which can cause the detrimental effects to other electrical equipment sharing the same electrical supply. In addition, due to the presence of inherent line inductance at the supply side, the fast transition of *di/dt* can cause unwanted large voltage spikes. Therefore, a low-pass LC filter is required at the supply side to filter out high frequency harmonics so that a set of sinusoidal and balanced input currents can be obtained (Figure 2.6b).

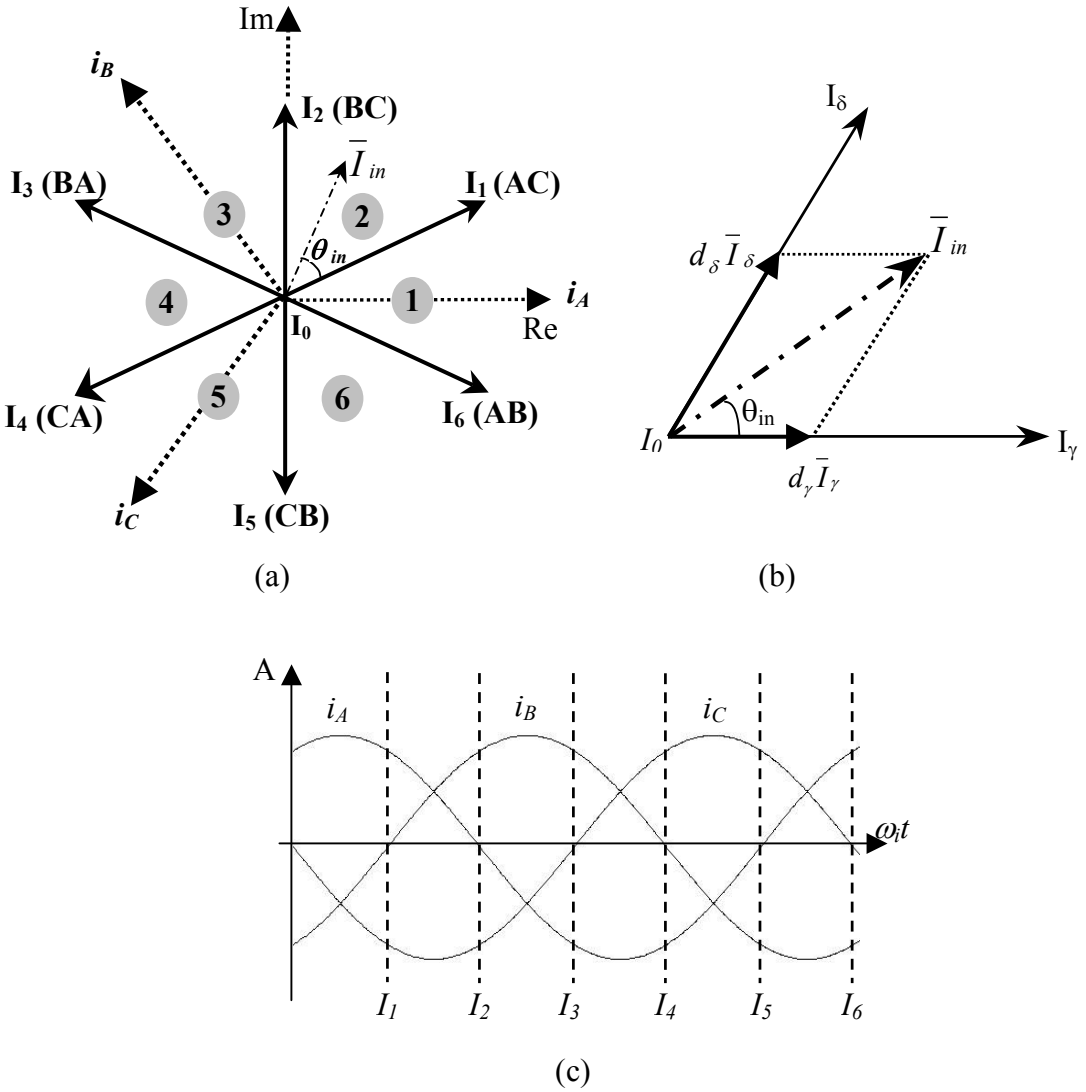


Figure 2.5: (a) The input current vectors formed by the valid switching combinations of the current source rectifier (b) To synthesis a reference vector in a given sector (c) The position of the input current vectors in the time domain of the input current waveforms.

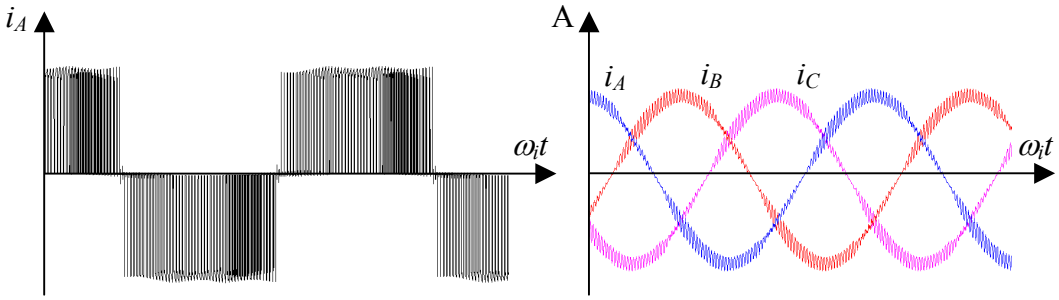


Figure 2.6 (a) The input current i_A generated by the current source rectifier based on the space vector modulation (b) The input current waveforms that are smoothed out by the low-pass LC filter

By obtaining the desired input current waveforms, the average of the DC-link voltage V_{pn}, generated by the current source rectifier, can be determined using the following equation:

$$V_{pn\_avg} = \frac{3}{2} * \hat{V}_{in} * m_R * \cos(\varphi_i) \tag{2.18}$$

where $\hat{V}_{in}$ is the peak amplitude of the input phase voltages. Based on (2.18), with the maximum input voltage supply, the current source rectifier can be modulated to generate maximum average DC-link voltage level, $V_{pn\_\max} = (3/2) * \hat{V}_{in}$, when the modulation index m_R = 1 and the displacement factor, φ_i, is controlled to zero. Figure 2.7 shows the DC-link voltage, V_{pn}, generated by the current source rectifier using space vector modulation scheme with m_R = 1 and φ_i = 0. The spikes to the zero voltage level in the waveform are due to the use of zero current vectors.

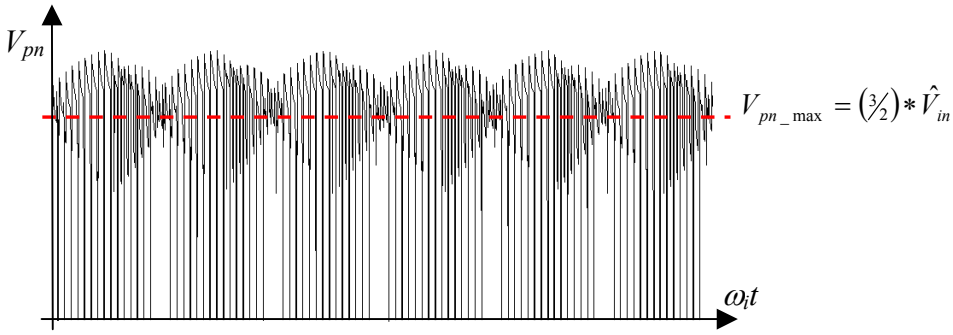


Figure 2.7: The "DC-link voltage V_{pn}" generated by the rectifier when m_R = 1 and φ_I = 0

2.3.2.2 The inversion stage

In the same way as for the rectification stage, to explain the operating principle, the inversion stage is initially considered as a stand-alone, three-phase, two-level voltage source inverter that supplied with a DC voltage source, $2*V_{DC}$ (Figure 2.8). Because of the balanced star-connected load ($i_a + i_b + i_c = 0$), the middle point '*o*' does not need to be physically present, but remains useful as a reference (ground) for the output voltages [13]. The switches of the voltage source inverter are modulated based on the constraint that the top and bottom switches of each phase leg must never be turned on simultaneously to prevent a short circuit. Hence, the switches of each phase leg are modulated based on the following expression:

$$S_{jp} + S_{jn} = 1 \qquad j \in \{a, b, c,\} \tag{2.19}$$

where S_{jp} and S_{jn} are the switching functions of the top and bottom unidirectional switches, respectively. There are eight valid switching combinations available for a three-phase voltage source inverter, as listed in Table 2.4. The output phase (line-to-output neutral-point *s*) voltages generated by the switching combination based on the DC-link voltage V_{pn} (= $2*V_{DC}$) can be determined using the following equations [13]:

$$\begin{aligned} V_{as} &= V_{pn}\left(\frac{2}{3}S_{ap} - \frac{1}{3}S_{bp} - \frac{1}{3}S_{cp}\right) \\ V_{bs} &= V_{pn}\left(\frac{2}{3}S_{bp} - \frac{1}{3}S_{ap} - \frac{1}{3}S_{cp}\right) \\ V_{cs} &= V_{pn}\left(\frac{2}{3}S_{cp} - \frac{1}{3}S_{ap} - \frac{1}{3}S_{bp}\right) \end{aligned} \tag{2.20}$$

By using space vector transformation (2.10), the output phase voltages generated by the first six switching combinations are transformed into six distinctive output voltage space vectors with fixed directions, as shown in Figure 2.9(a). Each voltage vector refers to the switching combination that represents the connections of the output terminals (*a*, *b* and *c*) to the DC-link terminals (*p* and *n*); e.g. V_1 (*PNN*) represents the

connection of the output terminal '*a*' to point '*p*' and the terminals '*b*' and '*c*' to point '*n*'. The magnitude of each voltage vector is proportional to the DC-link voltage V_{pn}. For the switching combinations that connect all output terminals to one DC-link point, zero voltage vectors V_0 are formed and positioned at the origin of the space vector diagram.

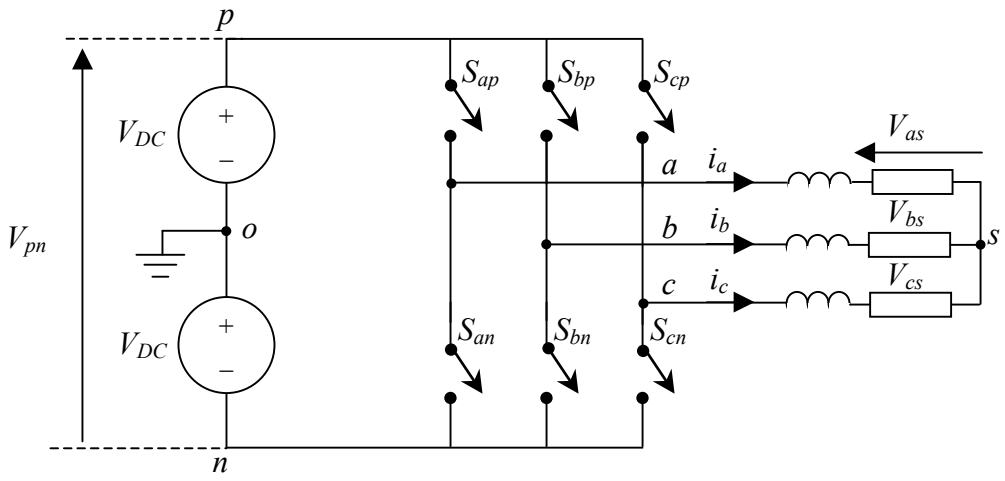


Figure 2.8: The circuit configuration of a three-phase two-level voltage source inverter

Switching Combinations						Output phase voltage		
S_{ap}	S_{bp}	S_{cp}	S_{an}	S_{bn}	S_{cn}	V_{as}	V_{bs}	V_{cs}
1	0	0	0	1	1	$(2/3)*V_{pn}$	$-(1/3)*V_{pn}$	$-(1/3)*V_{pn}$
1	1	0	0	0	1	$(1/3)*V_{pn}$	$(1/3)*V_{pn}$	$-(2/3)*V_{pn}$
0	1	0	1	0	1	$-(1/3)*V_{pn}$	$(2/3)*V_{pn}$	$-(1/3)*V_{pn}$
0	1	1	1	0	0	$-(2/3)*V_{pn}$	$(1/3)*V_{pn}$	$(1/3)*V_{pn}$
0	0	1	1	1	0	$-(1/3)*V_{pn}$	$-(1/3)*V_{pn}$	$(2/3)*V_{pn}$
1	0	1	0	1	0	$(1/3)*V_{pn}$	$-(2/3)*V_{pn}$	$(1/3)*V_{pn}$
1	1	1	0	0	0	*0*	*0*	*0*
0	0	0	1	1	1	*0*	*0*	*0*

Table 2.4: Valid switching combinations for the voltage source inverter and the generated output phase voltages (1 = ON, 0 = OFF)

For a three-phase voltage source inverter, a set of sinusoidal and balanced output phase voltages is the desired outputs. By using space vector transformation, this set of time-varying signals is transformed into a reference output voltage vector, $\overline{V}_{out}$, that rotates along a circular trajectory with the frequency ω_o in the space vector diagram. This reference vector can be expressed as:

$$\overline{V}_{out} = V_{om} e^{j(\omega_o t - \varphi_o)} = V_{om} \angle \theta_o \tag{2.21}$$

where V_{om} is the magnitude and θ_o is the direction of the reference vector. The variable, θ_o, is equal to $\omega_o t$ - φ_o, where $\omega_o t$ is the angle of the output phase voltages and φ_o is an arbitrary angle.

The space vector diagram of the voltage source inverter is divided into six sectors, as shown in Figure 2.9(a). The reference vector can be synthesized by two adjacent space vectors, V_α and V_β, and the zero voltage vector, V_0, in a given sector. For a switching period, T_{SW}, the output reference vector can be synthesized as below:

$$\overline{V}_{out} = d_\alpha V_\alpha + d_\beta V_\beta \tag{2.22}$$

The equations for determining the duty cycles d_α and d_β are:

$$\begin{aligned} d_\alpha &= m_I \sin\left(\frac{\pi}{3} - \theta_{out}\right) \\ d_\beta &= m_I \sin\theta_{out} \end{aligned} \tag{2.23}$$

where m_I is the modulation index of the voltage source inverter:

$$0 \le m_I = \sqrt{3}\, V_{om}/V_{pn} \le 1 \tag{2.24}$$

and θ_{out} is the angle of the reference vector, $\overline{V}_{out}$, within the sector. By calculating the duty cycles d_α and d_β, the duty cycle of the zero voltage vector, V_0, can be determined:

$$d_0 = 1 - d_\alpha - d_\beta \tag{2.25}$$

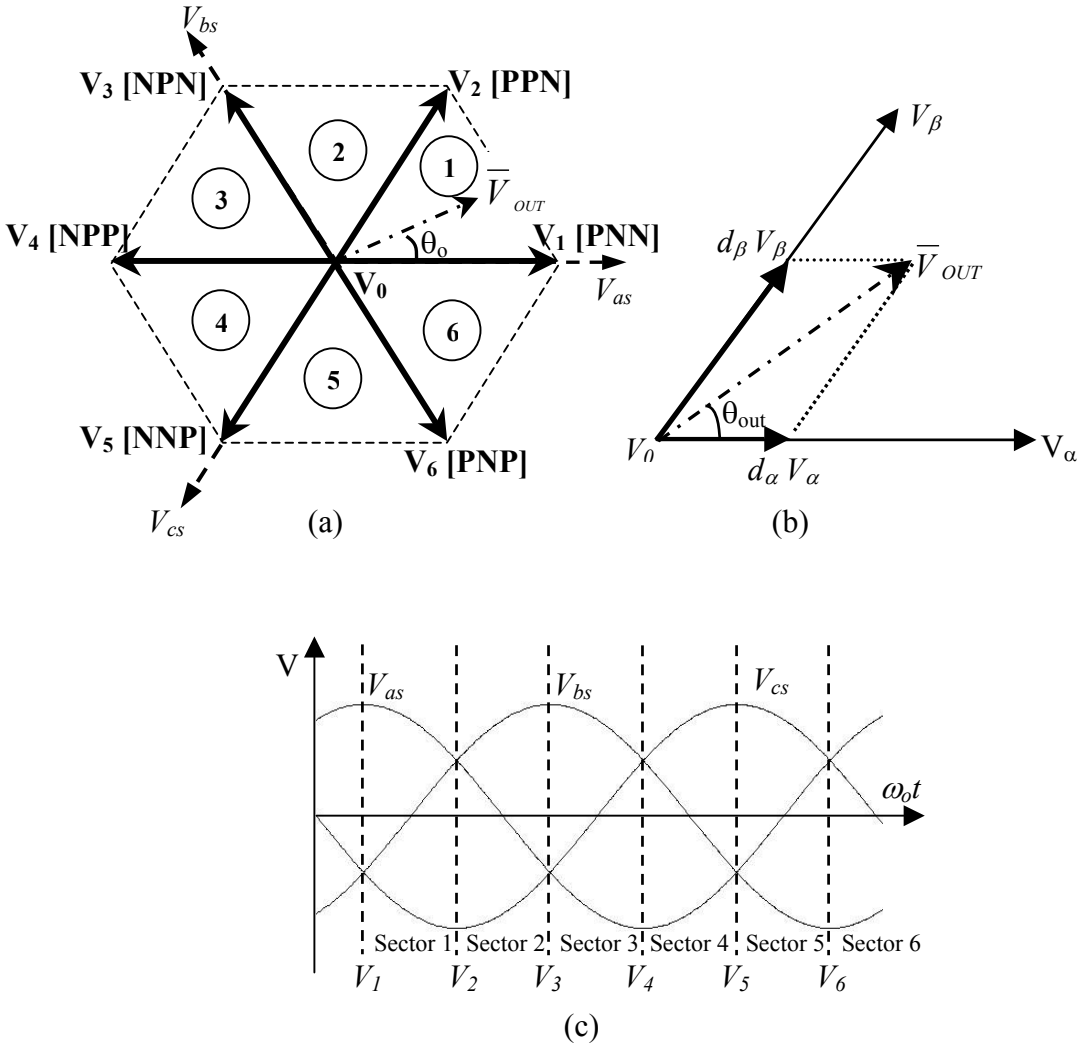
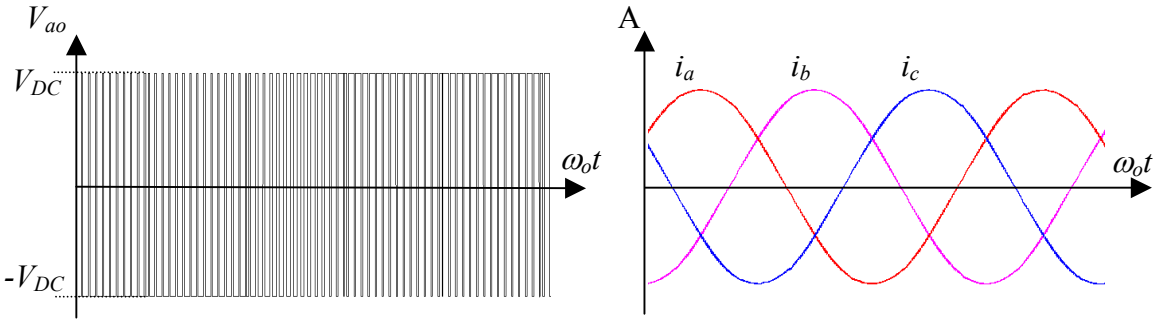


Figure 2.9: (a) The output voltage vectors formed by the valid switching combinations of the voltage source inverter (b) To synthesis a reference vector in a given sector (c) The position of the output voltage vectors in the time domain of the output phase voltage waveforms.

The output terminal (line-to-midpoint '*o*') voltages generated by a voltage source inverter consists of two discrete voltage levels ($+V_{DC}$ and $-V_{DC}$) with fast transition *dv/dt*, as shown in Figure 2.10(a). The inductive nature of typical loads generates smooth output currents, as shown in Figure 2.10(b).



(a) (b)

Figure 2.10: (a) The output line-to-midpoint voltage, V_{ao}, generated by the voltage source inverter using space vector modulation (b) Simulation result of the output currents

2.3.2.3 Synchronisation between the rectification and inversion stages

Using the modulation schemes applied to the rectification and inversion stages, this section describes the modulation pattern that combines the switching states from both stages in such a way that a correct balance of the input currents and the output voltages is obtained for each switching period.

For the indirect matrix converter topology, the rectification stage is modulated to supply maximum average DC-link voltage so that maximum overall voltage transfer ratio can be obtained. For this reason, the modulation index for the rectification stage, m_R, is set to unity and the displacement factor is controlled to zero. Besides that, to simplify the overall modulation, only the modulation on the inversion stage produces the zero vectors. Hence, the zero current vector of the rectification stage is eliminated and the rectification stage's switching sequence only consists of the two adjacent current vectors (I_γ and I_δ). By determining the duty cycles d_γ and d_δ (2.15) with the modulation index $m_R = 1$, the rectification stage's duty cycles are then adjusted using (2.26) to occupy the whole switching period.

$$d_\gamma{}^R = \frac{d_\gamma}{d_\gamma + d_\delta} \qquad d_\delta{}^R = \frac{d_\delta}{d_\gamma + d_\delta} \tag{2.26}$$

Due to the zero current vector cancellation, the average DC-link voltage is no longer constant (2.18) so this value needs to be recalculated using equation below:

$$V_{pn\_avg} = d_\gamma{}^R V_{l-l\gamma} + d_\delta{}^R V_{l-l\delta} \tag{2.27}$$

With the maximum DC-link voltage, V_{pn_avg}, supplied by the rectification stage, the modulation on the inversion stage controls the overall voltage transfer ratio. The maximum DC-link voltage, V_{pn_avg}, is applied in (2.28) to compensate the modulation index of the inversion stage, m_I:

$$m_I = \frac{\sqrt{3} * V_{om}}{V_{pn\_avg}} \tag{2.28}$$

By selecting the appropriate vectors and determining their duty cycles, the modulation pattern combines the switching states of the rectification stage (I_γ and I_δ) and the inversion stage (V_α, V_β and V_0) uniformly, producing a switching pattern shown in Figure 2.11. Considering an example where the vector $\overline{I}_{in}$ is located at sector 2 while the vector $\overline{V}_{out}$ is located at sector 1. The selected active current vectors for the rectification stage are I_1 (I_γ) and I_2 (I_δ) while the voltage vectors V_1 (V_α), V_2 (V_β) and V_0 are selected for the inversion stage.

To ensure the minimum switching transition between each vector, the selected voltage vectors are arranged in a double-sided switching sequence: $V_0 - V_2 - V_1 - V_0 - V_0 - V_1 - V_2 - V_0$, but with unequal halves because each half should apply on the rectifier switching sequence: $I_1 - I_2$. Referring to Figure 2.11, the time interval for each vector in this switching sequence can be determined using the following equations:

$$t_{r1} = d_\gamma^R * T_{sw} \tag{2.29}$$

$$t_{i1} = 0.5 * d_\gamma^R * d_0 * T_{sw} \tag{2.30}$$

$$t_{i2} = d_\gamma^R * d_\beta * T_{sw} \tag{2.31}$$

$$t_{i3} = d_{\gamma}^{R} * d_{\alpha} * T_{sw} \tag{2.32}$$

$$t_{i4} = 0.5 * d_{\delta}^{R} * d_{0} * T_{sw} \tag{2.33}$$

$$t_{i5} = d_{\delta}^{R} * d_{\alpha} * T_{sw} \tag{2.34}$$

$$t_{i6} = d_{\delta}^{R} * d_{\beta} * T_{sw} \tag{2.35}$$

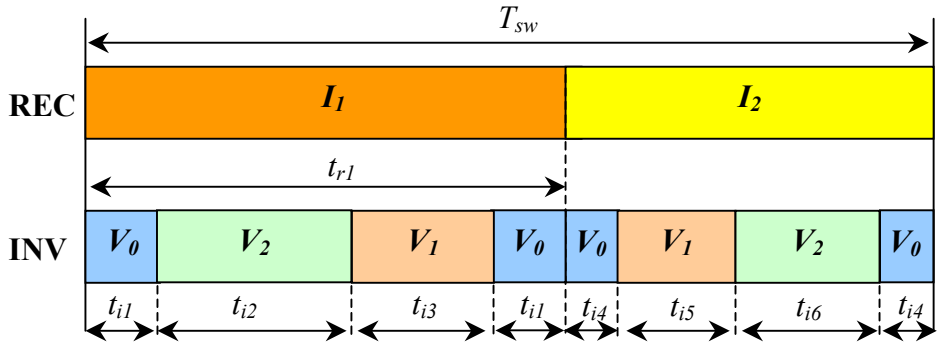


Figure 2.11: The switching pattern of the indirect matrix converter

2.3.2.4 Simulation results of the indirect matrix converter

The model of the indirect matrix converter shown in Figure 2.3 has been simulated using SABER, based on the specifications presented in Appendix A. Figure 2.12 presents the waveforms generated by the rectification stage (Figures 2.12(a) – 2.12(d)) and the inversion stage (Figures 2.12(e) – 2.12(g)) of the indirect matrix converter using space vector modulation. Referring to Figure 2.12(b), similar to the stand-alone rectifier (Figure 2.6a), the input current has significant high frequency distortion. By using a low-pass LC filter, the switching frequency harmonics are filtered out so that a set of sinusoidal, balanced input currents is obtained at the supply side, as shown in Figure 2.12(c). Due to the zero-current vector cancellation, the DC-link voltage generated by the rectification stage does not consist of the zero voltage levels so the average value of the DC-link voltage, V_{pn_avg}, is not constant, which is clearly shown in Figure 2.12(d).

By building the DC-link voltage with chops of the input line-to-line voltages, the output terminal (line-to-supply neutral) voltage, V_a, of the indirect matrix converter topology

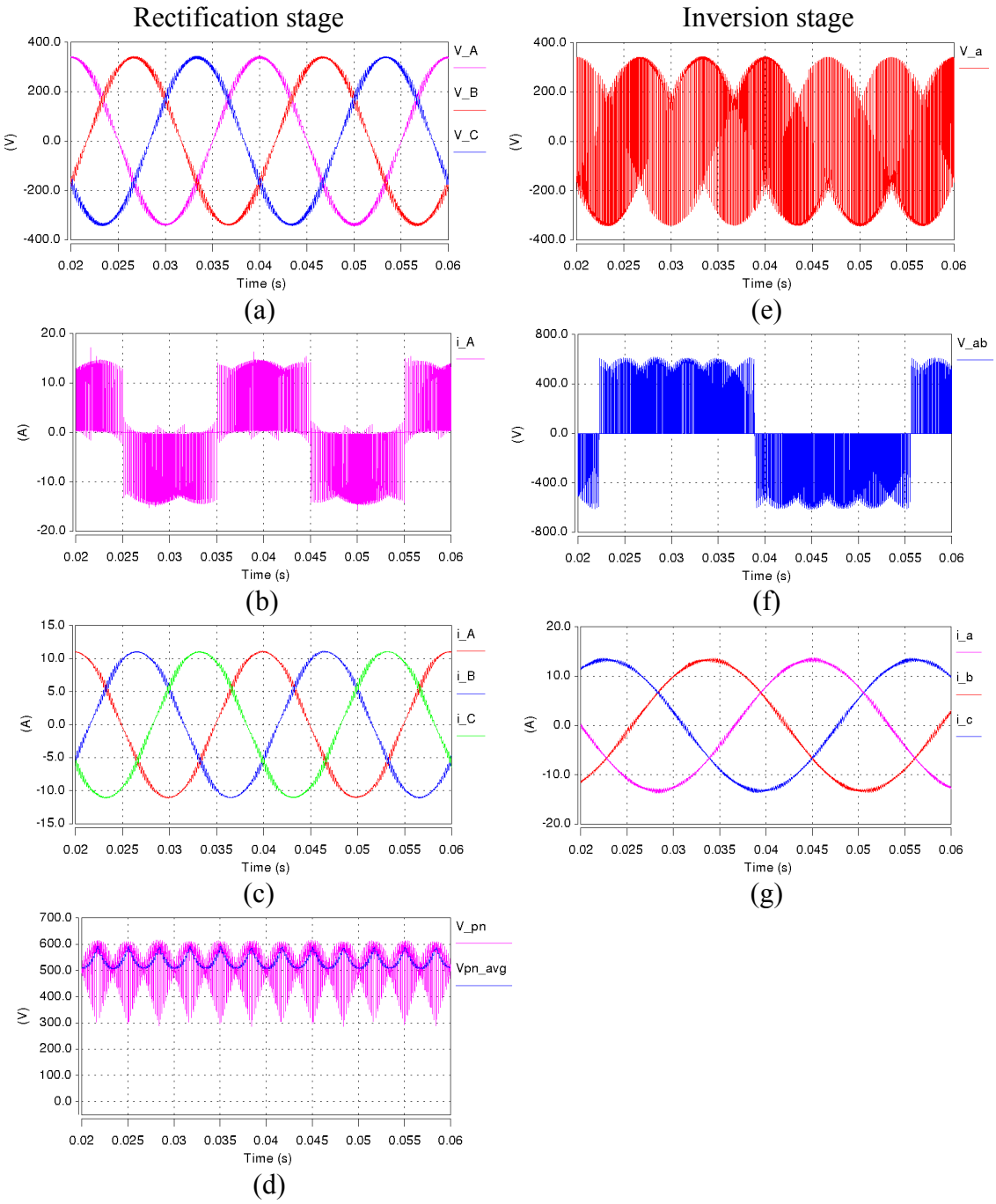


Figure 2.12: (a) The input phase voltage supplies (b) unfiltered input current, i_A (c) the filtered input currents (i_A, i_B and i_C) (d) The DC-link voltage, V_{pn} (e) the output terminal voltage, V_a (f) the line-to-line output voltage, V_{ab} (g) the output currents (i_a, i_b and i_c)

(Figure 2.12e) is obviously generated with the voltage levels within the envelope of the input voltages. For each switching period, the output terminal voltage consists of two voltage levels (V_{pz} and V_{nz}), which are the input voltages connected to the DC-links. As shown in Figure 2.12(f), the inversion stage is able to generate the three-level line-to-line output voltage. Finally, the input (Figure 2.12(c)) and output current waveforms (Figure 2.12(g)) of the indirect matrix converter evidently prove the ability of SVM to perform sine-wave-in/sine-wave-out operation.

2.4 Hardware Implementation of the Indirect Matrix Converter

2.4.1 Bi-directional Switches

As shown in Figure 2.3, the inversion stage of the indirect matrix converter topology is a three-phase voltage source inverter that is formed with six unidirectional switches, made from thyristors, transistors, GTOs, IGBTs or MOSFETs. With a freewheeling diode connected in an anti-parallel arrangement, each switch cell conducts current in both directions but blocks voltage of single polarity.

In order to perform four-quadrant operation as the direct matrix converter, the indirect matrix converter requires bi-directional switches that are capable of blocking voltage and conducting current in both directions for the rectification stage. Unfortunately, there is currently no such device available to fulfill these requirements so discrete devices are used to construct the desired switch cell. There are four types of bi-directional switch arrangements commonly known for the matrix converter. Only the bi-directional switch cells that are constructed using the IGBTs are shown in Figure 2.13, but other devices such as MOSFETs, MCTs, IGCTs can also be used for the same arrangements.

The first bi-directional switch cell arrangement is an IGBT connected at the center of a single-phase diode bridge [17], as shown in Figure 2.13(a). This arrangement only requires a single IGBT to carry current in both directions so only one gate drive circuit is required per switch cell, which is a major advantage. However, having three semiconductor devices in each conduction path, the device conduction losses are relatively high for this arrangement when compared to other arrangements.

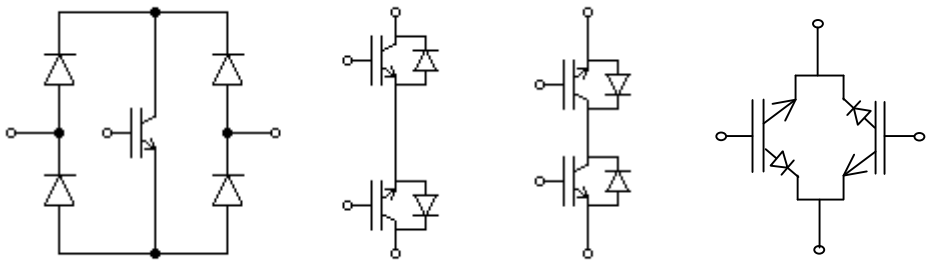


Figure 2.13: Bi-directional switch arrangements (a) Diode bridge (b) Common emitter back-to-back (c) Common collector back-to-back (d) anti-paralleled reverse blocking IGBTs

The common emitter bi-directional switch cell consists of two diodes and two IGBT switches that are connected in an anti-parallel arrangement, as shown in Figure 2.13(b). The diodes are needed to provide the reverse voltage blocking capability and the use of two IGBTs enables the independent control of the current direction. Compared to the diode-bridge arrangement, this arrangement requires only two devices to conduct current at any instant, so the conduction losses are lower. One possible disadvantage is the requirement for two gate drive circuits to operate the IGBTs. Due to its common emitter arrangement, one isolated power supply is required for each bi-directional switch cell. Hence, by using the common emitter bi-directional switch cells to construct the rectification stage, six isolated power supplies are required.

Alternatively, the common collector bi-directional switch cell, presented in Figure 2.13(c), is another arrangement that has the same conduction losses as the common emitter configuration due to the identical number of discrete devices. By using common collector bi-directional switch cells to construct the rectification stage, the number of isolated power supplies required for the gate drive circuits can be reduced to five [52].

Finally, the anti-paralleled reverse blocking IGBTs (RB-IGBT) arrangement, shown in Figure 2.13(d), can further reduce the number of discrete devices required in the constructing of a bi-directional switch cell [53]. The main feature of the RB-IGBT is its reverse voltage blocking capability, which eliminates the use of diodes. At any instant, there is only one device conducting current in any direction so the conduction losses are

lower than any other arrangement [53,54]. However, the switching losses can be higher due to the poor switching behavior of the intrinsic diode.

2.4.2 Commutation techniques for the indirect matrix converter

Due to the non-ideal switching characteristic of the devices, there is a delay in switching especially during turn-off. This delay can cause two switching devices, which are changing states, to be 'on' simultaneously and cause a short-circuit. As a result, a large current flows through the switch and damages the circuit. In order to ensure the safe switching, a specific commutation technique is required. For the indirect matrix converter topology, each stage requires different commutation technique due to the use of different circuit configurations.

For the inversion stage, having a freewheeling diode connected in anti-parallel with each switching device, a current path is always available for discharging the energy stored in the load even no device is gated. Hence, the dead time commutation technique can be applied to commutate the current in each phase leg. A time gap is introduced between the outgoing switch and the incoming switch. This time gap is referred as the 'dead time' because both switches are 'off' during this interval. This technique prevents a DC-link short-circuit during a change of switching states.

However, to commutate the current in the bi-directional switch cells of the rectification stage, a complex commutation strategy is required due to the lack of any natural freewheeling path. As discussed previously, the rectification stage is a three-phase to two-phase matrix converter, where the input lines must never be short-circuited and the output lines must never be open-circuited. Even though the dead time commutation technique can still be applied, additional circuitry, such as snubbers or clamping devices, are required across the switches, which further complicates the converter design and increases the cost and volume [52, 55, 56]. As the bi-directional switch cell shown in Figures 2.13(b) and 2.13(c) are commonly used in matrix converter topologies, the following sections describe the four-step commutation strategies that are applied to these configurations: the output current direction based commutation technique [57] and the relative input voltage magnitude based commutation technique [58]. A two-phase to single-phase matrix converter constructed with common emitter

bi-directional switch cells (Figure 2.14) is used to explain the principles of both commutation strategies.

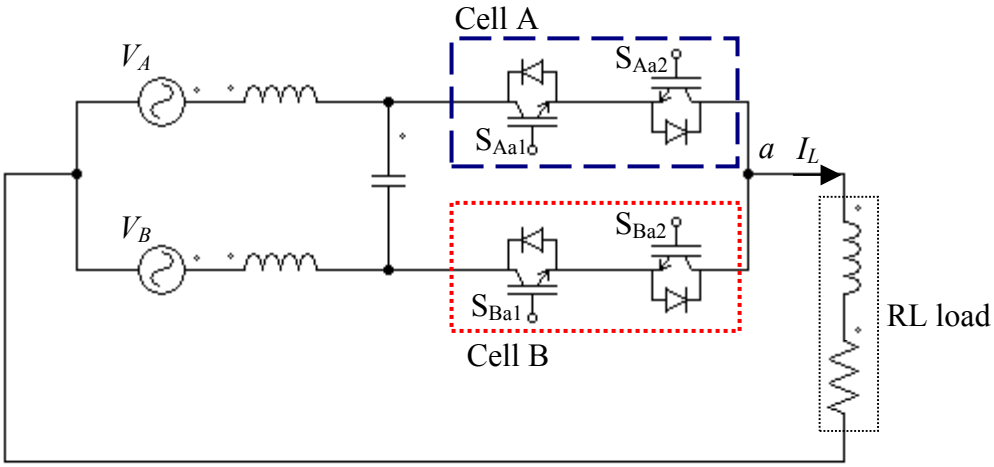


Figure 2.14: A two-phase to single-phase matrix converter

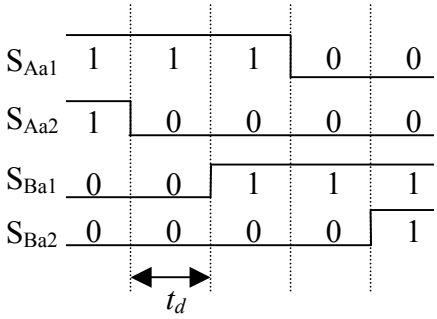
2.4.2.1 Output current direction based commutation technique

Output current direction based commutation techniques rely on knowledge of the load current direction (I_L) to determine the commutation sequence. Referring to Figure 2.14, under steady state condition, both devices in cell A are initially 'on' allowing the current to flow in both directions; the load current is assumed to be flowing in the direction where $I_L > 0$. When a commutation to cell B is required, the current direction is used to determine the non-conducting device in the outgoing cell, cell A. For the case where $I_L > 0$, the switch S_{Aa2} is not conducting so it is turned off first. Then, the device in the incoming cell, cell B, is turned on to form a path for the load current to continue flowing either at the point this incoming switch is gated on or when the outgoing device, S_{Aa1} is subsequently turned off. For the case where $I_L > 0$, the switch S_{Ba1} is gated on. With a new current path available, the device S_{Aa1} can be safely turned off without causing any output terminal open-circuited. Finally, the switch S_{Ba2} is gated on to complete the commutation sequence.

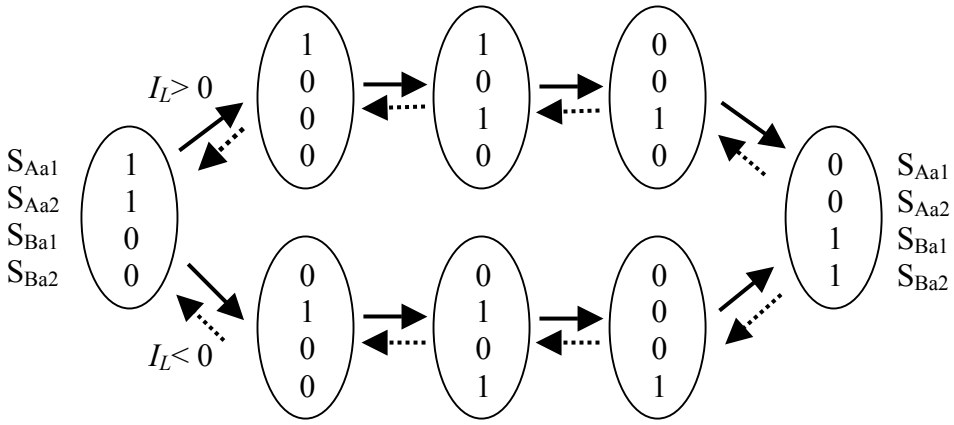
Figure 2.15(a) presents the timing diagram for this four-step output current-direction-based commutation strategy for the load current $I_L > 0$. Referring to the timing diagram,

a time gap, t_d, is introduced between each switching state change. Figure 2.15(b) illustrates the states diagram for this strategy for the load current in both directions.

The output current direction based commutation strategy allows the current to commutate from one bi-directional switch cell to another without causing the input lines short-circuit or the output terminal open-circuit. This commutation strategy enables the switching losses in the devices reduced by 50% due to half of the commutation process being soft switching and, hence, this method is often called the "semi-soft current commutation"[52].



(a) Timing diagram for $I_L > 0$



(b) States diagram

Figure 2.15: The four-step output current direction based commutation strategy

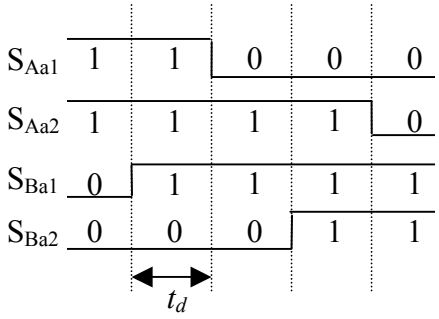
However, the current direction based commutation technique relies on the information of the load current direction, which can be a problem when the variation of the load current is too fast or the current level is too low for the traditional current sensor to detect and generate accurate results. In [59], a technique using the voltages across the bi-directional switches to determine the current direction has been proposed. This technique can accurately determine the load current direction without requiring any external sensor.

2.4.2.2 Relative input voltage magnitude based commutation technique

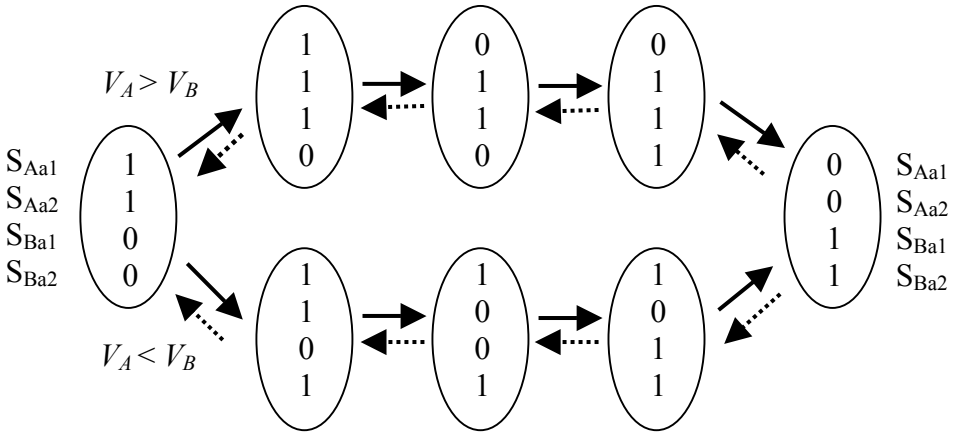
The relative input voltage magnitude based commutation technique is a semi-soft commutation strategy that relies on the knowledge of the relative magnitudes of the input voltages to determine the commutation sequence. The concept of this strategy is to form a freewheeling path in each switch cell involved in commutation. The commutation process begins by identifying the 'freewheeling' device in each switch cell based on the relative magnitudes of the input voltages.

Referring to Figure 2.14, for the case where $V_A > V_B$, the switches S_{Aa2} and S_{Ba1} are the 'freewheeling' devices in cell A and B respectively. Based on the timing diagram shown in Figure 2.16(a), the commutation sequence begins by gating on the freewheeling switch S_{Ba1} in the incoming cell, cell B. With the freewheeling paths available in both cells, the non-freewheeling device S_{Aa1} in the outgoing cell, cell A, can be turned off. Then, the non-freewheeling device S_{Ba2} is turned on. Finally, to complete the commutation sequence, the freewheeling device S_{Aa2} is gated off. Similar to the output current direction based commutation strategy, a time gap is introduced between each switching state change. The commutation sequence for the case where $V_A < V_B$ is also presented in the states diagram shown in Figure 2.16(b).

By applying this strategy, the commutation between two bi-directional switches can be safely implemented. However, if the relative magnitude of the input voltages is not measured correctly, a short circuit path can be mistakenly formed due to the wrong selection of freewheeling devices. Therefore, reliable measurement of the input voltages is required in order to ensure that this commutation strategy is effective.



(a) Timing diagram for $V_A > V_B$



(b) States diagram

Figure 2.16: The four-step relative input voltage magnitude based commutation strategy

2.4.3 Input filter design of the indirect matrix converter

As shown in Figure 2.12(b), the input currents of the indirect matrix converter contain switching frequency harmonics. Considering the cost and size [35,52], a simple low-pass LC filter often offers the best solution for filtering out these undesirable switching frequency harmonics. The input filter configuration for the indirect matrix converter is shown in Figure 2.17, where the filter capacitors (C_f) are connected in star arrangement and inductors (L_f) are connected in series with each supply line. This design forms a second order filter, with a cutoff frequency designed to be much lower than the switching frequency in order to provide considerable attenuation at the switching frequency. The cutoff frequency of the filter is configured by the choice of capacitor and inductor based on equation (2.36).

$$f_{cutoff} = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{2.36}$$

However, to design a suitable low pass filter for matrix converters, the selected capacitor and inductor should fulfill the following requirements:

- The choice of capacitor must assure that the reactive power at the supply frequency is minimized.
- The voltage drop across the inductor L_f at rated current is minimized (i.e. $V_A \cong V_A'$) in order to provide the possible highest voltage transfer ratio.
- The volume and weight of the selected capacitors and inductors are minimized.

By considering the rated power of the matrix converter and the required performance (e.g. $\cos(\varphi_i) > 0.9$ for $P_{out} > 10\%$ of rated power), the maximum filter capacitance, C_{f_max}, can be determined using the equation given below [51]:

$$C_{f\_\max} = \frac{P_{out} * \tan(\varphi_{i\_\max})}{3 * V_i^2 * \omega_i} \tag{2.37}$$

where φ_{i_max} is the maximum input displacement angle at the minimum output power, P_{out}. The variables 'V_i' and 'ω_i' are the magnitude and frequency of the supply voltage. By determining the capacitance C_f, the filter inductance, L_f, can be determined using equation (2.36). However, the filter inductance must ensure minimum voltage drop at rated current, which is lower than the value determined using equation (2.38) in [35].

$$L_f \le \frac{\sqrt{\left(\frac{\Delta V_L}{V_R}\right)^2 - 2*\left(\frac{\Delta V_L}{V_R}\right)}}{\omega_i} * \frac{V_R}{I_R} \tag{2.38}$$

where ΔV_L is the maximum voltage drop across the filter inductor; V_R and I_R are the rated voltage supply and current respectively.

Generally, to design an appropriate low pass filter for the indirect matrix converter, a compromise between the capacitor and the inductor's size has to be made. Low filter

capacitance promises the high input power factor but requires a large inductance to achieve the required cutoff frequency. In addition, the permissible maximum voltage drop, ΔV_L, often limits the size of selected inductor.

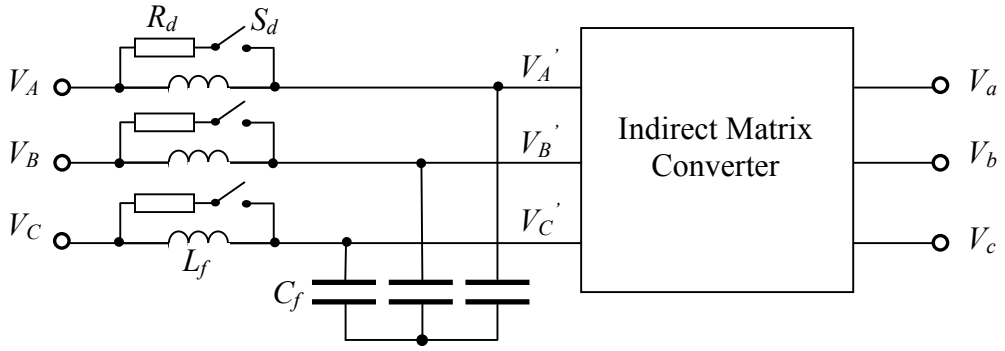


Figure 2.17: The input filter configuration

2.4.4 Protection issues for the indirect matrix converter

2.4.4.1 Over-voltage Protection

For matrix converter topologies, over-voltages can happen either at the supply side or the load side. At the load, the over-voltage occurs due to the unexpected shut down of the converter, for example in an over-current situation. When all bi-directional switches are turned off, there is no freewheeling path for the current to discharge the energy stored in the load inductance, which consequently causes an over-voltage. On the other hand, the over-voltage at the supply side can be due to line perturbations or a severe transient response of the input LC filter during the power-up. As a result, an additional protection circuit is essential to protect the matrix converter from any damage due to over-voltage condition.

2.4.4.2 Clamp circuit

A clamp circuit is a protection circuit that limits the over-voltage level either at the supply side or the load side of the converter in order to ensure the safe operation of the matrix converter [17,60]. The clamp circuit generally consists of two bridges of fast-

recovery diodes with a clamp capacitor and resistor that connected in parallel. During an over-voltage, the fast-recovery diodes provide paths for the current, which charge up the clamp capacitor. The resistor dissipates the energy stored in the clamp capacitor in order to maintain a safe voltage level.

For the indirect matrix converter topology, the clamp circuit configuration is shown in Figure 2.18. Due to the use of anti-parallel diodes in the inversion stage, natural freewheeling paths are always available. As the positive voltage level is applied to the *p*-terminal and the negative voltage level to the *n*-terminal of the DC-link, only two fast-recovery diodes are required to connect the DC-link to the clamp capacitor. A comprehensive analysis of the design of the clamp circuit for the matrix converters for industrial applications was discussed in [60]. For a motor load, the value of the clamp capacitor, C_C, can be determined using the equation given below:

$$C_C = \frac{\frac{3}{2} * {I_{\max}}^2 * \left(L_{\delta S} + L_{\delta R}\right)}{{V_{\max}}^2 + {V_{LL}}^2} \tag{2.39}$$

where I_{max} is the maximum current; $(L_{\delta S} + L_{\delta R})$ is the total motor leakage inductance; V_{max} is the maximum voltage level of the clamp capacitor (less than the voltage rating of the semiconductor devices) and V_{LL} is the steady state voltage across the clamp capacitor (the peak amplitude of the line-to-line supply voltage).

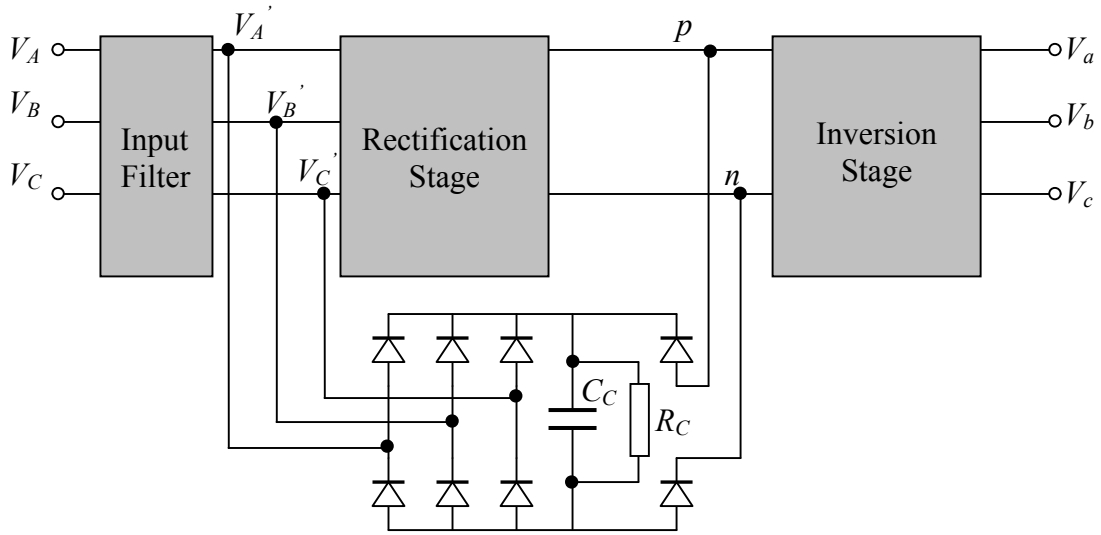


Figure 2.18: A clamp circuit configuration for the indirect matrix converter

2.4.4.3 Protection against over-voltage caused by the LC filter

Even though the low pass filter smoothes out the input current, it can cause undesirable disruptions for the matrix converter during the power-up. This transient response can appear when a voltage step is applied to the LC filter circuit, which can cause destructive over-voltage to the converter [35]. Hence, a method of connecting a damping resistor, R_d, and a switch, S_d, parallel with the inductor L_f has been proposed [35] for alleviating this problem. The selected damping resistor, R_d, has to be smaller than the choke reactance at the cut-off frequency:

$$R_d \leq 2 \cdot \pi \cdot f_{cutoff} \cdot L_f \tag{2.40}$$

Referring to Figure 2.17, S_d is initially turned on during the power-up. Due to the smaller resistance of R_d, the current mostly flows through the damping resistors instead of the chokes, which improves the waveforms during power-up. Once the filter and the clamp capacitor are fully charged to the supply voltages, S_d is turned off.

2.5 Advantages of the indirect matrix converter over the direct matrix converter

2.5.1 Overview

The indirect matrix converter offers the same benefits compared to the conventional matrix converter. In some applications, the indirect matrix converter may be preferred to the direct matrix converter due to the advantages discussed in this section.

2.5.2 Safer commutation

Referring to Figure 2.11, while a commutation is implemented at the rectification stage, a zero voltage vector, V_0, is produced by the inversion stage. By using the zero voltage vector, the DC-link current is zero. Hence, the switches of the rectification stage are

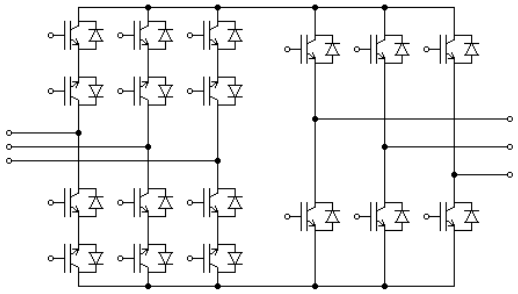
commutated at zero current, which promise a safer commutation environment and lower switching losses for the rectification stage [27].

2.5.3 Reduced number of switches

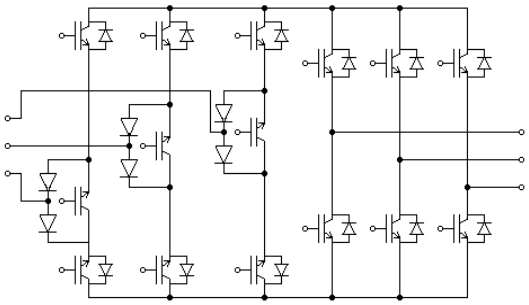
In [28, 30], the possibility of reducing the total number of semiconductor switches required for the indirect matrix converter topology has been presented. These topologies are referred as the "sparse matrix converters" [28] and Figure 2.19 presents three examples of these converters. Even though constructed with reduced number of switching devices, the sparse matrix converters are still able to provide unity input displacement factor, sinusoidal supply currents and load voltages that are identical to the conventional matrix converters. In addition, by having fewer switching devices, the design of the sparse matrix converters is simpler, which enables them to be constructed with reduced cost.

The process of reducing the switches is performed at the rectification stage. For the sparse matrix converter, shown in Figure 2.19(b), one switch and two clamp diodes are used to replace two middle switches of each phase leg of the rectification stage, which is able to reduce the total number of switching devices from 18 (the indirect matrix converter) to 15. This reduction does not affect the four-quadrant ability of the converter but does cause higher conduction losses by having more semiconductor devices in the current conduction path.

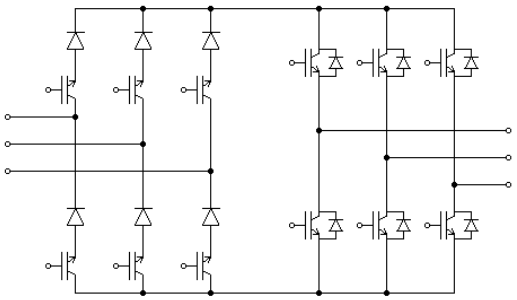
Alternatively, by knowing that the DC-link current only flows in one direction, the number of switching devices can be further reduced to 12 (very sparse matrix converter, VSMC) or 9 (ultra sparse matrix converter, USMC). However, due to this unidirectional DC-link current constraint, the VSMC and the USMC are not applicable for the regenerative operation and the minimum load power factor of the VSMC and USMC is limited to 0.866 [30].



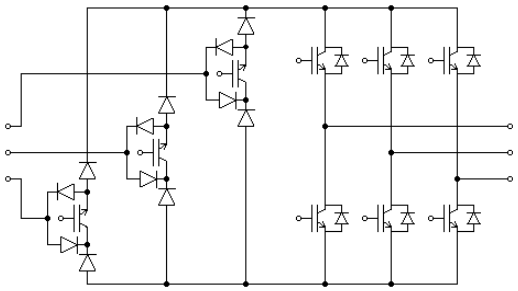
(a) Indirect matrix converter



(b) Sparse matrix converter



(c) Very sparse matrix converter



(d) Ultra sparse matrix converter

Figure 2.19: The indirect matrix converter topologies with reduced number of switches

2.5.3 Cost effective multi-drive system

Finally, the indirect matrix converter offers an attractive option for replacing traditional AC-DC-AC converters in the conventional multi-motor drive systems that require large DC-link energy storage components to couple the rectification stage to multiple inversion stages. The concept of multi-motor-drive systems has been proposed for specific cost reduction in the multiple motor drives applications [61]. The use of DC-link capacitors in conventional multi-motor-drive system has potential risks due to the high amount of stored energy. Hence, extra precautions for preventing shoot through faults have to be taken. In [29], a cost effective multi-motor-drive system using the indirect matrix converter has been proposed, which eliminates the need of DC-link energy storage components. Figure 2.20 shows the block diagram of a multi-drive system using indirect matrix converters.

The effectiveness of the indirect matrix converter to perform the sine-wave-in/sine-wave-out operation has been shown in Figure 2.12. In order to ensure similar high quality inputs and outputs in the multi-drive system, the average power, during a switching period, flowing through the virtual DC-link has to be maintained at a constant value, which is achievable in the case of symmetrical loads, no matter how many inversion stages. In [29], a central unit is used for controlling this system in the hardware implementation. The modulation on the rectification stage distributes the power in the DC-link to provide the sinusoidal synthesis of the input currents and the maximum average DC-voltage level for any of the inversion stages while the switching patterns of the inversion stages are synchronised with the rectification stage for sinusoidal output voltage generation.

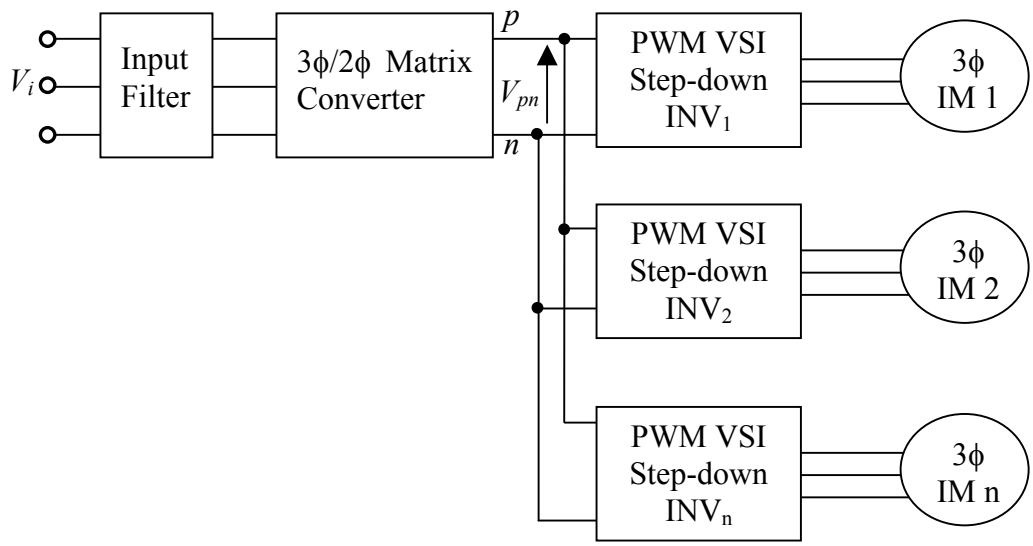


Figure 2.20: A multi-drive system based on the indirect matrix converter.

2.6 Conclusions

In this chapter, the indirect matrix converter technology from the converter derivation, the modulation scheme and the hardware implementation has been fully reviewed. Derived from the indirect transfer function approach proposed for the conventional matrix converter, the indirect matrix converter is able to generate high quality inputs and output waveforms identical to the direct matrix converter by applying space vector modulation.

In the hardware implementation, similar to the conventional matrix converter, bi-directional switches and associated commutation techniques are required for the indirect matrix converter to effectively perform the desired four-quadrant operation. A procedure for designing a suitable and effective input filter for the indirect matrix converter is also presented so that a set of sinusoidal input currents can be obtained at the supply side. For protecting the indirect matrix converter, the clamp circuit and damping resistors are essential to protect the converter from any damage due to over voltages that can occur either at the supply side or the load side.

Finally, the advantages of the indirect matrix converter over the direct matrix converter are reviewed, which clarify why the indirect matrix converter may be preferred to the conventional matrix converter in some applications.

Chapter 3

Three-level Neutral-point-clamped Voltage Source Inverter

3.1 Introduction

As discussed in Chapter 1, the three-level-output-stage matrix converter is a multilevel matrix converter topology that applies the three-level neutral-point-clamped voltage source inverter concept to the inversion stage of an indirect matrix converter topology. In order to provide the foundation to understand a modulation strategy proposed for the three-level-output-stage matrix converter, this chapter reviews the three-level neutral-point-clamped voltage source inverter technology from the operating principles to the related modulation schemes, which are well established in research [64 - 69]. The neutral-point balancing problem of the three-level neutral-point-clamped voltage source inverter and associated control methods are also discussed. This chapter will be concluded with the simulation results of the three-level neutral-point-clamped voltage source inverter, which are shown to prove the ability of the three-level neutral-point-clamped voltage source inverter to generate multilevel outputs and the effectiveness of the modulation scheme in controlling the neutral-point balancing problem.

3.2 Circuit Topology

The three-level neutral-point-clamped voltage source inverter (NPC VSI) was introduced by Nabae in 1981 [10] and is probably the most popular among the multilevel converter topologies for high voltage, high power applications. As shown in Figure 3.1, the NPC VSI is supplied by two series-connected capacitors (C1 and C2), where both capacitors are charged to an equal potential of V_{DC}, with the DC-link middle point '*o*' as a zero DC voltage neutral point. Each phase leg of the NPC VSI consists of

four series-connected switching devices and two clamping diodes. These diodes clamp the middle switches' potential to the DC-link point '*o'*.

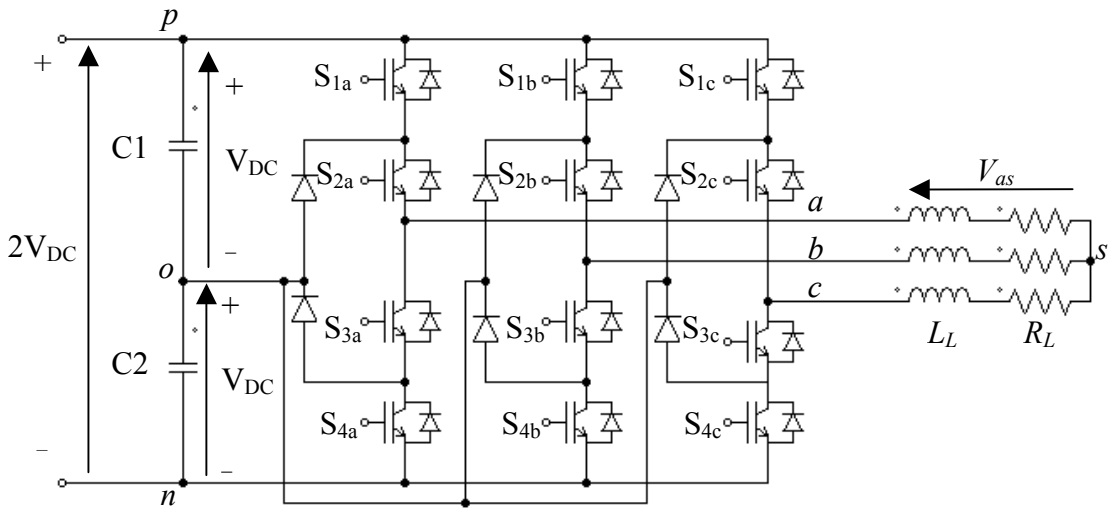


Figure 3.1: The schematic diagram of a conventional three-level neutral-point-clamped voltage source inverter using the IGBT switches

In order to generate the three-level output, the switching devices in each phase leg are controlled according to the switching combinations presented in Table 3.1. At any time, only two of the four switching devices are turned on and the output terminal can be connected to any of the DC-link points (*p*, *o* or *n*), which can be represented by a switching state (P, O or N); for example switching state *P* represents the connection of the output terminal to the DC-link point '*p'*. Using the DC-link middle point '*o*' as a reference, the NPC VSI is obviously able to generate three distinct voltage levels at the output terminal of each phase leg, V_{xo}, which can be determined using the following equation:

$$V_{xo} = V_{DC}(m_{x1} - m_{x3}) \tag{3.1}$$

The variables m_{x1} and m_{x3} represent the switch combinations (S_{1x} & S_{2x}) and (S_{3x} & S_{4x}) in each phase leg ($x \in \{a, b, c\}$), which is one when both switches in the combination are 'on' and zero otherwise [13].

S_{1x}	S_{2x}	S_{3x}	S_{4x}	V_{xo}	Switching state
ON	ON	OFF	OFF	V_{DC}	P
OFF	ON	ON	OFF	0	O
OFF	OFF	ON	ON	$-V_{DC}$	N

Table 3.1: The switching combination for the switches in each phase leg of the three-level neutral-point-clamped voltage source inverter ($x \in \{a, b, c\}$)

For a three-level three-phase NPC VSI, there are twenty-seven switching states that represent the connections of the output terminals (*a*, *b* and *c*) to their respective DC-link points. Having a star-connected load applied to the NPC VSI, as shown in Figure 3.1, these switching states are able to generate specific output phase (line-to-load neutral, *s*) and output line-to-line voltages, as shown in Table 3.2. The output voltages can be determined using equations (3.2) and (3.3) [13].

$$V_{as} = (2/3).V_{DC}[m_{a1} - m_{a3} - (1/2)(m_{b1} - m_{b3} + m_{c1} - m_{c3})]$$

$$V_{bs} = (2/3).V_{DC}[m_{b1} - m_{b3} - (1/2)(m_{a1} - m_{a3} + m_{c1} - m_{c3})]$$

$$V_{cs} = (2/3).V_{DC}[m_{c1} - m_{c3} - (1/2)(m_{a1} - m_{a3} + m_{b1} - m_{b3})] \quad (3.2)$$

$$V_{ab} = V_{ao} - V_{bo} = V_{DC}(m_{a1} - m_{a3} - m_{b1} + m_{b3})$$

$$V_{bc} = V_{bo} - V_{co} = V_{DC}(m_{b1} - m_{b3} - m_{c1} + m_{c3})$$

$$V_{ca} = V_{co} - V_{ao} = V_{DC}(m_{c1} - m_{c3} - m_{a1} + m_{a3}) \quad (3.3)$$

Referring to Table 3.2, with the ability to generate three voltage levels at each output terminal, the NPC VSI is able to produce five distinctive levels ($\pm 2V_{DC}$, $\pm V_{DC}$ and 0V) for the output line-to-line voltages. Compared to a conventional two-level voltage source inverter, the NPC VSI has the following advantages:

Switching State Combination			Output phase voltages			Output line-to-line voltages		
a	*b*	*c*	V_{as}	V_{bs}	V_{cs}	V_{ab}	V_{bc}	V_{ca}
P	P	P	0	0	0	0	0	0
O	O	O	0	0	0	0	0	0
N	N	N	0	0	0	0	0	0
P	O	O	$\frac{2}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	V_{DC}	0	$-V_{DC}$
O	P	O	$-\frac{1}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$-V_{DC}$	V_{DC}	0
O	O	P	$-\frac{1}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	0	$-V_{DC}$	V_{DC}
P	P	O	$\frac{1}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	0	V_{DC}	$-V_{DC}$
O	P	P	$-\frac{2}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$-V_{DC}$	0	V_{DC}
P	O	P	$\frac{1}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	V_{DC}	$-V_{DC}$	0
N	O	O	$-\frac{2}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$-V_{DC}$	0	V_{DC}
O	N	O	$\frac{1}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	V_{DC}	$-V_{DC}$	0
O	O	N	$\frac{1}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	0	V_{DC}	$-V_{DC}$
N	N	O	$-\frac{1}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	0	$-V_{DC}$	V_{DC}
O	N	N	$\frac{2}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	V_{DC}	0	$-V_{DC}$
N	O	N	$-\frac{1}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$-V_{DC}$	V_{DC}	0
P	N	N	$\frac{4}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$2\cdot V_{DC}$	0	$-2\cdot V_{DC}$
P	P	N	$\frac{2}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$-\frac{4}{3}\cdot V_{DC}$	0	$2\cdot V_{DC}$	$-2\cdot V_{DC}$
N	P	P	$-\frac{4}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$-2\cdot V_{DC}$	0	$2\cdot V_{DC}$
N	N	P	$-\frac{2}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$\frac{4}{3}\cdot V_{DC}$	0	$-2\cdot V_{DC}$	$2\cdot V_{DC}$
P	N	P	$\frac{2}{3}\cdot V_{DC}$	$-\frac{4}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$2\cdot V_{DC}$	$-2\cdot V_{DC}$	0
N	P	N	$-\frac{2}{3}\cdot V_{DC}$	$\frac{4}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$-2\cdot V_{DC}$	$2\cdot V_{DC}$	0
P	O	N	V_{DC}	0	$-V_{DC}$	V_{DC}	V_{DC}	$-2\cdot V_{DC}$
O	P	N	0	V_{DC}	$-V_{DC}$	$-V_{DC}$	$2\cdot V_{DC}$	$-V_{DC}$
N	P	O	$-V_{DC}$	V_{DC}	0	$-2\cdot V_{DC}$	V_{DC}	V_{DC}
N	O	P	$-V_{DC}$	0	V_{DC}	$-V_{DC}$	$-V_{DC}$	$2\cdot V_{DC}$
P	N	O	V_{DC}	$-V_{DC}$	0	$2\cdot V_{DC}$	$-V_{DC}$	$-V_{DC}$
O	N	P	0	$-V_{DC}$	V_{DC}	V_{DC}	$-2\cdot V_{DC}$	V_{DC}

Table 3.2: Switching states for the three-level neutral-point-clamped voltage source inverter.

- By constructing the output waveforms with multiple voltage levels (e.g. five levels for the output line-to-line voltage), the output waveform visibly resembles the desired sinusoidal waveform so the harmonic distortion is lower.

- By having the output consists of multiple smaller voltage levels with lower ΔV, the stresses imposed on motor bearing and winding isolation in the adjustable speed drive application are lower than that for a two-level voltage source inverter [4,5].

- The connection of the clamping diodes limits the voltage stress across the off-state switching devices to one capacitor voltage level; half of the DC-link voltage [9]. Due to the reduced voltage stress, medium voltage rated semiconductor devices can be used to construct the converters for high voltage, high power applications.

However, the high number of power semiconductor devices and complex modulation scheme are required for this topology to achieve the desired results. Besides that, the neutral-point balancing problem of the NPC VSI is an inherent drawback, which has been widely published in the literatures.

In order to generate a set of balanced and sinusoidal output waveforms, various modulation strategies have been proposed for the NPC VSI, such as staircase modulation [7], carrier based multilevel pulse-width modulation [62], switching frequency optimal pulse-width modulation [63] and space vector modulation (SVM) [64 - 69]. SVM is probably the most popular technique due to its low complexity and high efficiency when implemented with modern digital technology. In the following section, only the SVM is reviewed because its concept provides the foundation for a space vector modulation for the three-level-output-stage matrix converter. The neutral-point balancing problem of the NPC VSI and associated control methods will also be discussed because the three-level-output-stage matrix converter also inherits the neutral-point balancing problem, which must be controlled in order to ensure proper operation of the converter.

3.3 Space vector modulation

SVM is a pulse width modulation strategy that uses the concept of space vectors to compute the duty cycles of the switches. To implement this modulation strategy to the NPC VSI, the output phase voltages generated by the switching states of the NPC VSI have to be converted into space vectors using the following transformation:

$$\overline{V} = \frac{2}{3}\left(V_{as} + V_{bs} e^{j\frac{2}{3}\pi} + V_{cs} e^{-j\frac{2}{3}\pi} \right) \tag{3.4}$$

For the NPC VSI, all the switching state combinations listed in Table 3.2 can be transformed into eighteen distinct voltage space vectors with fixed directions, as shown in Table 3.3. Based on their magnitudes, these voltage space vectors can be divided into four groups: zero voltage vector ZVV (V_0), small voltage vectors SVV (V_1, V_4, V_7, V_{10}, V_{13} and V_{16}), middle voltage vectors MVV (V_3, V_6, V_9, V_{12} and V_{15}) and large voltage vectors LVV (V_2, V_5, V_8, V_{11}, V_{14} and V_{17}). Figure 3.2 shows the space vector diagram of the NPC VSI that is formed by these voltage space vectors, where the ZVV and SVV obviously have redundant switching states that offer an additional degree of freedom in the synthesize of the output voltage vector.

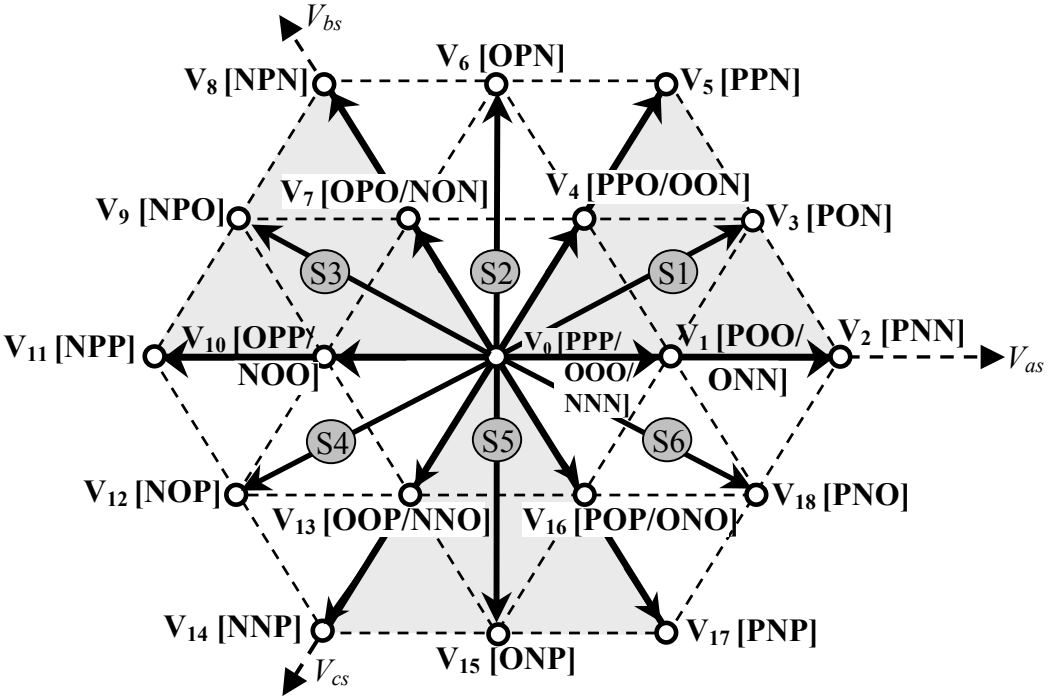


Figure 3.2: The space vector diagram for the three-level neutral-point-clamped voltage source inverter

Switching state combination			Output voltage vectors		
a	*b*	*c*	Vector	Magnitude	Angle
P	P	P	V_0	0V	0
O	O	O			
N	N	N			
P	O	O	V_1	$\frac{2}{3} V_{DC}$	0
O	N	N			
P	N	N	V_2	$\frac{4}{3} V_{DC}$	0
P	O	N	V_3	$\frac{2}{\sqrt{3}} V_{DC}$	π/6
P	P	O	V_4	$\frac{2}{3} V_{DC}$	π/3
O	O	N			
P	P	N	V_5	$\frac{4}{3} V_{DC}$	π/3
O	P	N	V_6	$\frac{2}{\sqrt{3}} V_{DC}$	π/2
O	P	O	V_7	$\frac{2}{3} V_{DC}$	2π/3
N	O	N			
N	P	N	V_8	$\frac{4}{3} V_{DC}$	2π/3
N	P	O	V_9	$\frac{2}{\sqrt{3}} V_{DC}$	5π/6
O	P	P	V_{10}	$\frac{2}{3} V_{DC}$	π
N	O	O			
N	P	P	V_{11}	$\frac{4}{3} V_{DC}$	π
N	O	P	V_{12}	$\frac{2}{\sqrt{3}} V_{DC}$	- 5π/6
O	O	P	V_{13}	$\frac{2}{3} V_{DC}$	- 2π/3
N	N	O			
N	N	P	V_{14}	$\frac{4}{3} V_{DC}$	- 2π/3
O	N	P	V_{15}	$\frac{2}{\sqrt{3}} V_{DC}$	- π/2
P	O	P	V_{16}	$\frac{2}{3} V_{DC}$	- π/3
O	N	O			
P	N	P	V_{17}	$\frac{4}{3} V_{DC}$	- π/3
P	N	O	V_{18}	$\frac{2}{\sqrt{3}} V_{DC}$	- π/6

Table 3.3: The magnitude and angle of each voltage space vector formed by the switching state of the NPC VSI using the space vector transformation.

The desired output for the NPC VSI is a set of sinusoidal and balanced output voltages. Using the space vector transformation (3.4), this set of time-varying signals is transformed into a reference output voltage vector, $\overline{V}_{out}$, that rotates along a circular trajectory with frequency ω_o in the space vector diagram. This reference output voltage vector can be expressed as:

$$\overline{V}_{out} = V_{om} e^{j(\omega_o t - \varphi_o)} = V_{om} \angle \theta_o \tag{3.5}$$

where V_{om} is the magnitude and θ_o is the direction of the reference vector. The variable θ_o is equal to $\omega_o t$ - φ_o, where $\omega_o t$ is the angle of the output phase voltages and φ_o is an arbitrary angle. The reference vector, $\overline{V}_{out}$, can be synthesized with three nearest voltage space vectors, which are selected based on the triangle in which the reference vector is located at the sampling instant. Referring to Figure 3.2, the space vector diagram of the NPC VSI is divided into six sectors (S1 – S6), where each sector consists of four triangles.

Due to the circular symmetry of a three-phase system, it is sufficient to analyze the procedures for synthesizing the reference vector, $\overline{V}_{out}$, that is located in S1 ($0 \le \theta_o < 60^0$) to derive the duty cycle equations for the selected vectors in each triangle. To facilitate this explanation, Figure 3.3 shows sector S1 of the space vector diagram for the NPC VSI. For a switching period, T_{SW}, the output reference vector is synthesized using equation (3.6) based on the constraint $d_x + d_y + d_z = 1$, where d_x, d_y and d_z are the duty cycles that represent the active times of the selected vectors within the switching period, T_{SW}.

$$\overline{V}_{out} = d_x V_x + d_y V_y + d_z V_z \tag{3.6}$$

Let us consider an example where voltage vectors V_1, V_3 and V_4 are selected to synthesize a reference vector, $\overline{V}_{out}$, that is located in triangle *T3* at the sampling instant. The duty cycle equations of the selected voltage vectors can be derived as follow:

1. Specify the voltage vector V_2 as the reference axis and its magnitude as units. Each selected voltage vector and the reference vector can then be expressed as:

$$V_x = V_1 = \frac{1}{2}\ ;\ V_y = V_3 = \frac{\sqrt{3}}{2}e^{j\frac{\pi}{6}}\ ;\ V_z = V_4 = \frac{1}{2}e^{j\frac{\pi}{3}}\ ;\ \overline{V}_{out} = V_{opu}\cdot e^{j\theta_{out}} \tag{3.7}$$

where $V_{opu} = \dfrac{V_{om}}{4V_{DC}/3}$

2. Substitute (3.7) into (3.6) and then convert (3.6) into trigonometric form:

$$V_{opu}\left(\cos\theta_{out} + j\sin\theta_{out}\right) = \frac{1}{2}d_x + \frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6} + j\sin\frac{\pi}{6}\right)\cdot d_y + \frac{1}{2}\left(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}\right)\cdot d_z$$

3. Separate the real and imaginary parts from the equation above:

Real: $$\frac{1}{2}d_x + \frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6}\right)\cdot d_y + \frac{1}{2}\left(\cos\frac{\pi}{3}\right)\cdot d_z = V_{opu}\left(\cos\theta_{out}\right)$$

Imaginary: $$\frac{\sqrt{3}}{2}\left(\sin\frac{\pi}{6}\right)\cdot d_y + \frac{1}{2}\left(\sin\frac{\pi}{3}\right)\cdot d_z = V_{opu}\left(\sin\theta_{out}\right)$$

4. Solve the real and imaginary parts using the constraint $d_x + d_y + d_z = 1$.

5. The equations for the duty cycles d_x, d_y and d_z of triangle *T3* are then determined:

$$d_x = 1 - 2\cdot m_u\cdot\sin\theta_{out}$$

$$d_y = 2\cdot m_u\cdot\sin\left(\theta_{out} + \pi/3\right) - 1$$

$$d_z = 2\cdot m_u\cdot\sin\left(\theta_{out} - \pi/3\right) + 1 \tag{3.8}$$

where

$$m_u = \frac{2\cdot V_{opu}}{\sqrt{3}} = \frac{\sqrt{3}\cdot V_{om}}{2\cdot V_{DC}}\ \text{ is the modulation index } (0 \le m_u \le 1) \tag{3.9}$$

and θ_{out} is the angle of the reference vector, $\overline{V}_{out}$, within the sector. For the other triangles (*T1*, *T2* or *T4*), the duty cycle equations for the selected voltage vectors can be derived following a similar procedure. Table 3.4 presents the duty cycle equations of the selected voltage vectors for all triangles within this sector.

- $|\mathbf{V_{SVV}}| = \frac{2}{3} V_{DC}$
- $|\mathbf{V_{MVV}}| = \frac{2}{\sqrt{3}} V_{DC}$
- $|\mathbf{V_{LVV}}| = \frac{4}{3} V_{DC}$
- $\theta_{V1}, \theta_{V2} = 0$
- $\theta_{V3} = \pi/6$
- $\theta_{V4}, \theta_{V5} = \pi/3$

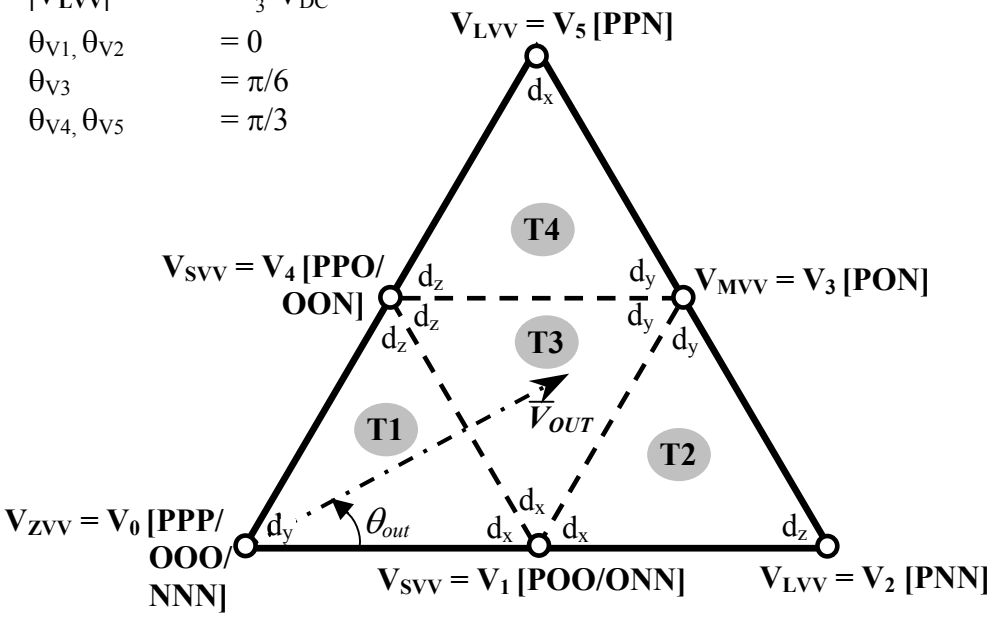


Figure 3.3: Sector 1 of the space vector diagram of the three-level neutral point clamped voltage source inverter

Triangle	d_x	d_y	d_z
T1	$2 \cdot m_u \cdot \sin\left(\frac{\pi}{3} - \theta_{out}\right)$	$1 - 2 \cdot m_u \cdot \sin\left(\theta_{out} + \frac{\pi}{3}\right)$	$2 \cdot m_u \cdot \sin\theta_{out}$
T2	$2 - 2 \cdot m_u \cdot \sin\left(\theta_{out} + \frac{\pi}{3}\right)$	$2 \cdot m_u \cdot \sin\theta_{out}$	$2 \cdot m_u \cdot \sin\left(\frac{\pi}{3} - \theta_{out}\right) - 1$
T3	$1 - 2 \cdot m_u \cdot \sin\left(\theta_{out}\right)$	$2 \cdot m_u \cdot \sin\left(\frac{\pi}{3} + \theta_{out}\right) - 1$	$2 \cdot m_u \cdot \sin\left(\theta_{out} - \frac{\pi}{3}\right) + 1$
T4	$2 \cdot m_u \cdot \sin\theta_{out} - 1$	$2 \cdot m_u \cdot \sin\left(\frac{\pi}{3} - \theta_{out}\right)$	$2 - 2 \cdot m_u \cdot \sin\left(\theta_{out} + \frac{\pi}{3}\right)$

Table 3.4: The duty cycle equations for the selected voltage vectors in each triangle

By determining the duty cycles of the selected voltage vectors, the duty cycles for the switches, over a switching period, can be determined. To complete the modulation process, the selected voltage vectors are applied to the output according to a switching sequence. Ideally, a switching sequence is formed in such a way that high quality output waveform is obtained with minimum number of switching transitions. For example, the voltage vectors V_1, V_3 and V_4 are selected to synthesize the reference vector so, to ensure one switching transition for each phase leg [13], one possible switching sequence is POO – PON – OON – ONN. However, in order to control the neutral-point balancing problem of the NPC VSI, the redundant switching states of the selected SVV(s) must be equally applied to the output. As a result, the switching sequence is now PPO – POO – PON – OON – ONN and the number of switching transitions is unavoidably increased. In the following section, the neutral-point balancing problem of the NPC VSI and associated control methods are reviewed to explain why the redundant switching state combinations of the selected SVV(s) must be equally applied to the output for each switching period.

3.3.1 The neutral-point balancing problem

The neutral-point balancing problem of the NPC VSI has been extensively discussed in academic publications [64 – 69]. It is an inherent problem of the NPC VSI that is caused by uneven charging/discharging of the DC-link capacitors (C1 and C2) when the output terminal is connected to the DC-link middle point '*o*'.

As mentioned in Section 3.2, each output terminal of the NPC VSI can be connected to the DC-link middle point '*o*' for the zero DC-voltage level (V_{xo} = 0V). However, whenever the output terminal is connected to point '*o*', the neutral-point current, i_o, causes uneven charging or discharging of the DC-link capacitors, depending on the loading conditions. Figure 3.4 illustrates how certain switching states affect the voltage levels of the capacitors when the output terminal(s) connected to the neutral-point. Without proper control, the uneven changing voltage levels of the DC-link capacitors impact on the ability of the NPC VSI to properly generate the three-level output waveform, causing the output voltage distortion. The uncontrolled changing voltage levels also impose unnecessary voltage stress on the switching devices because, with the

connection of the clamping diodes, the voltage stress across the off-state switching devices is proportional to the voltage across the capacitor.

In SVM, only the vectors MVV and SVV cause the uneven changing voltage levels of the DC-link capacitors due to the connection of the output to the neutral-point. Table 3.5 presents the voltage vectors that can cause the neutral-point balancing problem and their respective generated neutral-point current, i_o. Referring to this table, for each SVV, the switching state that connects the output phase current with positive sign to the point '*o*' is referred to as the 'positive small voltage vector' while the switching state that connects the output phase current with negative sign is referred to as the 'negative small voltage vector'.

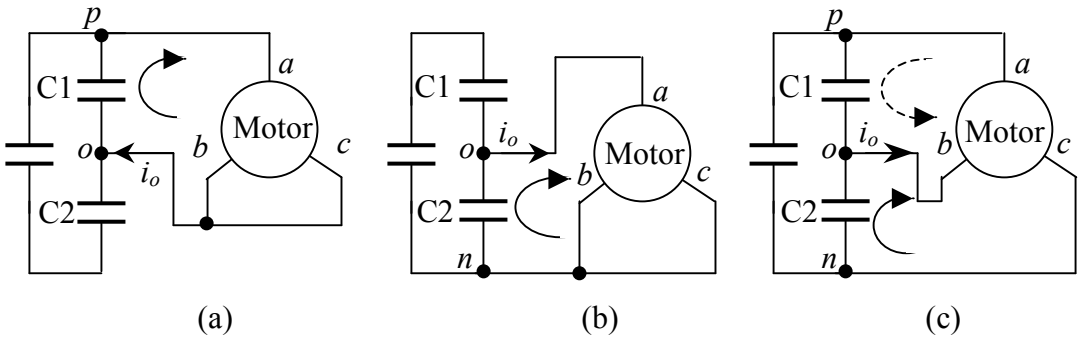


Figure 3.4: The neutral-point balancing problem caused by the switching states (a) POO (b) ONN (c) PON (⟶ = discharging and ⇢ = charging)

Positive small voltage vectors	i_o	Negative small voltage vectors	i_o	Medium voltage vectors	i_o
ONN	i_a	POO	$-i_a$	PON	i_b
PPO	i_c	OON	$-i_c$	OPN	i_a
NON	i_b	OPO	$-i_b$	NPO	i_c
OPP	i_a	NOO	$-i_a$	NOP	i_b
NNO	i_c	OOP	$-i_c$	ONP	i_a
POP	i_b	ONO	$-i_b$	PNO	i_c

Table 3.5: The neutral-point current, i_o, generated by the small voltage space vectors and the medium voltage space vectors

In order to maintain the voltage levels of the DC-link capacitors, selected MVV and SVV should be applied in such a way that the average neutral-point current over a switching period is maintained at zero [67]. Referring to Table 3.5, the positive and negative small voltage vectors of a SVV apparently connect the same output phase current to the neutral-point but with opposite sign. Hence, by applying both switching states of a selected SVV with equal active time in the switching sequence, the i_o can be balanced and zero average neutral-point current over a switching period can be obtained. However, unlike the SVV, the MVV does not have any redundant vectors.

Various neutral-point balancing control methods have been proposed that apply the positive and negative small voltage vectors of selected SVVs and adjust their active times in the switching sequence to compensate for the total neutral-point current. However, when the modulation index is high [67], the i_o generated by the MVV cannot be completely compensated by the SVVs. In [69], the nearest three virtual space vector modulation (NTV SVM) has been proven to be able to control the neutral-point balancing problem over the full range of output voltage and for all power factors, provided that the sum of the output phase currents equals zero ($i_a + i_b + i_c = 0$).

3.3.1.1 The nearest three virtual space vector modulation

In order to maintain the DC-link capacitor voltages, the NTV SVM defines a set of virtual vectors that are able to produce zero average neutral-point current over each switching period. As shown in Figure 3.5, there are four types of virtual vectors: the virtual zero vector (V_{ZV}), the virtual small vector (V_{SV}), the virtual medium vector (V_{MV}) and the virtual large vector (V_{LV}). These virtual vectors are formed using the voltage space vectors from the conventional SVM:

- V_{LV} is formed with LVV. This virtual vector generates zero neutral-point current because the LVV does not connect any output terminal to the neutral-point.
- V_{MV} is formed by an equal linear combination of three voltage vectors from the same sector, where each voltage vector connects different output phase current (i_a, i_b or i_c) to the neutral-point. The V_{MV} is able to generate zero average neutral-point current provided $i_a + i_b + i_c = 0$. For example, referring to Table

3.5, the medium voltage vector *PON* from sector 1 connects an output phase current, i_b, to the neutral-point. Based on the output current relationship $i_a + i_b + i_c = 0$, in order to compensate the current i_b, the small voltage vectors *PPO* and *ONN* have to be equally applied to connect currents i_a and i_c, respectively, to the neutral-point. The linear combination of these voltage vectors creates the V_{MV1}. If the vector V_{MV1} is applied for an interval t_{MV}, the switching states *PPO, PON* and *ONN* are equally active for (1/3)*t_{MV}. Hence, the average neutral-point current during this interval will be:

$$\left(1/t_{MV}\right)\left[\left(i_a * \tfrac{1}{3} * t_{MV}\right) + \left(i_b * \tfrac{1}{3} * t_{MV}\right) + \left(i_c * \tfrac{1}{3} * t_{MV}\right)\right] = 0$$

- V_{SV} is formed by equitable linear combination of the positive and negative small voltage vectors of a SVV. As shown in Table 3.5, the positive and negative small voltage vectors of a SVV connect the same output phase current to the neutral-point but with opposite sign. Hence, by applying both vectors for equal time, the i_o can be balanced and zero average neutral-point current can be obtained. For example, V_{SV1} is formed with switching states *POO* and *ONN*. If V_{SV1} is selected for an interval t_{SV}, *POO* is applied for (1/2)*t_{SV} and *ONN* is active for (1/2)*t_{SV}. As a result, the average neutral-point current during this interval will be:

$$\left(1/t_{SV}\right)\left[\left(-i_a * \tfrac{1}{2} * t_{SV}\right) + \left(i_a * \tfrac{1}{2} * t_{SV}\right)\right] = 0$$

- V_{ZV} is formed with ZVV, which obviously does not generate any neutral-point current, i_o, because all output terminals are connected to an identical DC-link point, so there is no current flowing in the DC-link capacitors.

Tables 3.6 and 3.7 show the voltage vector combinations that form the virtual small vectors and virtual medium vectors, respectively, for all sectors. By having a set of virtual vectors, the space vector diagram for the NPC VSI modulated using NTV SVM, as shown in Figure 3.6, is obviously different to the diagram given in Figure 3.2. To synthesize a reference output voltage vector, $\overline{V}_{out}$, three nearest virtual vectors are selected based on the triangle that the reference vector is located at the sampling instant.

Referring to Figure 3.5, there are now five triangles (*T1 – T5*) for each sector. The procedures for deriving the duty cycle equations of the selected virtual vectors for each triangle are similar to those given in Section 3.3. Table 3.8 presents the duty cycle equations for the selected virtual vectors in each triangle, where m_u is the modulation index of the NPC VSI (3.9) and θ_{out} is the angle of the reference vector, $\overline{V}_{out}$, within the sector.

- $|\mathbf{V_{SV}}| = \frac{2}{3} V_{DC}$
- $|\mathbf{V_{MV}}| = \frac{4V_{DC}}{3\sqrt{3}}$
- $|\mathbf{V_{LV}}| = \frac{4}{3} V_{DC}$
- $\theta_{VSV1}, \theta_{VLV1} = 0$
- $\theta_{VSV2}, \theta_{VLV2} = \pi/3$
- $\theta_{VMV2} = \pi/6$

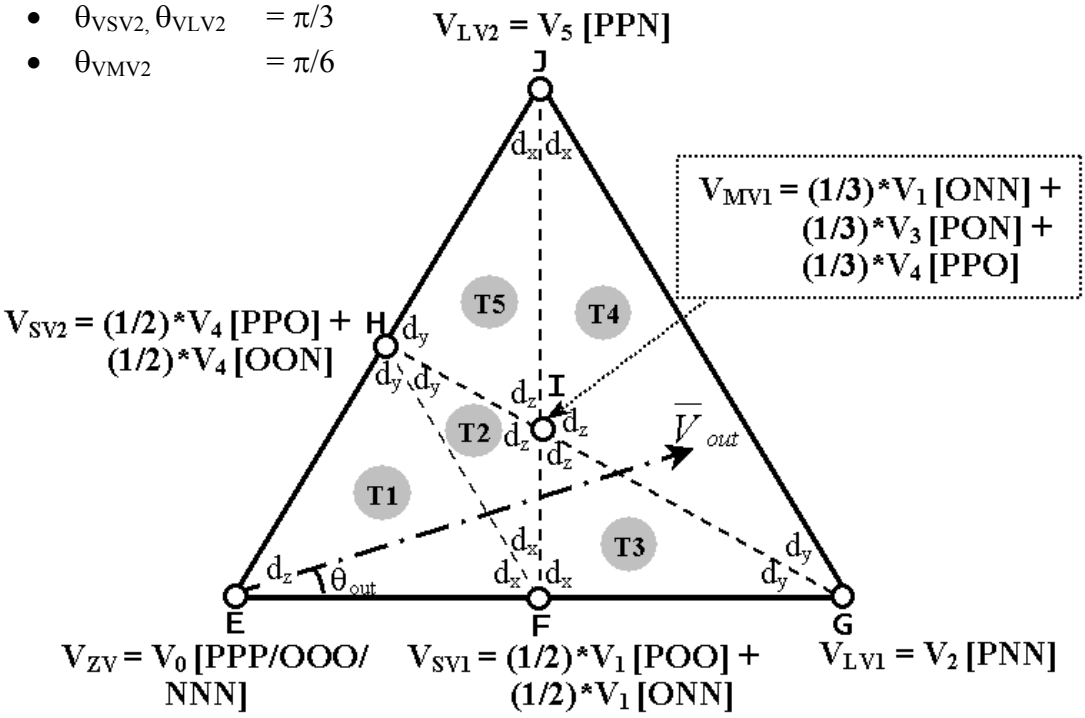


Figure 3.5: Sector 1 of the NPC VSI based on the Nearest Three Virtual Space Vector Modulation

Virtual Small Vector			Vector Combination	
Vector	Magnitude	Angle	Vector with i_o = +*ve*	i_o = - *ve*
V_{SV1}	$\frac{2}{3} V_{DC}$	0	ONN	POO
V_{SV2}	$\frac{2}{3} V_{DC}$	$\pi/3$	PPO	OON
V_{SV3}	$\frac{2}{3} V_{DC}$	$2\pi/3$	NON	OPO
V_{SV4}	$\frac{2}{3} V_{DC}$	π	OPP	NOO
V_{SV5}	$\frac{2}{3} V_{DC}$	$-2\pi/3$	NNO	OOP
V_{SV6}	$\frac{2}{3} V_{DC}$	$-\pi/3$	POP	ONO

Table 3.6: The voltage vector combinations for the virtual small vectors

Virtual medium vector			Vector Combination		
Vector	Magnitude	Angle	Vector with $i_o = i_a$	$i_o = i_b$	$i_o = i_c$
V_{MV1}	$\frac{4}{3\sqrt{3}} V_{DC}$	$\pi/6$	ONN	PON	PPO
V_{MV2}	$\frac{4}{3\sqrt{3}} V_{DC}$	$\pi/2$	OPN	NON	PPO
V_{MV3}	$\frac{4}{3\sqrt{3}} V_{DC}$	$5\pi/6$	OPP	NON	NPO
V_{MV4}	$\frac{4}{3\sqrt{3}} V_{DC}$	$-5\pi/6$	OPP	NOP	NNO
V_{MV5}	$\frac{4}{3\sqrt{3}} V_{DC}$	$-\pi/2$	ONP	POP	NNO
V_{MV6}	$\frac{4}{3\sqrt{3}} V_{DC}$	$-\pi/6$	ONN	POP	PNO

Table 3.7: The voltage vector combinations for the virtual medium vectors

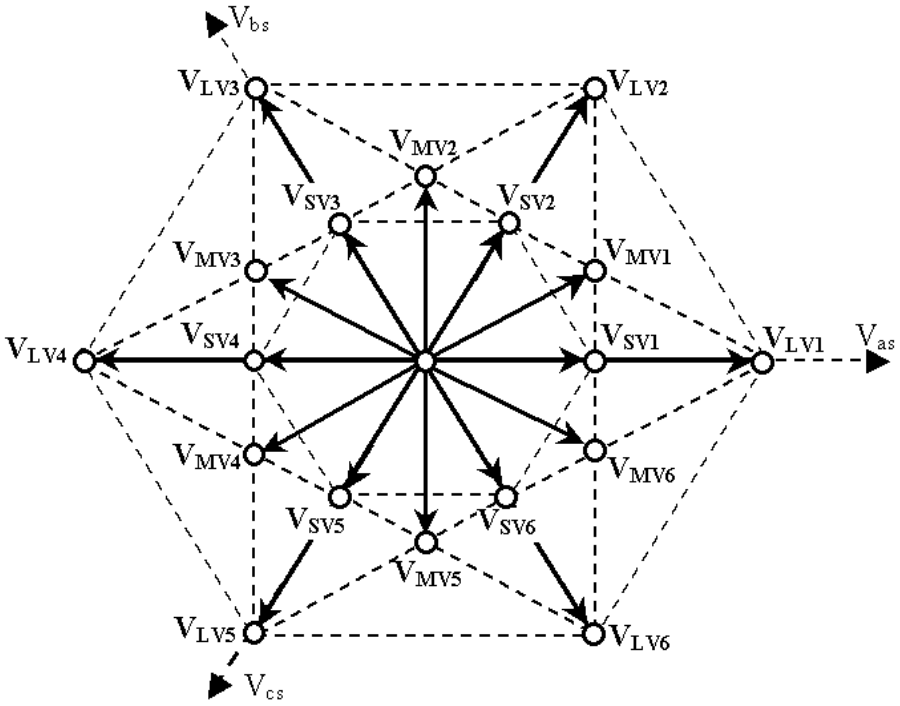


Figure 3.6: The space vector diagram for the three-level neutral-point-clamped voltage source modulated using NTV SVM.

Triangle	d_x	d_y	d_z
T1 [ΔEFH]	$m_u\left(\sqrt{3}\cos\theta_{out}-\sin\theta_{out}\right)$	$2m_u\sin\theta_{out}$	$1-m_u\left(\sqrt{3}\cos\theta_{out}+\sin\theta_{out}\right)$
T2 [ΔFIH]	$2-m_u\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)$	$2-2\sqrt{3}m_u\cos\theta_{out}$	$3m_u\left(\sqrt{3}\cos\theta_{out}+\sin\theta_{out}\right)-3$
T3 [ΔFGI]	$2-m_u\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)$	$\sqrt{3}m_u\cos\theta_{out}-1$	$3m_u\sin\theta_{out}$
T4 [ΔGJI]	$0.5m_u\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)-1$	$2-2\sqrt{3}m_u\cos\theta_{out}$	$1.5m_u\left(\sqrt{3}\cos\theta_{out}-\sin\theta_{out}\right)$
T5 [ΔHIJ]	$0.5m_u\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)-1$	$\sqrt{3}m_u\cos\theta_{out}-1$	$3-1.5m_u\left(\sqrt{3}\cos\theta_{out}+\sin\theta_{out}\right)$

Table 3.8: The duty cycle equations for the selected virtual vectors in each triangle

3.3.2 The switching sequences

In order to generate high quality output waveforms, the even DC-link capacitor voltages have to be maintained so the NTV SVM is applied to the NPC VSI and the following switching sequences are derived based on this modulation scheme. As discussed in Section 3.3.1.1, three nearest virtual vectors are selected to synthesize a reference vector. By determining the duty cycles of the selected virtual vectors, the voltage vectors that form the selected virtual vectors are applied to the output according to the switching sequences presented in Table 3.9.

Let us consider an example where the virtual vectors V_{MV1} (= V_z), V_{LV1} (= V_y) and V_{LV2} (= V_x) are selected to synthesize a reference vector, $\overline{V}_{out}$, that is located in triangle *T4* of sector 1. Based on NTV SVM, these virtual vectors are formed with the voltage vectors: V1 (ONN), V2 (PNN), V3 (PON), V4 (PPO) and V5 (PPN). These voltage vectors are applied to the output according to the switching sequence: PPO – PPN – PON – PNN – ONN, as highlighted in Table 3.9. For a switching period, T_{SW}, the active time of each voltage vector in this switching sequence is determined using equation (3.10). In order to reduce the output harmonic content, the switching sequence is reversed in the next switching cycle so that a double-sided switching sequence is formed.

$$t_1 = t_3 = t_5 = \frac{1}{3} \cdot d_z \cdot T_{SW}$$

$$t_2 = d_x \cdot T_{SW}$$

$$t_4 = d_y \cdot T_{SW} \tag{3.10}$$

3.4 Simulation results

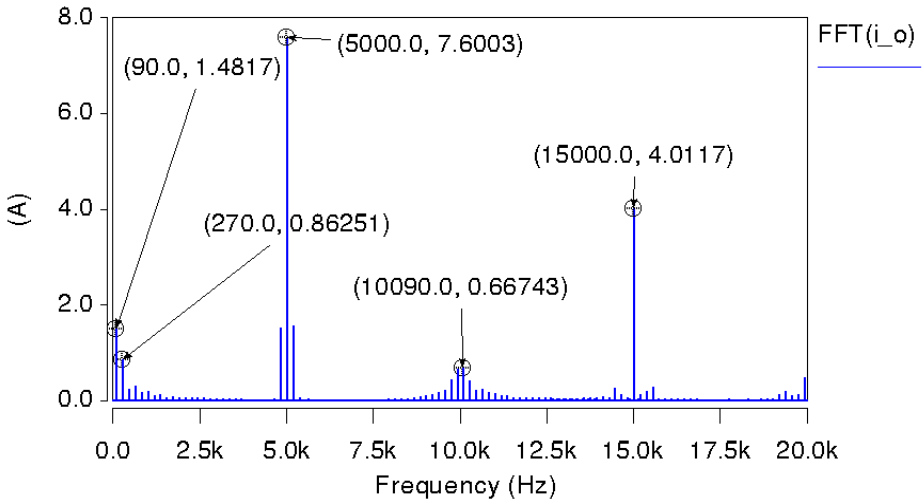
To prove the effectiveness of the NTV SVM in balancing the neutral-point current, the NPC VSI has been simulated using SABER, based on the specifications presented in Appendix A, with both conventional SVM and NTV SVM. For the conventional SVM, the positive and negative small voltage vectors of the selected SVVs are applied with equal active time during each switching sequence. Hence, only the uncompensated

Triangle	Sector	t_1			t_2			t_3			t_4			t_5			t_6			t_7		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T1	1	P	P	P	P	P	O	P	O	O	O	O	O	O	O	N	O	N	N	N	N	N
	2	P	P	P	P	P	O	O	P	O	O	O	O	O	O	N	N	O	N	N	N	N
	3	P	P	P	O	P	P	O	P	O	O	O	O	N	O	O	N	O	N	N	N	N
	4	P	P	P	O	P	P	O	O	P	O	O	O	N	O	O	N	N	O	N	N	N
	5	P	P	P	P	O	P	O	O	P	O	O	O	O	N	O	N	N	O	N	N	N
	6	P	P	P	P	O	P	P	O	O	O	O	O	O	N	O	O	N	N	N	N	N

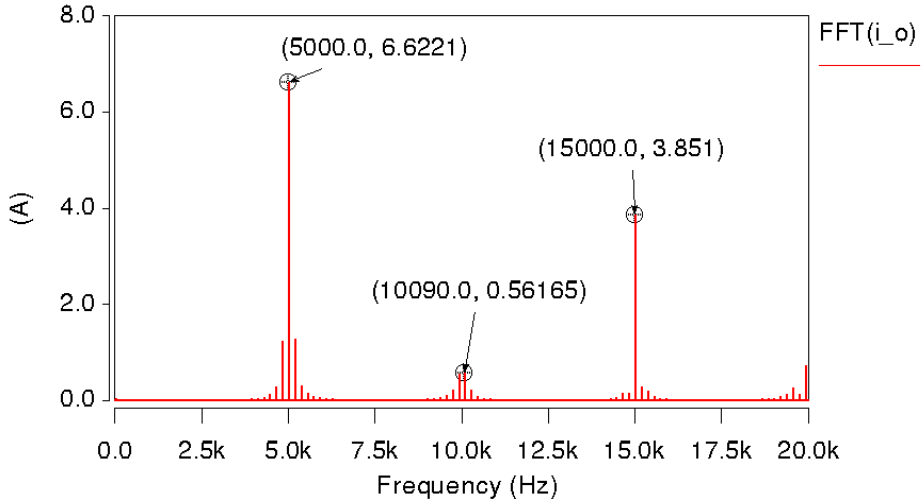
Triangle	Sector	t_1			t_2			t_3			t_4			t_5		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T2	1	P	P	O	P	O	O	P	O	N	O	O	N	O	N	N
	2	P	P	O	O	P	O	O	P	N	O	O	N	N	O	N
	3	O	P	P	O	P	O	N	P	O	N	O	O	N	O	N
	4	O	P	P	O	O	P	N	O	P	N	O	O	N	N	O
	5	P	O	P	O	O	P	O	N	P	O	N	O	N	N	O
	6	P	O	P	P	O	O	P	N	O	O	N	O	O	N	N
T3	1	P	P	O	P	O	O	P	O	N	P	N	N	O	N	N
	2	P	P	O	P	P	N	O	P	N	O	O	N	N	O	N
	3	O	P	P	O	P	O	N	P	O	N	P	N	N	O	N
	4	O	P	P	N	P	P	N	O	P	N	O	O	N	N	O
	5	P	O	P	O	O	P	O	N	P	N	N	P	N	N	O
	6	P	O	P	P	N	P	P	N	O	O	N	O	O	N	N
T4	1	P	P	O	P	P	N	P	O	N	P	N	N	O	N	N
	2	P	P	O	P	P	N	O	P	N	N	P	N	N	O	N
	3	O	P	P	N	P	P	N	P	O	N	P	N	N	O	N
	4	O	P	P	N	P	P	N	O	P	N	N	P	N	N	O
	5	P	O	P	P	N	P	O	N	P	N	N	P	N	N	O
	6	P	O	P	P	N	P	P	N	O	P	N	N	O	N	N
T5	1	P	P	O	P	P	N	P	O	N	O	O	N	O	N	N
	2	P	P	O	O	P	O	O	P	N	N	P	N	N	O	N
	3	O	P	P	N	P	P	N	P	O	N	O	O	N	O	N
	4	O	P	P	O	O	P	N	O	P	N	N	P	N	N	O
	5	P	O	P	P	N	P	O	N	P	O	N	O	N	N	O
	6	P	O	P	P	O	O	P	N	O	P	N	N	O	N	N

Table 3.9: The switching sequences for the three-level neutral-point-clamped voltage source inverter modulated using NTV SVM.

i_o caused by the MVV in the conventional SVM would lead to the neutral-point balancing problem. Operated at a high modulation index (m_u = 0.9), the spectra of i_o for both modulation strategies are shown in Figure 3.7.



(a) Conventional SVM



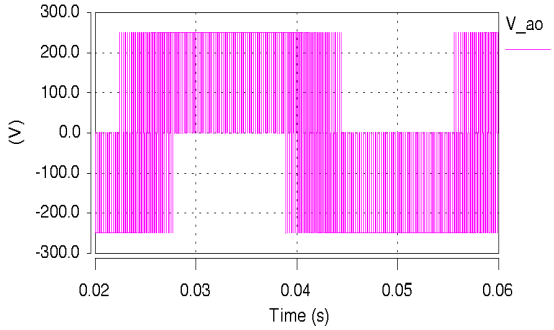
(b) NTV SVM

Figure 3.7: The spectra of the neutral-point current, i_o, for the three-level neutral-point-clamped voltage source inverter

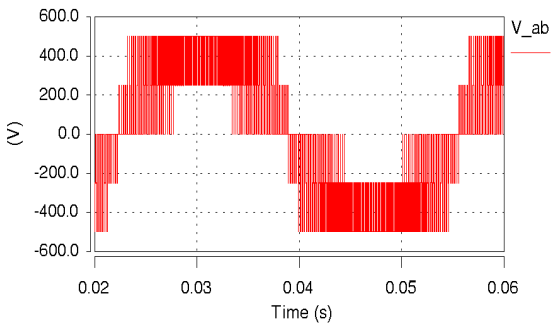
As shown in Figure 3.7(a), using the conventional SVM, the spectrum of i_o shows the presence of low order harmonics around the output frequency (= 30Hz), which proves that the average neutral-point current over a switching period is not maintained at zero. These low order harmonic currents would cause the uneven DC-link capacitor voltages.

By applying NTV SVM to compensate for i_o generated by the MVV, there are no low order harmonic current around the output frequency in the spectrum of i_o, as shown in Figure 3.7(b), verifying that the NTV SVM is effective in controlling the neutral-point balancing problem of the NPC VSI.

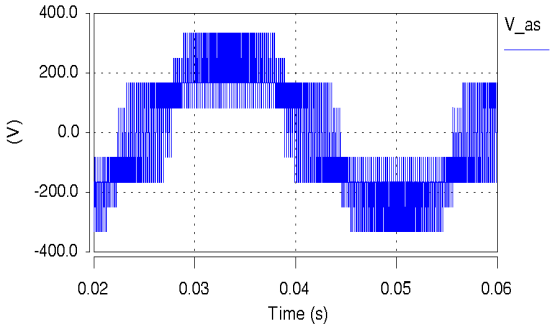
By maintaining the DC-link capacitor voltages, the NPC VSI can be operated to generate multilevel outputs, as shown in Figure 3.8. Having three voltage levels at the DC-links, the NPC VSI is able to generate three-level output terminal voltage V_{ao}, five-level line-to-line for V_{ab} etc at high modulation indexes. To examine whether the voltage levels are properly applied to generate the desired outputs, the load currents of the NPC VSI at a high modulation index (m_u = 0.9) is shown in Figure 3.9 and this shows that the load currents are balanced and sinusoidal.



(a) The output terminal voltage V_{ao}



(b) The line-to-line output voltage V_{ab}



(c) The output phase voltage V_{as}

Figure 3.8: The output voltages generated by the NPC VSI using the NTV SVM

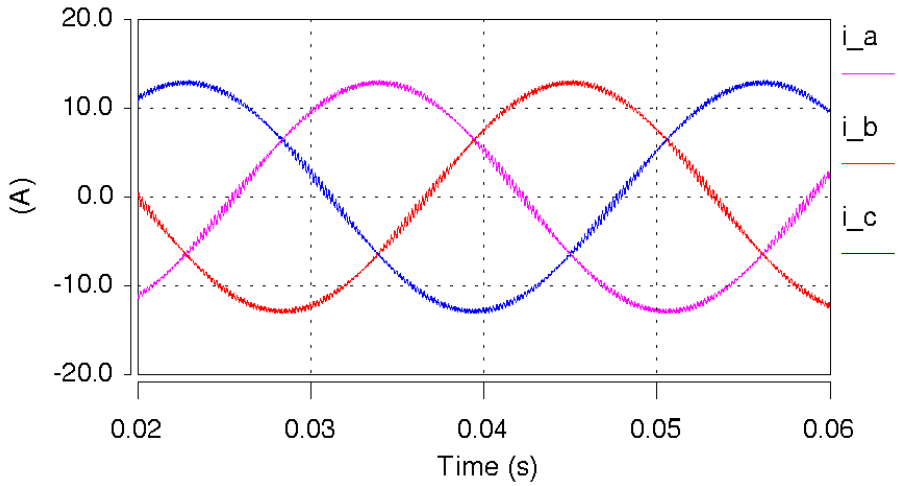


Figure 3.9: The load currents (i_a, i_b and i_c) generated by the three-level neutral-point-clamped voltage source inverter using NTV SVM.

3.5 Conclusions

In this chapter, the operating principles and space vector modulation for the three-level neutral-point-clamped voltage source inverter has been reviewed. Having three voltage levels at the DC links, the three-level neutral-point-clamped voltage source inverter is able to generate three distinctive levels output terminal voltage and five-level output line-to-line voltage. By applying the space vectors concept to compute the duty cycles for the switches, the three-level neutral-point-clamped voltage source inverter can be effectively modulated to apply the DC-link voltage levels to generate the output waveforms so that, on average, the converter output closely resemble a set of balanced, sinusoidal waveforms.

In addition, the neutral-point balancing problem of the three-level neutral-point-clamped voltage source inverter and some control methods have been discussed. In order to control the neutral-point balancing problem, the average neutral-point current over each switching period must be zero so that even DC-link capacitor voltages are maintained and the three-level neutral-point-clamped voltage source inverter is able to generate proper outputs.

Chapter 4

Simplified Three-level Neutral-point-clamped Voltage Source Inverter

4.1 Introduction

The indirect three-level sparse matrix converter is a multilevel neutral-point-clamped matrix converter topology that incorporates the simplified three-level neutral-point-clamped voltage source inverter concept in an indirect matrix based topology. In order to facilitate an explanation of the operating principles and modulation schemes for the indirect three-level sparse matrix converter, this chapter reviews the simplified three-level neutral-point-clamped voltage source inverter technology. Simulation results are presented at the end of this chapter to prove the ability of this topology to generate multilevel outputs and the effectiveness of the modulation scheme in controlling the balance required for neutral point.

4.2 Circuit Topology

Compared to the two-level voltage source inverter, the ability of three-level neutral-point-clamped voltage source inverter to generate higher quality output voltages is well recognised, as discussed in section 3.2. However, the high number of power semiconductor devices requirement is undoubtedly a drawback. To overcome this downside, a simplified three-level neutral-point-clamped voltage source inverter (SNPC VSI) was proposed [43,44], which is able to generate the three-level outputs but requires far fewer power semiconductor devices.

As shown in figure 4.1, the SNPC VSI is a cascaded converter that comprises of a three-level dual-buck stage and a two-level voltage source inverter. Similar to the conventional three-level neutral-point-clamped voltage source inverter, the SNPC VSI

is supplied by two series-connected capacitors (C1 and C2), where both capacitors are charged to an equal potential of V_{DC}. The DC-link middle point '*o*' acts as a zero DC voltage neutral-point. Using the DC-link middle point '*o*' as a reference, there are clearly three output voltage levels available: V_{DC} (V_{po}), 0V and $-V_{DC}$ (V_{no}). At any instant, the three-level dual buck stage is able to supply two of the three voltage levels to the inverter's terminals (*p_inv* and *n_inv*) based on the switching combinations in Table 4.1. To prevent DC-link short circuits, the switching states for S_{B1} and S_{B4} are always opposite to those for S_{B2} and S_{B3}, respectively.

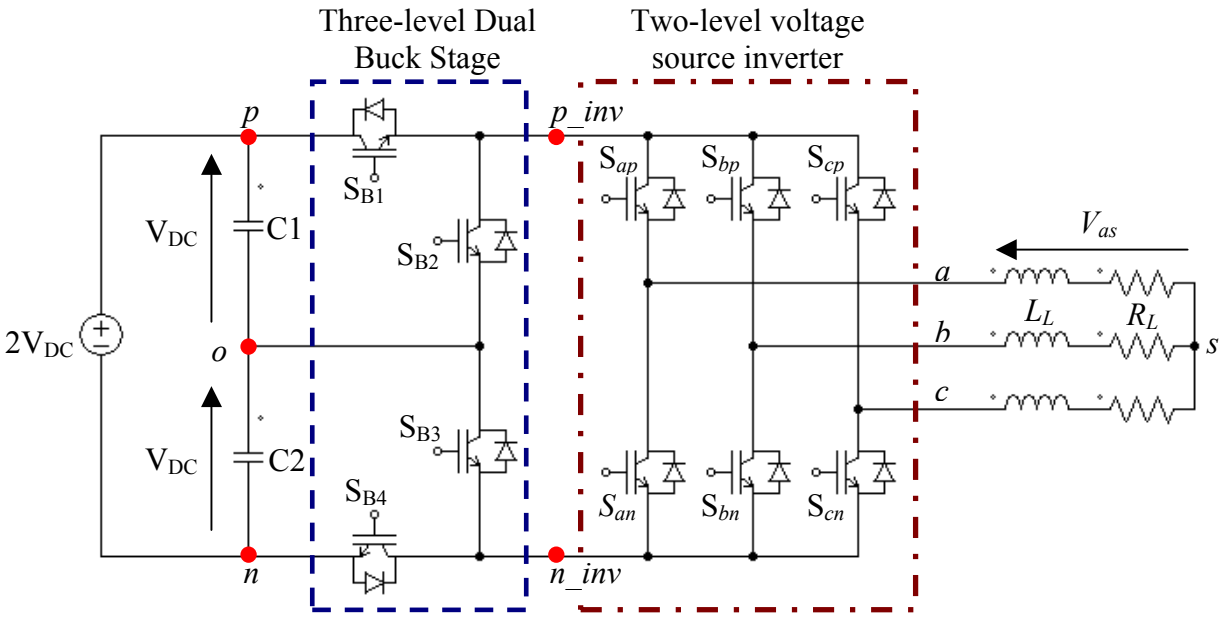


Figure 4.1: The circuit configuration of a simplified three-level neutral-point-clamped voltage source inverter using IGBT switching devices

Switching Combination				Voltage level applied at	
S_{B1}	S_{B2}	S_{B3}	S_{B4}	*p_inv*	*n_inv*
ON	OFF	OFF	ON	V_{DC}	$-V_{DC}$
OFF	ON	OFF	ON	0V	$-V_{DC}$
OFF	ON	ON	OFF	0V	0V
ON	OFF	ON	OFF	V_{DC}	0V

Table 4.1: The switching combinations for the three-level dual buck stage

The two-level voltage source inverter can then be modulated to generate the three-level output according to the switching combinations presented in Table 4.2. The switches in each phase leg of the two-level voltage source inverter are modulated based on the following expression:

$$S_{xp} + S_{xn} = 1 \qquad x \in \{a, b, c,\} \tag{4.1}$$

where S_{xp} and S_{xn} are the switching functions of the top and bottom unidirectional switches, respectively. As shown in Table 4.2, each output terminal voltage (V_{xo}) of the SNPC VSI has three possible voltage levels: V_{DC}, 0V and $-V_{DC}$. These levels show the ability of the converter to generate multilevel outputs as the conventional three-level neutral-point-clamped voltage source inverter.

Buck stage				Voltage source inverter		Output terminal voltage, V_{xo}
S_{B1}	S_{B2}	S_{B3}	S_{B4}	S_{xp}	S_{xn}	
ON	OFF	OFF	ON	ON	OFF	V_{DC}
ON	OFF	ON	OFF	ON	OFF	V_{DC}
ON	OFF	OFF	ON	OFF	ON	$-V_{DC}$
OFF	ON	OFF	ON	OFF	ON	$-V_{DC}$
OFF	ON	OFF	ON	ON	OFF	0V
OFF	ON	ON	OFF	ON	OFF	0V
OFF	ON	ON	OFF	OFF	ON	0V
ON	OFF	ON	OFF	OFF	ON	0V

Table 4.2: The valid switching combinations for the switches in each phase leg of the inverter (x $\in$ {a, b, c}) and the three-level dual buck stage

Representing each DC-link voltage level with a switching state: $P = V_{po} = V_{DC}$, $O = 0V$ and $N = V_{no} = -V_{DC}$, a three-phase SNPC VSI is able to generate twenty-one switching states, as shown in Table 4.3. These states represent the DC-link voltage levels connected to the output terminals (*a*, *b* and *c*). For example, the switching state *POO* signifies that the three-level dual buck stage supplies the voltage level *P* to the inverter's terminal '*p_inv*' and *O* to terminal '*n_inv*' while the two-level inverter connects the voltage level *P* to the output terminal '*a*' and *O* to terminals '*b*' and '*c*'. Compared to the switching states achieved by a conventional three-level neutral-point-clamped voltage source inverter listed in Table 3.2, the SNPC VSI is able to achieve most of the switching states except the six that require each output terminal to be connected to different voltage levels. This is because, at any instant, only two DC-link voltage levels can be supplied to the two-level voltage source inverter.

To determine the output phase (line-to-load neutral) and output line-to-line voltages generated by each switching state of the SNPC VSI, equations (4.2) and (4.3) are derived based on equations (3.1) – (3.3). The variables m_{x1} and m_{x2} represent the switch combinations (S_{B1} & S_{xp}) and (S_{B4} & S_{xn}). m_{x1} and m_{x2} equal one when both switches in the combination are 'on' or zero otherwise. Assuming a star-connected load applied to the SNPC VSI, as shown in Figure 4.1, the output phase and output line-to-line voltages generated by each switching state are presented in Table 4.3. This table clearly shows that the SNPC VSI is able to produce five distinct levels ($\pm 2V_{DC}$, $\pm V_{DC}$ and 0V) for the output line-to-line voltages.

$$V_{ab} = V_{DC}(m_{a1} - m_{a2} - m_{b1} + m_{b2})$$

$$V_{bc} = V_{DC}(m_{b1} - m_{b2} - m_{c1} + m_{c2})$$

$$V_{ca} = V_{DC}(m_{c1} - m_{c2} - m_{a1} + m_{a2}) \qquad (4.2)$$

$$V_{as} = (2/3).V_{DC}[m_{a1} - m_{a2} - (1/2)(m_{b1} - m_{b2} + m_{c1} - m_{c2})]$$

$$V_{bs} = (2/3).V_{DC}[m_{b1} - m_{b2} - (1/2)(m_{a1} - m_{a2} + m_{c1} - m_{c2})]$$

$$V_{cs} = (2/3).V_{DC}[m_{c1} - m_{c2} - (1/2)(m_{a1} - m_{a2} + m_{b1} - m_{b2})] \qquad (4.3)$$

Switching State Combination			Output phase voltages			Output line-to-line voltages		
a	*b*	*c*	V_{as}	V_{bs}	V_{cs}	V_{ab}	V_{bc}	V_{ca}
P	P	P	0	0	0	0	0	0
O	O	O	0	0	0	0	0	0
N	N	N	0	0	0	0	0	0
P	O	O	$\frac{2}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	V_{DC}	0	$-V_{DC}$
O	P	O	$-\frac{1}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$-V_{DC}$	V_{DC}	0
O	O	P	$-\frac{1}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	0	$-V_{DC}$	V_{DC}
P	P	O	$\frac{1}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	0	V_{DC}	$-V_{DC}$
O	P	P	$-\frac{2}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$-V_{DC}$	0	V_{DC}
P	O	P	$\frac{1}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	V_{DC}	$-V_{DC}$	0
N	O	O	$-\frac{2}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$-V_{DC}$	0	V_{DC}
O	N	O	$\frac{1}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	V_{DC}	$-V_{DC}$	0
O	O	N	$\frac{1}{3}\cdot V_{DC}$	$\frac{1}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	0	V_{DC}	$-V_{DC}$
N	N	O	$-\frac{1}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	0	$-V_{DC}$	V_{DC}
O	N	N	$\frac{2}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	V_{DC}	0	$-V_{DC}$
N	O	N	$-\frac{1}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$-\frac{1}{3}\cdot V_{DC}$	$-V_{DC}$	V_{DC}	0
P	N	N	$\frac{4}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$2\cdot V_{DC}$	0	$-2\cdot V_{DC}$
P	P	N	$\frac{2}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$-\frac{4}{3}\cdot V_{DC}$	0	$2\cdot V_{DC}$	$-2\cdot V_{DC}$
N	P	P	$-\frac{4}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$-2\cdot V_{DC}$	0	$2\cdot V_{DC}$
N	N	P	$-\frac{2}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$\frac{4}{3}\cdot V_{DC}$	0	$-2\cdot V_{DC}$	$2\cdot V_{DC}$
P	N	P	$\frac{2}{3}\cdot V_{DC}$	$-\frac{4}{3}\cdot V_{DC}$	$\frac{2}{3}\cdot V_{DC}$	$2\cdot V_{DC}$	$-2\cdot V_{DC}$	0
N	P	N	$-\frac{2}{3}\cdot V_{DC}$	$\frac{4}{3}\cdot V_{DC}$	$-\frac{2}{3}\cdot V_{DC}$	$-2\cdot V_{DC}$	$2\cdot V_{DC}$	0

Table 4.3: Switching states for the simplified three-level neutral-point-clamped voltage source inverter

Compared to the conventional three-level neutral-point-clamped voltage source inverter, the circuit configuration of the SNPC VSI is simpler, using only ten switching devices. Even though the SNPC VSI is not able to achieve certain switching states that require each output to be connected to different voltage levels, it is still able to generate three distinctive levels for the output terminal voltages and five-level for the output line-to-line voltages. This number of levels can improve the quality of the output waveforms compared to a two-level voltage source inverter.

To modulate the SNPC VSI to generate a set of sinusoidal and balanced output waveforms, suitable modulation methods have been proposed [43,44]. In the following section, a space vector modulation (SVM) that was proposed by the Author in [44] is described because it constitutes the foundation for a space vector modulation proposed for the indirect three-level sparse matrix converter. Due to the ability of the converter to connect the output terminal(s) to neutral-point '*o*', the SNPC VSI inevitably inherits the neutral-point balancing problem. Therefore, the neutral-point balancing problem in the SNPC VSI and a suitable control method will also be discussed.

4.3 Space Vector Modulation

SVM is a pulse-width modulation strategy that uses the concept of space vectors to compute the duty cycles of the switches. To implement this modulation strategy for the SNPC VSI, the output phase voltages generated by the switching states of the SNPC VSI have to be converted into space vectors using the following transformation:

$$\overline{V} = \frac{2}{3}\left(V_{as} + V_{bs} e^{j\frac{2}{3}\pi} + V_{cs} e^{-j\frac{2}{3}\pi} \right) \tag{4.4}$$

For the SNPC VSI, all switching states listed in Table 4.3 can be transformed into thirteen distinctive voltage space vectors with fixed directions, as shown in Table 4.4. Based on their magnitudes, these voltage space vectors can be divided into three groups: zero voltage vector ZVV (V_0), small voltage vectors SVV (V_1, V_3, V_5, V_7, V_9 and V_{11}) and large voltage vectors LVV (V_2, V_4, V_6, V_8, V_{10} and V_{12}). Figure 4.2 shows the space vector diagram of the SNPC VSI that is formed by these voltage space vectors.

Compared to the space vector diagram of the conventional three-level neutral-point-clamped voltage source inverter given in Figure 3.2, the SNPC VSI is clearly not able to produce the medium voltage vector due to its inability to connect each output terminal to different voltage levels. The ZVV and SVV have redundant switching state combinations that offer additional degree of freedom in the synthesize of the output voltage vector, which are useful to ensure minimum switching transition in a switching sequence and allow the control needed for the neutral-point balancing problem.

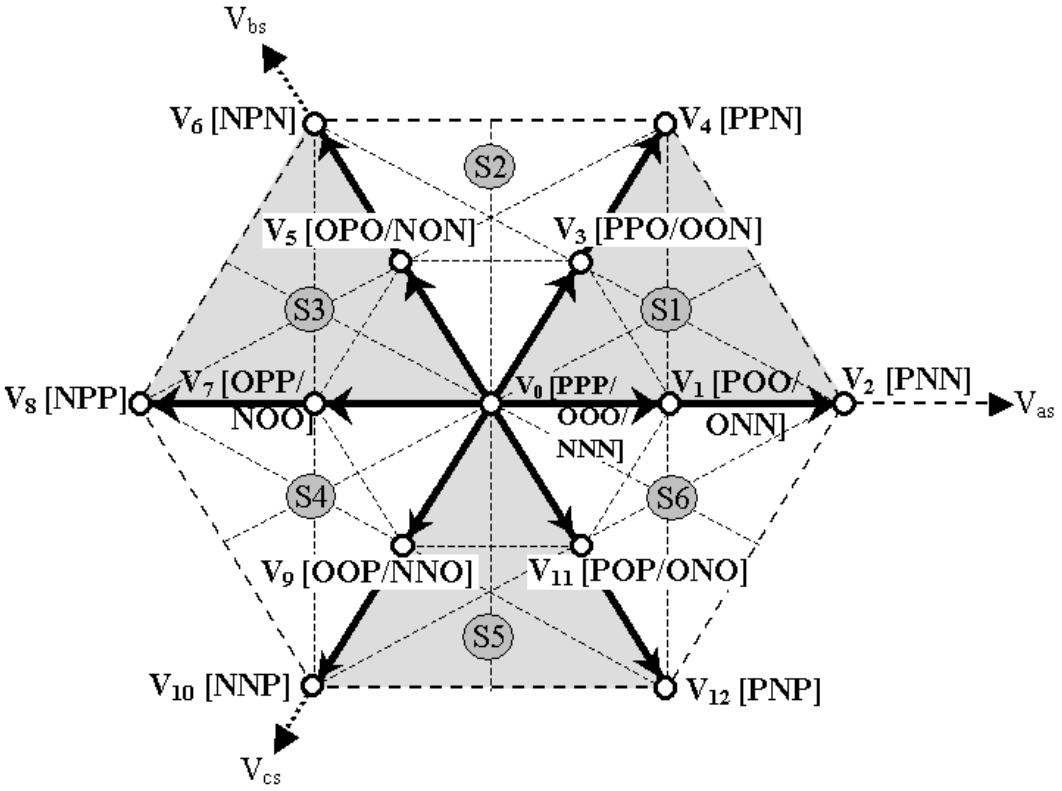


Figure 4.2: The space vector diagram for the simplified three-level neutral-point-clamped voltage source inverter

As mentioned earlier, a set of sinusoidal and balanced output voltages is normally the desired output for the SNPC VSI. Using the space vector transformation (4.4), this set of time-varying signals is transformed into a reference output voltage vector, $\overline{V}_{out}$, that rotates along a circular trajectory with frequency ω_o in the space vector diagram. This reference output voltage vector can be expressed as:

$$\overline{V}_{out} = V_{om} e^{j(\omega_o t - \varphi_o)} = V_{om} \angle \theta_o \tag{4.5}$$

Switching state combination			Output voltage vectors		
a	*b*	*c*	Vector	Magnitude	Angle
P	P	P	V_0	0V	0
O	O	O			
N	N	N			
P	O	O	V_1	$\frac{2}{3} V_{DC}$	0
O	N	N			
P	N	N	V_2	$\frac{4}{3} V_{DC}$	0
P	P	O	V_3	$\frac{2}{3} V_{DC}$	$\pi/3$
O	O	N			
P	P	N	V_4	$\frac{4}{3} V_{DC}$	$\pi/3$
O	P	O	V_5	$\frac{2}{3} V_{DC}$	$2\pi/3$
N	O	N			
N	P	N	V_6	$\frac{4}{3} V_{DC}$	$2\pi/3$
O	P	P	V_7	$\frac{2}{3} V_{DC}$	π
N	O	O			
N	P	P	V_8	$\frac{4}{3} V_{DC}$	π
O	O	P	V_9	$\frac{2}{3} V_{DC}$	$-2\pi/3$
N	N	O			
N	N	P	V_{10}	$\frac{4}{3} V_{DC}$	$-2\pi/3$
P	O	P	V_{11}	$\frac{2}{3} V_{DC}$	$-\pi/3$
O	N	O			
P	N	P	V_{12}	$\frac{4}{3} V_{DC}$	$-\pi/3$

Table 4.4: The magnitude and angle of each voltage space vector formed by the switching state of the SNPC VSI using the space vector transformation.

where V_{om} is the magnitude and θ_o (= $\omega_o t$ - φ_o) is the direction of the reference vector. $\omega_o t$ is the angle of the output phase voltage and φ_o is an arbitrary angle. The reference vector can be synthesized with three nearest space vectors that are selected based on the triangle that the reference vector is located at the sampling instant. Referring to Figure 4.2, the space vector diagram for the SNPC VSI is divided into six sectors (S1 – S6), which each sector consists of eight small triangles.

Due to the circular symmetry of a three-phase system, it is sufficient to analyze the procedure for synthesizing a reference vector, $\overline{V}_{out}$, which is located in sector S1 ($0 \le \theta_o < 60^0$) to derive the duty cycle equations for the selected vectors in each triangle. To facilitate this explanation, Figure 4.3 shows sector S1 of the space vector diagram for the SNPC VSI. Let us consider an example where the reference vector, $\overline{V}_{out}$, is located in triangle *T7* at the sampling instant. The selected voltage vectors are: V_2, V_3 and V_4. For a switching period, T_{SW}, this reference output voltage vector is synthesized using equation (4.6) based on the constraint $d_{V2} + d_{V3} + d_{V4} = 1$, where d_{V2}, d_{V3} and d_{V4} are duty cycles that represent the active times of the selected vectors within the switching period, $T_{SW.}$

$$\overline{V}_{out} = d_{V2}V_2 + d_{V3}V_3 + d_{V4}V_4 \tag{4.6}$$

The duty cycle equations of the selected voltage vectors can be derived as follow:

1. Specify the voltage vector V_2 as the reference axis and its magnitude as unit. Each voltage vector and the reference vector can then be expressed as:

$$V_2 = 1 \; ; \; V_3 = \frac{\sqrt{3}}{2} e^{j\frac{\pi}{6}} \; ; \; V_4 = \frac{1}{2} e^{j\frac{\pi}{3}} \; ; \; \overline{V}_{out} = V_{opu} \cdot e^{j\theta_{out}} \tag{4.7}$$

where $V_{opu} = \dfrac{V_{om}}{4V_{dc}/3}$

2. Substitute (4.7) into (4.6) and then convert (4.6) into trigonometric form:

$$V_{opu}\left(\cos\theta_{out} + j\sin\theta_{out}\right) = d_{V2} + \frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6} + j\sin\frac{\pi}{6}\right)\cdot d_{V3} + \frac{1}{2}\left(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}\right)\cdot d_{V4}$$

3. Separate the real and imaginary parts from the equation above:

Real: $$d_{V2} + \frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6}\right)\cdot d_{V3} + \frac{1}{2}\left(\cos\frac{\pi}{3}\right)\cdot d_{V4} = V_{opu}\left(\cos\theta_{out}\right)$$

Imaginary: $$\frac{\sqrt{3}}{2}\left(\sin\frac{\pi}{6}\right)\cdot d_{V3} + \frac{1}{2}\left(\sin\frac{\pi}{3}\right)\cdot d_{V4} = V_{opu}\left(\sin\theta_{out}\right)$$

4. Solve the real and imaginary parts using the constraint $d_{V2} + d_{V3} + d_{V4} = 1$.

5. The equations for the duty cycles d_{V2}, d_{V3} and d_{V4} of triangle *T7* are then determined:

$$d_{V2} = 0.5 \cdot m_u\left(\sqrt{3}\cdot\cos\theta_{out} - \sin\theta_{out}\right)$$

$$d_{V3} = 2 - m_u\left(\sqrt{3}\cdot\cos\theta_{out} + \sin\theta_{out}\right)$$

$$d_{V4} = 0.5 \cdot m_u\left(\sqrt{3}\cdot\cos\theta_{out} + 3\cdot\sin\theta_{out}\right) - 1 \qquad (4.8)$$

where

$$m_u = \frac{2\cdot V_{opu}}{\sqrt{3}} = \frac{\sqrt{3}\cdot V_{om}}{2\cdot V_{DC}} \text{ is the modulation index } (0 \le m_u \le 1) \qquad (4.9)$$

and θ_{out} is the angle of the reference vector, $\overline{V}_{out}$, within the sector. For the other triangles, the duty cycle equations for the selected voltage vectors can be derived using the same procedure. Table 4.5 presents the duty cycle equations of the selected voltage vectors for all triangles within a sector.

By determining the duty cycles of the selected voltage vectors, the duty cycles for the switches, over a switching period, can be determined. To complete the modulation process, selected vectors are applied to the output according to a switching sequence. For the SNPC VSI, a switching sequence should be formed in such a way that high quality output waveforms are obtained with minimum number of switching transitions and allow the neutral-point balancing problem to be controlled.

- $|V_{V1}| = |V_{V3}| = 2V_{DC}/3$
- $|V_{V2}| = |V_{V4}| = 4V_{DC}/3$
- $\theta_{V1}, \theta_{V2} = 0$
- $\theta_{V3}, \theta_{V4} = \pi/3$

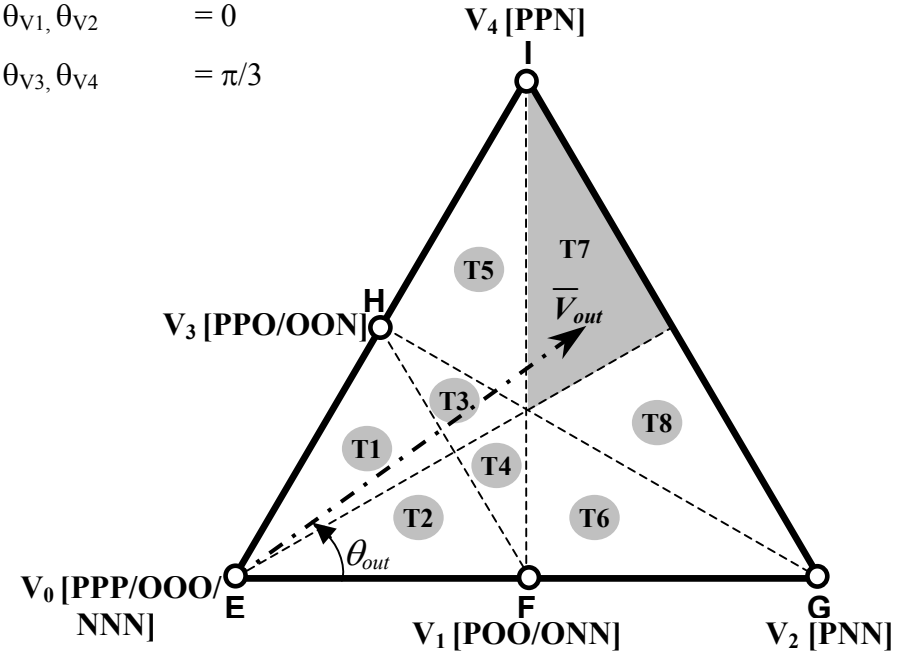


Figure 4.3: Sector 1 of the space vector diagram for the simplified three-level neutral-point-clamped voltage source inverter

Similar to the conventional three-level neutral-point-clamped voltage source inverter, the neutral-point balancing problem of the SNPC VSI is due to uneven charging/discharging of the DC-link capacitors (C1 and C2). As shown in Table 4.2, each output terminal of the SNPC VSI can be connected to the DC-link middle point '*o*' to form the zero voltage level (V_{xo} = 0V). However, whenever the output terminal is connected to point '*o*', the neutral-point current, i_o, can cause uneven charging or discharging of the DC-link capacitors, depends on the loading condition. As an example, Figure 4.4 illustrates how certain switching states affect the voltage levels of the capacitors when the DC-link middle point '*o*' is connected to the output terminal(s). Without proper control, the uneven changing voltage levels of the DC-link capacitors would impact on the ability of the SNPC VSI to properly generate the three-level output waveform, causing output voltage distortion.

Triangle	Duty cycle equations
T1/T2 (ΔEFH)	• $d_{V0} = 1 - m_u\left(\sqrt{3}\cdot\cos\theta_{out} + \sin\theta_{out}\right)$ • $d_{V1} = m_u\left(\sqrt{3}\cdot\cos\theta_{out} - \sin\theta_{out}\right)$ • $d_{V3} = 2\cdot m_u\cdot\sin\theta_{out}$
T3/T5 (ΔFHI)	• $d_{V1} = m_u\left(\sqrt{3}\cdot\cos\theta_{out} - \sin\theta_{out}\right)$ • $d_{V3} = 2 - 2\cdot\sqrt{3}\cdot m_u\cdot\sin\theta_{out}$ • $d_{V4} = m_u\left(\sqrt{3}\cdot\cos\theta_{out} + \sin\theta_{out}\right) - 1$
T4/T6 (ΔFHG)	• $d_{V1} = 2 - m_u\left(\sqrt{3}\cdot\cos\theta_{out} + 3\sin\theta_{out}\right)$ • $d_{V2} = m_u\left(\sqrt{3}\cdot\cos\theta_{out} + \sin\theta_{out}\right) - 1$ • $d_{V3} = 2\cdot m_u\cdot\sin\theta_{out}$
T7 (ΔHIG)	• $d_{V2} = 0.5\cdot m_u\left(\sqrt{3}\cdot\cos\theta_{out} - \sin\theta_{out}\right)$ • $d_{V3} = 2 - m_u\left(\sqrt{3}\cdot\cos\theta_{out} + \sin\theta_{out}\right)$ • $d_{V4} = 0.5\cdot m_u\left(\sqrt{3}\cdot\cos\theta_{out} + 3\cdot\sin\theta_{out}\right) - 1$
T8 (ΔFGI)	• $d_{V1} = 2 - m_u\left(\sqrt{3}\cdot\cos\theta_{out} + 3\sin\theta_{out}\right)$ • $d_{V2} = \sqrt{3}\cdot m_u\cdot\cos\theta_{out} - 1$ • $d_{V4} = m_u\cdot\sin\theta_{out}$

Table 4.5: The duty cycle equations for the selected voltage vectors in each triangle

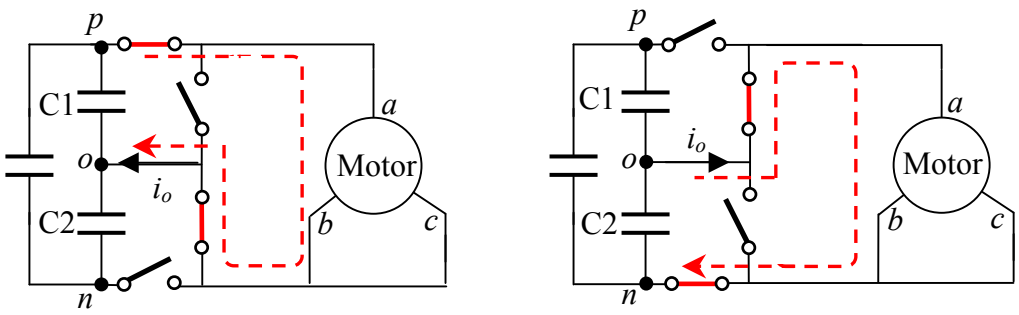


Figure 4.4: The neutral-point balancing problem caused by the switching states (a) POO (b) ONN

In SVM, only the SVV causes the uneven changing voltage levels of the DC-link capacitors due to the connection of the output to the neutral-point. Table 4.5 presents the neutral-point current, i_o, generated by the SVV. Similar to the conventional three-level neutral-point-clamped voltage source inverter, for each SVV, the switching state that connects the output phase current with positive sign to the DC-link middle point '*o*' can be referred to as the 'positive small voltage vector' while the switching state that connects the output phase current with negative sign is referred to as the 'negative small voltage vector'.

Positive Small Voltage Vectors	i_o	Negative Small Voltage Vectors	i_o
ONN	i_a	POO	$-i_a$
PPO	i_c	OON	$-i_c$
NON	i_b	OPO	$-i_b$
OPP	i_a	NOO	$-i_a$
NNO	i_c	OOP	$-i_c$
POP	i_b	ONO	$-i_b$

Table 4.6: The neutral-point current, i_o, generated by the small voltage vectors

In order to maintain the voltage levels of the DC-link capacitors, SVV(s) should be applied in such a way that the average neutral-point current over a switching period is maintained at zero. Referring to Table 4.6, the positive and negative small voltage vectors of a SVV apparently connect the same output phase current to the neutral-point but with opposite sign. Hence, by applying both switching states of a selected SVV with equal active time in a switching sequence, the i_o can be balanced and zero average neutral-point current over a switching period can be obtained. For example, the small voltage vector V_1 is selected for an interval t_{V1}. In order to balance the i_o, *POO* and *ONN* have to be equally applied for (1/2)*t_{V1}. As a result, the average neutral-point current during this interval will be:

$$\left(1/t_{V1}\right)\left[\left(-i_a * \tfrac{1}{2} * t_{V1}\right) + \left(i_a * \tfrac{1}{2} * t_{V1}\right)\right] = 0$$

4.3.1 Switching sequences

Knowing that the DC-link capacitor voltages must be maintained in order to generate high quality output waveforms, the switching sequences for the SNPC VSI are formed in such a way that the positive and negative small voltage vectors of the selected SVVs are equally applied to the output, as presented in Tables 4.7 – 4.9.

Let us consider an example when the reference vector, $\overline{V}_{out}$, is located in triangle *T7* of sector S1. The voltage vectors V_2 (PNN), V_3 (PPO/OON) and V_4 (PPN) are selected to synthesize this reference vector. The switching sequence highlighted in Table 4.9 is used to apply the selected voltage vectors to the output. For a switching period, T_{SW}, the active time of each voltage vector within this switching sequence is determined with equation (4.10). To improve the output harmonic content the switching sequence is reversed in the next switching cycle so that a double-sided switching sequence is formed [13].

$$t_1 = t_4 = \left(1/2\right) \cdot d_{V3} \cdot T_{SW}$$

$$t_2 = d_{V4} \cdot T_{SW}$$

$$t_3 = d_{V2} \cdot T_{SW} \tag{4.10}$$

Triangle	Sector	t_1			t_2			t_3			t_4			t_5			t_6			t_7		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T1/T2 (ΔEFH)	1	P	P	P	P	P	O	P	O	O	O	O	O	O	O	N	O	N	N	N	N	N
	2	P	P	P	P	P	O	O	P	O	O	O	O	O	O	N	N	O	N	N	N	N
	3	P	P	P	O	P	P	O	P	O	O	O	O	N	O	O	N	O	N	N	N	N
	4	P	P	P	O	P	P	O	O	P	O	O	O	N	O	O	N	N	O	N	N	N
	5	P	P	P	P	O	P	O	O	P	O	O	O	O	N	O	N	N	O	N	N	N
	6	P	P	P	P	O	P	P	O	O	O	O	O	O	N	O	O	N	N	N	N	N

Table 4.7: The switching sequences for triangles T1 and T2

Triangle	Sector	t_1			t_2			t_3			t_4			t_5		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T3/T5 (ΔFHI)	1	P	O	O	P	P	O	P	P	N	O	O	N	O	N	N
	2	P	P	O	O	P	O	N	P	N	N	O	N	O	O	N
	3	O	P	O	O	P	P	N	P	P	N	O	O	N	O	N
	4	O	P	P	O	O	P	N	N	P	N	N	O	N	O	O
	5	O	O	P	P	O	P	P	N	P	O	N	O	N	N	O
	6	P	O	P	P	O	O	P	N	N	O	N	N	O	N	O
T4/T6 (ΔFHG)	1	P	P	O	P	O	O	P	N	N	O	N	N	O	O	N
	2	O	P	O	P	P	O	P	P	N	O	O	N	N	O	N
	3	O	P	P	O	P	O	N	P	N	N	O	N	N	O	O
	4	O	O	P	O	P	P	N	P	P	N	O	O	N	N	O
	5	P	O	P	O	O	P	N	N	P	N	N	O	O	N	O
	6	P	O	O	P	O	P	P	N	P	O	N	O	O	N	N

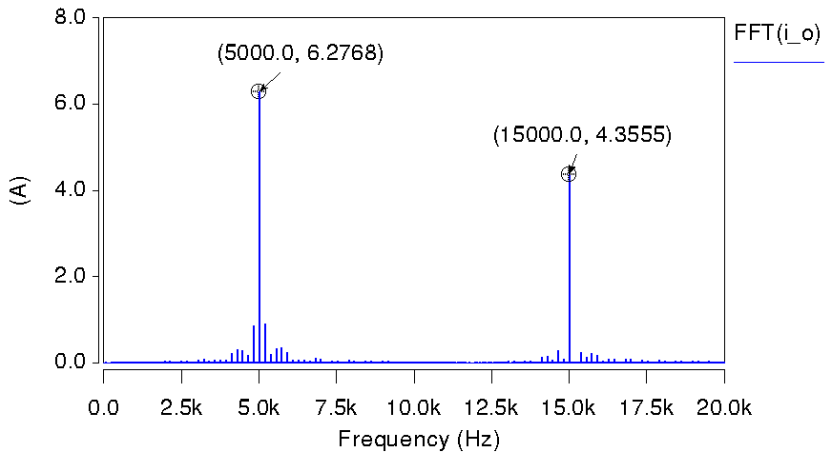
Table 4.8: The switching sequences for triangles T3 to T6

Triangle	Sector	t_1			t_2			t_3			t_4		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T7 (ΔHIG)	1	P	P	O	P	P	N	P	N	N	O	O	N
	2	O	P	O	N	P	N	P	P	N	N	O	N
	3	O	P	P	N	P	P	N	P	N	N	O	O
	4	O	O	P	N	N	P	N	P	P	N	N	O
	5	P	O	P	P	N	P	N	N	P	O	N	O
	6	P	O	O	P	N	N	P	N	P	O	N	N
T8 (ΔFGI)	1	P	O	O	P	N	N	P	P	N	O	N	N
	2	P	P	O	P	P	N	N	P	N	O	O	N
	3	O	P	O	N	P	N	N	P	P	N	O	N
	4	O	P	P	N	P	P	N	N	P	N	O	O
	5	O	O	P	N	N	P	P	N	P	N	N	O
	6	P	O	P	P	N	P	P	N	N	O	N	O

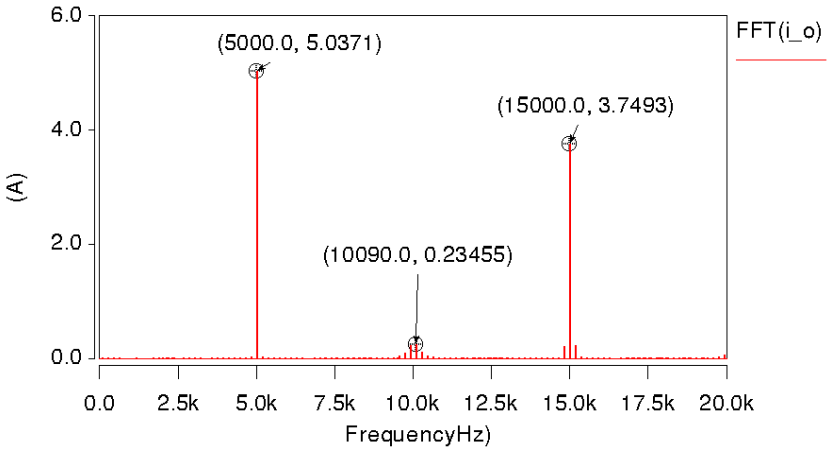
Table 4.9: The switching sequences for triangles T7 and T8

4.4 Simulation results

To prove the effectiveness of the SVM in balancing the neutral-point current, the SNPC VSI has been simulated using SABER at high (m_u = 0.9) and low (m_u = 0.4) modulation indexes, based on the specifications presented in Appendix A. The spectra of the neutral-point current, i_o, for both modulation indexes are shown in Figure 4.5. By applying the positive and negative SVVs with equal active time in the switching sequences the spectra of i_o, shown in Figure 4.5, shows no low order harmonic around the output frequency (= 30Hz). This result verifies that the neutral-point current generated by the SVVs is effectively balanced and the average neutral-point current over a switching period is maintained at zero, keeping the voltage levels of the DC-link capacitors from changing unevenly.



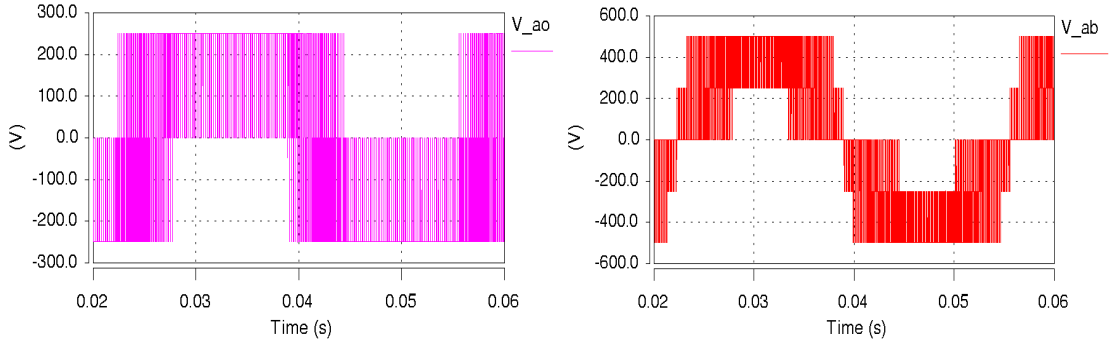
(a) High modulation index



(b) Low modulation index

Figure 4.5: The spectra of the neutral-point current, i_o, for the simplified three-level neutral-point-clamped voltage source inverter.

By maintaining the voltage levels of the DC-link capacitors, the SNPC VSI can be operated to generate multilevel outputs, as shown in Figure 4.6. Having three voltage levels at the DC-links, the SNPC VSI is able to generate three distinctive levels for the output terminal voltage V_{ao} and five-level line-to-line for V_{ab} at high modulation indexes. To examine whether the DC-link voltage levels are properly applied to generate the desired outputs, the load currents of the SNPC VSI at a high modulation index (m_u = 0.9) is shown in Figure 4.7. This figure clearly shows that the load currents are balanced and sinusoidal.



(a) The output terminal voltage, V_{ao} (b) The output line-to-line voltage, V_{ab}

Figure 4.6: The output voltages generated by the SNPC VSI

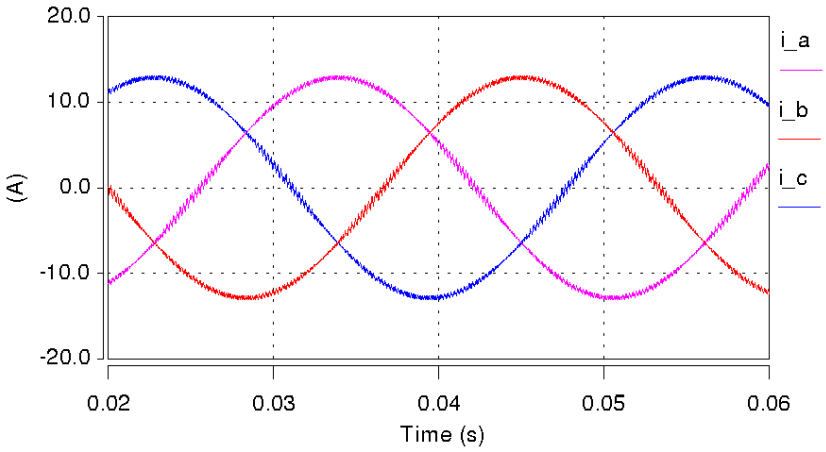


Figure 4.7: The load currents (i_a, i_b and i_c) generated by the simplified three-level neutral-point-clamped voltage source inverter

4.5 Conclusions

In this chapter, the operating principles and space vector modulation for the simplified three-level neutral-point-clamped voltage source inverter have been reviewed. Having three voltage levels at the DC links, the simplified three-level neutral-point-clamped voltage source inverter is able to generate three-level output terminal voltages and five-level output line-to-line voltages. By applying space vector modulation, the simplified three-level neutral-point-clamped voltage source inverter can be effectively modulated to generate the output waveforms so that, on average, the converter output closely resemble a set of balanced, sinusoidal waveforms.

In addition, the neutral-point balancing problem of this topology and associated control method has been discussed. To maintain the DC-link capacitor voltages, the average neutral-point current over a switching period must be zero. The redundant switching states of the selected small voltage vectors must therefore be equally applied to the output in each switching sequence during steady state operation.

Chapter 5

Three-level-output-stage Matrix Converter

5.1 Introduction

The three-level-output-stage matrix converter [28] is a multilevel matrix converter topology that applies the three-level neutral-point-clamped voltage source inverter concept to the inversion stage of an indirect matrix converter topology. Even though this topology was not verified through simulations and experiments in [28], associated modulation/control methods have been proposed [39 - 41] for controlling the three-level-output-stage matrix converter to generate a set of sinusoidal, balanced input and output waveforms. Having the ability to generate multilevel outputs, the three-level-output-stage matrix converter has a better output performance than the indirect matrix converter in terms of waveform harmonic content.

As discussed in Chapter 1, the output voltage quality of the three-level-output-stage matrix converter is used as a standard to assess the output performance of the indirect three-level sparse matrix converter considered in this work. Therefore, this chapter will analyse the performance of the three-level-output-stage matrix converter that is modulated using a space vector modulation that was proposed by the Author in [39]. To begin with, the operating principles of the three-level-output-stage matrix converter are presented. Then, a detailed explanation of the modulation strategy is given. Simulation results are shown to demonstrate the ability of the three-level-output-stage matrix converter to generate the desired input and output waveforms. Finally, output performance comparisons between the three-level-output-stage matrix converter and indirect matrix converter are made in order to show that the three-level-output-stage matrix converter is able to generate higher quality output waveforms than the indirect matrix converter.

5.2 Circuit Topology

As shown in Figure 5.1, the three-level-output-stage matrix converter consists of a rectification stage and an inversion stage. Similar to the indirect matrix converter, a three-phase to two-phase matrix converter is used as a rectifier to build up a switching DC-link voltage, V_{pn}, for the inversion stage. In order to apply the three-level neutral-point-clamped voltage source inverter (NPC VSI) to the inversion stage, the rectified DC-link voltage, V_{pn}, is transformed into dual voltage supplies, V_{po} and V_{no}, by connecting the DC-link middle point '*o*' to the neutral-point of the star-connected input filter capacitors. Using the DC-link middle point '*o*' as a reference, there are obviously three voltage levels at the DC-links: V_{po}, $0V$ and V_{no}. Based on these DC-link voltage levels, the inversion stage can be modulated to generate the multilevel output voltage waveforms.

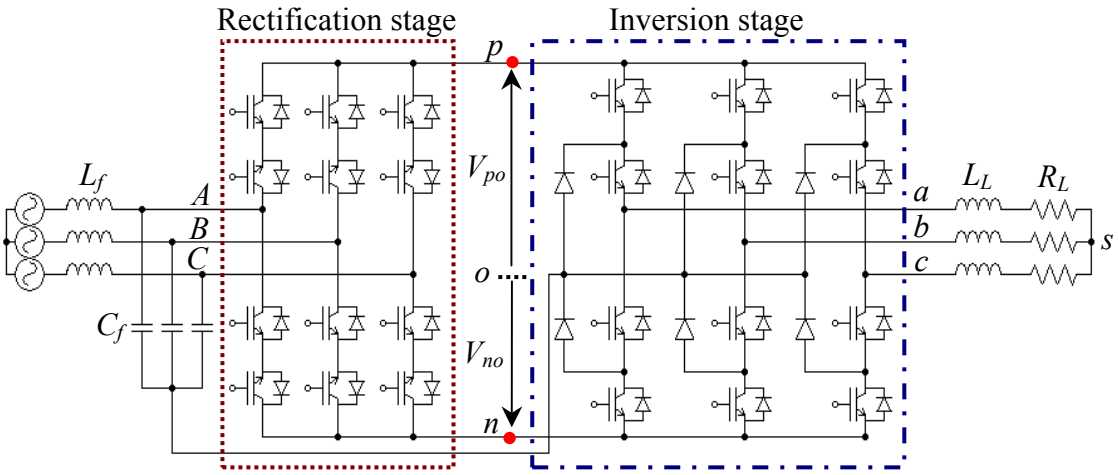


Figure 5.1: The schematic diagram of the three-level-output-stage matrix converter

As discussed in Section 2.3.2.1, at any instant, only two bi-directional switches in the rectification stage can be turned on to connect an input line-to-line voltage to the DC-links (*p* and *n*). Hence, the rectification stage can be represented with two conducting switches that connect the positive voltage level to the DC-link '*p*' terminal and negative voltage level to the '*n*' terminal, as shown in Figure 5.2. The circuit given in Figure 5.2 clearly resembles the conventional NPC VSI. As an example, if the rectification stage

connects the input line-to-line voltage V_{AB} to the DC-links, the DC-link voltage, V_{po}, is equal to the input line-to-neutral-point voltage V_{Ao} and $V_{no} = V_{Bo}$. By modulating the switching devices in each phase leg of the inversion stage according to the switching combinations in Table 5.1, each output terminal voltage (V_{xo}) of the inversion stage obviously has three possible voltage levels: V_{Ao}, 0V and V_{Bo}, which verify its ability to generate multilevel outputs.

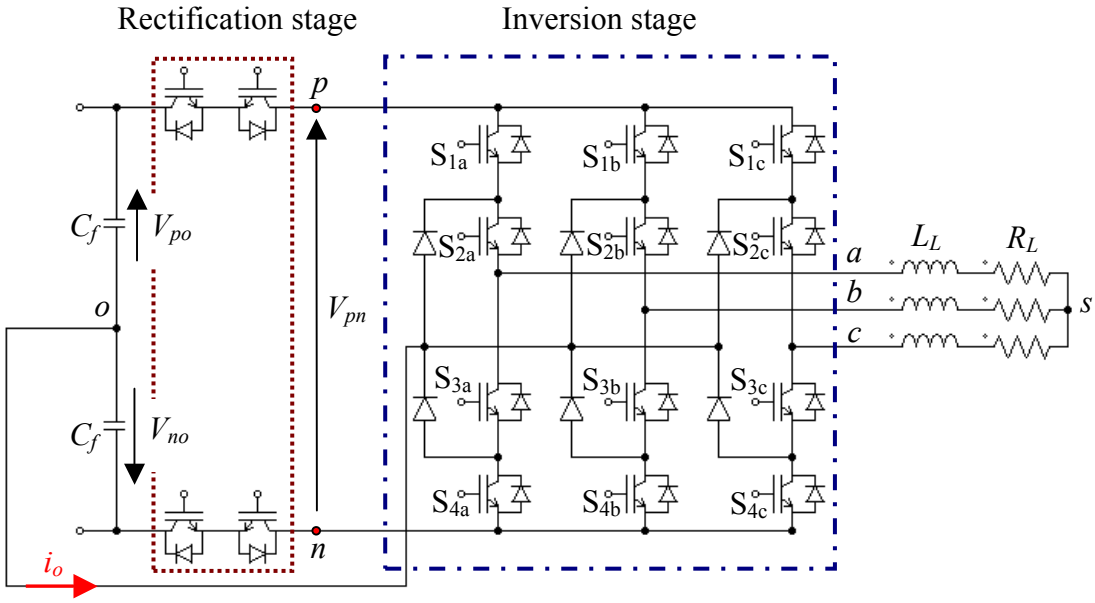


Figure 5.2: The equivalent state of the three-level-output-stage matrix converter with the rectification stage represented using two conducting switches.

S_{1x}	S_{2x}	S_{3x}	S_{4x}	V_{xo}	Switching state
ON	ON	OFF	OFF	V_{po}	P
OFF	ON	ON	OFF	0	O
OFF	OFF	ON	ON	V_{no}	N

Table 5.1: The switching combination for the switches in each phase leg of the inversion stage ($x \in \{a, b, c\}$)

Compared to the indirect matrix converter, the three-level-output-stage matrix converter is able to generate higher quality outputs due to its ability to construct the output waveforms with multiple voltage levels. In addition, it offers the same benefits as the indirect matrix converter: adjustable input displacement factor; high quality input waveforms; capability of regeneration and the lack of bulky and limited lifetime energy storage components.

However, complicated circuit configuration of the three-level-output-stage matrix converter is a drawback. The circuit consists of 24 switching devices and 30 diodes. It is possible to reduce the number of switching devices in the rectification stage to simplify the circuit, as reviewed in Section 2.5.3, but will not be elaborated in this chapter. Due to the high number of switching devices, a complex modulation strategy is required. In addition, the three-level-output-stage matrix converter inherits the neutral-point balancing problem from the NPC VSI. This problem could cause output voltage distortion if the neutral-point current, i_o, that flows to the input filter capacitors is not properly controlled.

To modulate the three-level-output-stage matrix converter to generate a set of balanced, sinusoidal input and output waveforms, associated modulation/control methods have been proposed in [39 – 41]. Proposed by the Author in [39], a space vector modulation (SVM) is derived based on the concept of the indirect SVM applied to an indirect matrix converter topology. Since the operating principles and space vector modulation for the three-phase to two-phase matrix converter (current source rectifier) and the NPC VSI have been explained in Section 2.3.2.1 and Chapter 3 respectively, this space vector modulation for the three-level-output-stage matrix converter can be easily explained in the following section.

5.3 Space Vector Modulation

Based on the strategy in [39], the rectification and inversion stages of the three-level-output-stage matrix converter are modulated using SVM. In each stage a combination of vectors is produced to synthesise a reference vector of given amplitude and angle. After determining the vectors and their duty cycles, the modulation pattern of the three-level-output-stage matrix converter then combines the switching states for both stages

uniformly so that a correct balance of the input currents and output voltages can be obtained for each switching period.

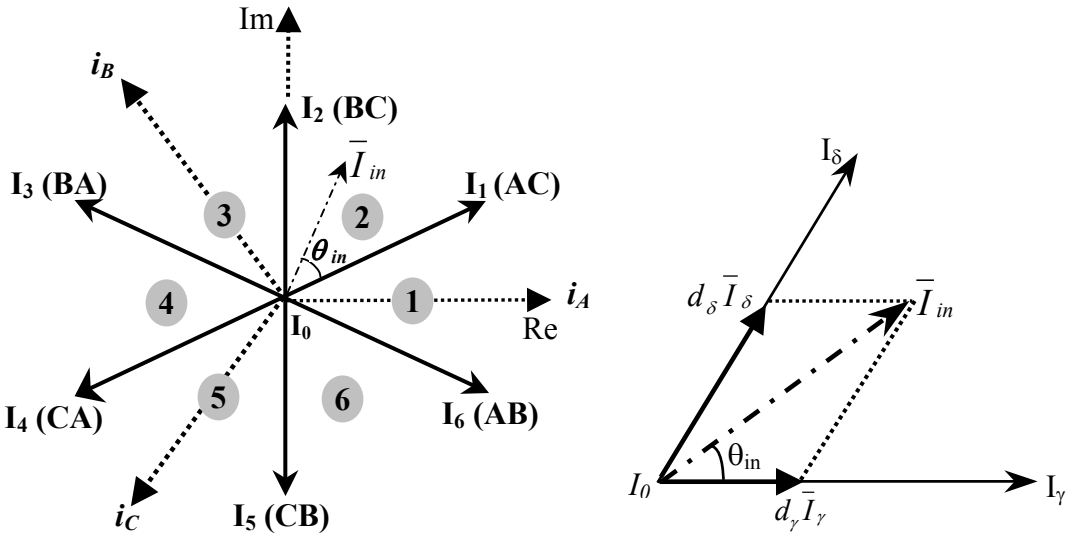
5.3.1 The Rectification Stage

Similar to the indirect matrix converter topology, the rectification stage of the three-level-output-stage matrix converter is modulated using SVM to maintain a set of sinusoidal, balanced input currents as well as generating a switching DC-link voltage, V_{pn}, for the inversion stage. As reviewed in Section 2.3.2.1, the input current vector, $\bar{I}_{in}$, is the reference vector for the rectification stage. To synthesize a reference vector, $\bar{I}_{in}$, that rotates in the space vector diagram, as shown in Figure 5.3(a), two adjacent current vectors (I_γ and I_δ) and a zero current vector (I_0) are selected based on the sector that the $\bar{I}_{in}$ is located at the sampling instant. As illustrated in Figure 5.3(b), the proportion between the duty cycles of I_γ and I_δ defines the direction and the duty cycle of I_0 determines the magnitude of the reference vector. The duty cycles for the vectors I_γ, I_δ and I_0 can be determined using (5.1), where m_R is the modulation index of the rectification stage and θ_{in} is the angle of the reference vector within the sector.

$$d_\gamma = m_R \cdot \sin\left(\frac{\pi}{3} - \theta_{in}\right) \qquad d_\delta = m_R \cdot \sin(\theta_{in}) \qquad d_0 = 1 - d_\gamma - d_\delta \tag{5.1}$$

For the three-level-output-stage matrix converter, the rectification stage is modulated to generate maximum DC-link voltage to inversion stage so that maximum overall voltage transfer ratio can be achieved. As a result, the modulation index, m_R, is set to unity (=1) and input displacement factor is controlled to zero (unity power factor). To simplify the overall modulation process, only the modulation on the inversion stage produces zero vectors. Hence, the zero current vector is eliminated and the rectification stage's switching sequence only consists of I_γ and I_δ. By determining the duty cycles d_γ and d_δ (5.1) with the modulation index m_R = 1, the rectification stage's duty cycles are then adjusted using (5.2) to occupy the whole switching period.

$$d_\gamma{}^R = \frac{d_\gamma}{d_\gamma + d_\delta} \qquad d_\delta{}^R = \frac{d_\delta}{d_\gamma + d_\delta} \tag{5.2}$$



(a) (b)

Figure 5.3: (a) The space vector diagram for the rectification stage (b) To synthesis a reference vector in a given sector

Due to the zero current vector cancellation, the average DC-link voltage over a switching period is no longer constant and needs to be determined using equation (5.3). With the maximum average DC-link voltage, V_{pn_avg}, supplied by the rectification stage, the modulation on the inversion stage controls the overall voltage transfer ratio of the converter.

$$V_{pn\_avg} = d_\gamma{}^R V_{l-l\gamma} + d_\delta{}^R V_{l-l\delta} \tag{5.3}$$

5.3.2 The Inversion Stage

As shown in Figure 5.1, the NPC VSI is used as the inversion stage of the three-level-output-stage matrix converter. The connection from the DC-link middle point '*o*' to the neutral-point of the star-connected input filter capacitors is essential to provide the required dual voltage supplies and a zero voltage middle point.

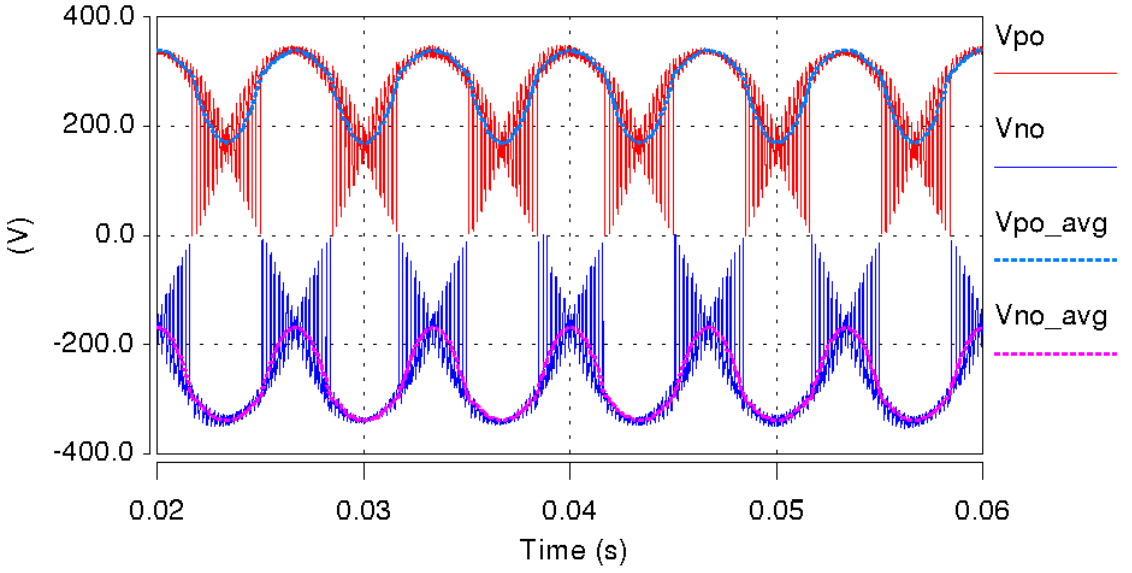
In order to operate the three-level-output-stage matrix converter to generate proper multilevel output voltages, the modulation on the inversion stage must ensure that the average neutral-point current over a switching period is maintained at zero. As shown in Table 5.1, each output terminal of the inversion stage can be connected to the DC-link point '*o*' for the zero voltage level (V_{xo} = 0V). Whenever the output terminal is connected to point '*o*', the neutral-point current, i_o, would cause uneven charging/discharging of the input filter capacitors, depending on the loading condition. Without proper control, the uneven changing voltage levels of the input filter capacitors would affect the DC-link voltages provided by the rectification stage, which would directly impact on the ability of the inversion stage to generate proper multilevel outputs, causing output voltage distortion. This situation is similar to the neutral-point balancing problem for a stand-alone NPC VSI.

The modulation on the inversion stage must be able to apply the unequal DC-link voltages, V_{po} and V_{no}, to generate the desired outputs. As shown in Figure 5.4(a), V_{po} and V_{no} provided by the rectification stage are obviously not equal. Referring to their spectra, shown in Figure 5.4(b), these DC-link voltages consist of a DC component and a third order harmonic of the input frequency that is inherently included in the rectification stage's output when it is modulated using SVM. For each switching period, the inversion stage is modulated based on the averages of the DC-link voltages, V_{po} and $V_{no.}$ Identifying that the third order harmonics for the DC-link voltages are 180^0 out of phase, as shown in Figure 5.14(a), the averages of V_{po} and V_{no} can be approximated as below:

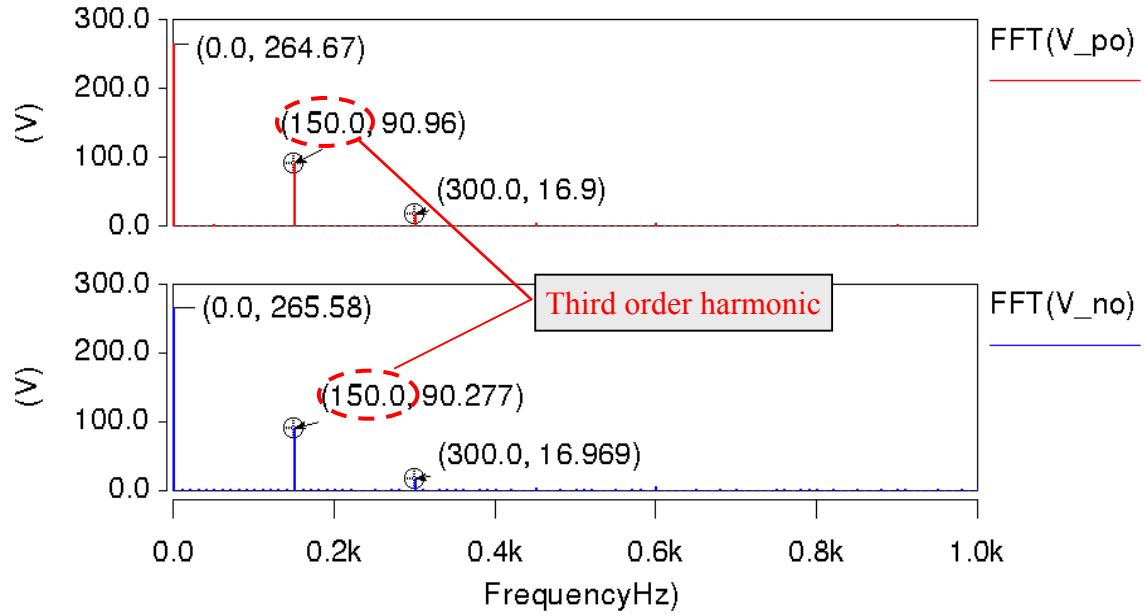
$$V_{po\_avg} \approx \left(V_{pn\_avg} \Big/ 2 \right) + \left(\frac{V_{pn\_avg}}{6} \right) \cdot \cos(3 \cdot \omega_i \cdot t)$$

$$V_{no\_avg} \approx -\left(V_{pn\_avg} \Big/ 2 \right) + \left(\frac{V_{pn\_avg}}{6} \right) \cdot \cos(3 \cdot \omega_i \cdot t) \qquad (5.4)$$

where ω_i is equal to $2\pi f_i$ with f_i = the frequency of the supply voltages. The waveforms 'V_{po_avg}' and 'V_{no_avg}', shown in Figure 5.4(a), clearly resemble the low frequency DC-link voltages, V_{po} and V_{no}.



(a) The voltage waveforms



(b) The spectra

Figure 5.4. The DC-link voltages, V_{po} and V_{no}, provided by the rectification stage with supply frequency, f_i = 50Hz

Since SVM is applied to the inversion stage, the effects of the unequal DC-link voltages on the voltage space vectors must be examined. For this reason, the output voltages generated by the switching states of the inversion stage have to be determined. Like the NPC VSI, the inversion stage of the three-level-output-stage matrix converter can achieve twenty-seven switching states that represent the connections of the output terminals (*a*, *b* and *c*) to their respective DC-link points (*p*, *n* or *o*), as shown in Table 3.2. To facilitate explanation, only the switching states listed in Table 5.2 are analysed. The output phase voltages generated by each switching state are determined using equation (5.5), which is derived based on (3.2) but expressed in terms of V_{po_avg} and V_{on_avg} (= $-V_{no\_avg}$). m_{x1} and m_{x2} represent the switch combinations (S_{1x} & S_{2x}) and (S_{3x} & S_{4x}), which is one when both switches in the combination are 'on' or zero otherwise. Referring to Table 5.2, it is obvious that the output phase voltages generated by each switching state depends on the connected DC-link voltage(s). For example, switching state *POO* applies only the DC-link voltage, V_{po_avg}, to the output. Hence, the output phase voltages generated by *POO* is apparently different to *ONN*, which uses only V_{on_avg}. However, when $V_{po\_avg} = V_{on\_avg}$, the output phase voltages generated by *POO* and *ONN* would be identical, as shown in Table 3.1.

$$V_{as} = \left(\tfrac{1}{3}\right)\left[V_{po\_avg}\left(2 \cdot m_{a1} - m_{b1} - m_{c1}\right) - V_{on\_avg}\left(2 \cdot m_{a3} - m_{b3} - m_{c3}\right)\right]$$

$$V_{bs} = \left(\tfrac{1}{3}\right)\left[V_{po\_avg}\left(2 \cdot m_{b1} - m_{a1} - m_{c1}\right) - V_{on\_avg}\left(2 \cdot m_{b3} - m_{a3} - m_{c3}\right)\right]$$

$$V_{cs} = \left(\tfrac{1}{3}\right)\left[V_{po\_avg}\left(2 \cdot m_{c1} - m_{a1} - m_{b1}\right) - V_{on\_avg}\left(2 \cdot m_{c3} - m_{a3} - m_{b3}\right)\right] \qquad (5.5)$$

Using space vector transformation (3.4), these switching states can be converted into voltage space vectors, shown in Table 5.2. As an example, the voltage space vectors for the case where $V_{po\_avg} > V_{on\_avg}$ are shown in Figure 5.5. Compared to the diagram given in Figure 3.3, the small voltage vectors (SVV) and medium voltage vectors (MVV) are obviously affected by the unequal DC-link voltages while the large voltage vectors (V_2 and V_5) remain unchanged because $V_{po\_avg} + V_{on\_avg}$ is equal to V_{pn_avg}. At any instant, except when $V_{po\_avg} = V_{on\_avg}$, each redundant switching state of a SVV (e.g. V_1) generates a different magnitude of voltage vector (V_{1A} and V_{1B}) due to the use of the

			Output phase voltages			Output voltage space vectors		
a	*b*	*c*	V_{as}	V_{bs}	V_{cs}	$\overline{V}$	Magnitude	Angle
P	P	P	0	0	0	V_0	0	0
O	O	O	0	0	0			
N	N	N	0	0	0			
P	O	O	$\frac{2}{3}\cdot V_{po\_avg}$	$-\frac{1}{3}\cdot V_{po\_avg}$	$-\frac{1}{3}\cdot V_{po\_avg}$	V_{1A}	$\frac{2}{3}\cdot V_{po\_avg}$	0
O	N	N	$\frac{2}{3}\cdot V_{on\_avg}$	$-\frac{1}{3}\cdot V_{on\_avg}$	$-\frac{1}{3}\cdot V_{on\_avg}$	V_{1B}	$\frac{2}{3}\cdot V_{on\_avg}$	0
P	N	N	$\frac{2}{3}(V_{po\_avg}+V_{on\_avg})$	$-\frac{1}{3}(V_{po\_avg}+V_{on\_avg})$	$-\frac{1}{3}(V_{po\_avg}+V_{on\_avg})$	V_2	$\frac{2}{3}\cdot(V_{po\_avg}+V_{on\_avg})$	0
P	O	N	$\frac{1}{3}(2V_{po\_avg}+V_{on\_avg})$	0	$-\frac{1}{3}(V_{po\_avg}+2V_{on\_avg})$	V_3	$\frac{2}{3}(V_{po\_avg}^2+V_{po\_avg}V_{on\_avg}+V_{on\_avg}^2)^{1/2}$	$\tan^{-1}\left(\frac{\sqrt{3}\cdot V_{on\_avg}}{2V_{po\_avg}+V_{on\_avg}}\right)$
P	P	O	$\frac{1}{3}\cdot V_{po\_avg}$	$\frac{1}{3}\cdot V_{po\_avg}$	$-\frac{2}{3}\cdot V_{po\_avg}$	V_{4A}	$\frac{2}{3}\cdot V_{po\_avg}$	$\pi/3$
O	O	N	$\frac{1}{3}\cdot V_{on\_avg}$	$\frac{1}{3}\cdot V_{on\_avg}$	$-\frac{2}{3}\cdot V_{on\_avg}$	V_{4B}	$\frac{2}{3}\cdot V_{on\_avg}$	$\pi/3$
P	P	N	$\frac{1}{3}(V_{po\_avg}+V_{on\_avg})$	$\frac{1}{3}(V_{po\_avg}+V_{on\_avg})$	$-\frac{2}{3}(V_{po\_avg}+V_{on\_avg})$	V_5	$\frac{2}{3}\cdot(V_{po\_avg}+V_{on\_avg})$	$\pi/3$

Table 5.2: The output phase voltages and voltage space vectors generated by the switching states of the inversion stage.

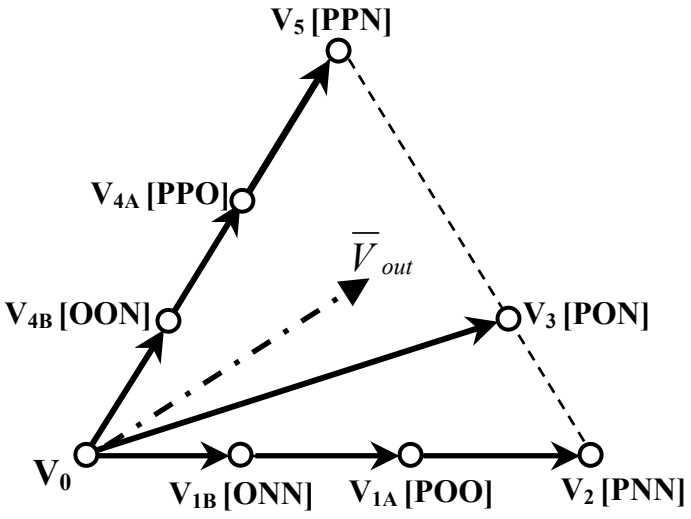


Figure 5.5: The voltage vectors generated by the unequal DC-link voltages when the $V_{po\_avg} > V_{on\_avg}$

different DC-link voltages. On the other hand, the MVV (e.g. V_3) not only has varying magnitude but also varying angle ($19^o < \theta_{V3} < 41^o$), depending on V_{po_avg} and V_{on_avg}. As shown in Figure 5.5, these voltage space vectors with varying magnitude and angle (only for MVV) complicate the process of synthesizing the reference vector, $\overline{V}_{out}$, for the inversion stage.

To effectively modulate the inversion stage using SVM to generate the desired outputs, the nearest three virtual space vector modulation (NTV SVM) is a good option. The ability of NTV SVM to control the neutral-point balancing problem has been proven in Chapter 3. Therefore, by applying NTV SVM to the inversion stage, the average neutral-point current over each switching period can be maintained at zero, keeping the voltage levels of the input filter capacitors from changing unevenly. The concept of defining virtual vectors, by linearly combining the voltage space vectors, in NTV SVM is able to overcome the modulation complication caused by the uneven DC-link voltages. By linearly combining the varying voltage vectors (SVV and MVV) to form a set of virtual vectors with constant magnitude and fixed direction, as shown in Figure 5.6, the process of synthesizing the reference vector, $\overline{V}_{out}$, can be greatly simplified.

As shown in Figure 5.6, the virtual medium vectors (V_{MV}) and virtual small vectors (V_{SV}) are formed by linear combinations of varying voltage vectors, SVV and MVV. To take into account the effects of the unequal DC-link voltages on the SVV and MVV, C_1 to C_7 are introduced to control the active time of these voltage vectors within the combinations. At any sampling instant, C_1 to C_7 are varied according to the SVV and MVV in order to maintain the magnitudes and angles of V_{MV} and V_{SV}, shown in Figure 5.6, that are obtained using even DC-link voltages ($V_{po\_avg} = V_{on\_avg} = V_{pn\_avg}/2$). The equations of determining C_1 to C_7 are presented in (5.6) and (5.7), where the varying magnitudes and angles of SVV and MVV are evidently taken into consideration in the calculations.

$$C_1 = C_3 = \left(\frac{V_{on\_avg} - \left[V_{pn\_avg} \middle/ 2 \right]}{V_{on\_avg} - V_{po\_avg}} \right), \qquad C_2 = C_4 = \left(\frac{\left[V_{pn\_avg} \middle/ 2 \right] - V_{po\_avg}}{V_{on\_avg} - V_{po\_avg}} \right) \tag{5.6}$$

$$C_6 = h \cdot g, \qquad C_7 = \frac{1}{e}\left(\frac{V_{pn\_avg}}{3} - a - f \cdot h \cdot g\right), \qquad C_5 = 1 - C_6 - C_7 \tag{5.7}$$

where

$$a = \begin{cases} \left[2V_{on\_avg}/3\right] - \sec 1,3,5 \\ \left[2V_{po\_avg}/3\right] - \sec 2,4,6 \end{cases}, b = \begin{cases} \left[2V_{po\_avg}/3\right] - \sec 1,3,5 \\ \left[2V_{on\_avg}/3\right] - \sec 2,4,6 \end{cases},$$

$$c = \frac{2\left(V_{po\_avg}{}^2 + V_{po\_avg}V_{on\_avg} + V_{on\_avg}{}^2\right)^{1/2}}{3}\cos\theta_M,$$

$$d = \frac{2\left(V_{po\_avg}{}^2 + V_{po\_avg}V_{on\_avg} + V_{on\_avg}{}^2\right)^{1/2}}{3}\sin\theta_M,$$

$$e = \frac{b}{2} - a, \qquad f = c - a, \qquad g = \left(d \cdot e - \frac{\sqrt{3}}{2} f \cdot b\right)^{-1},$$

$$h = \frac{V_{pn\_avg}}{\sqrt{3}}\left(\frac{e}{3} - \frac{b}{2}\right) + \frac{\sqrt{3}}{2} b \cdot a,$$

θ_M is the angle of medium voltage vector within the sector (e.g. For sector 1, θ_M $= \theta_{V3} = \tan^{-1}\left(\frac{\sqrt{3} \cdot V_{on\_avg}}{2V_{po\_avg} + V_{on\_avg}}\right)$)

- $|\mathbf{V_{SV}}| = V_{pn\_avg}/3$
- $|\mathbf{V_{MV}}| = \frac{2V_{pn\_avg}}{3\sqrt{3}}$
- $|\mathbf{V_{LV}}| = 2V_{pn\_avg}/3$
- $\theta_{VSV1}, \theta_{VLV1} = 0$
- $\theta_{VSV2}, \theta_{VLV2} = \pi/3$
- $\theta_{VMV2} = \pi/6$

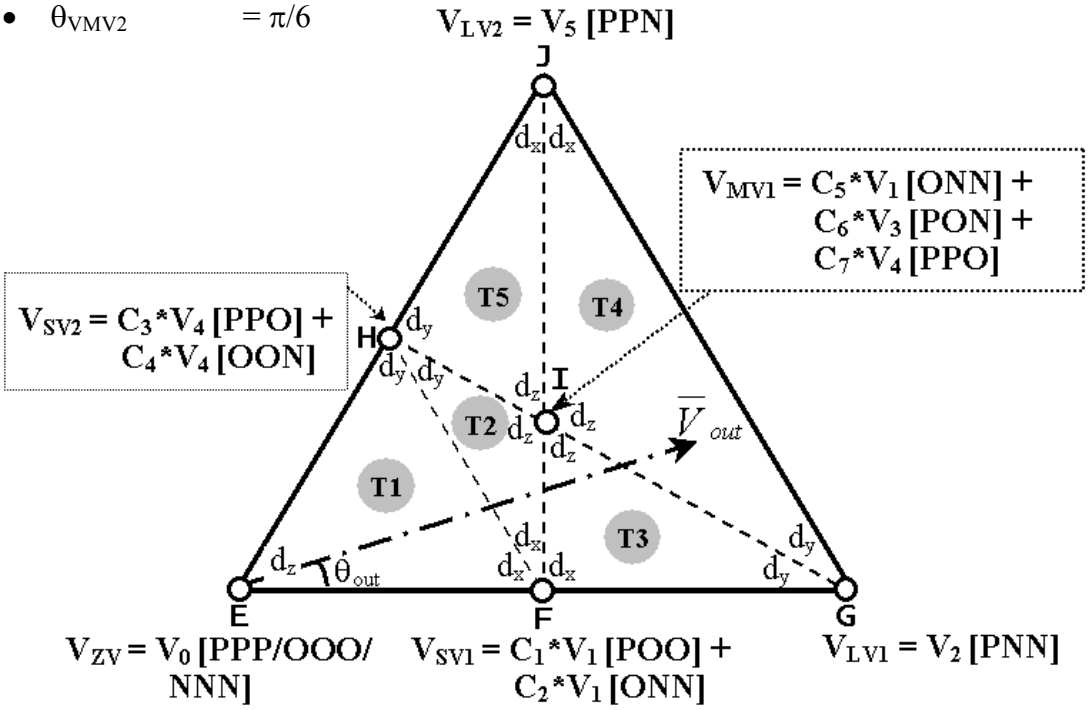


Figure 5.6: Sector 1 of the space vector diagram for the inversion stage that is modulated using the nearest three virtual space vector modulation.

To determine how C_1 to C_4 vary due to the unequal DC-link voltages, equation (5.4) is substituted into (5.7), where V_{on_avg} = - V_{no_avg}. Due to the 180° output of phase for the third order harmonics of the DC-link voltages, $C_1 = C_2 = C_3 = C_4 = ½$, as proven below:

$$C_1 = C_3 = \left(\frac{\frac{V_{pn\_avg}}{2} - \frac{V_{pn\_avg}}{6}\cos(\theta) - \left[V_{pn\_avg} \Big/ 2 \right]}{\frac{V_{pn\_avg}}{2} - \frac{V_{pn\_avg}}{6}\cos\theta - \frac{V_{pn\_avg}}{2} - \frac{V_{pm\_avg}}{6}\cos\theta} \right) = \frac{-\frac{V_{pn\_avg}}{6}\cos\theta}{-\frac{2V_{pn\_avg}}{6}\cos\theta} = \frac{1}{2}$$

This result shows that V_{SV} are formed by equal linear combinations of SVVs, although the unequal DC-link voltages affect the magnitudes of the SVVs. This is because, when forming V_{SV}, the effect of V_{po_avg} on one voltage vector is balanced by the effect of V_{on_avg} on another. For example, when $V_{po\_avg} > V_{on\_avg}$, the magnitude of *POO* is increased while, due to the 180° output of phase of V_{on_avg}, the magnitude of *ONN* is decreased equally. To achieve the correct magnitude of V_{SV1} it is formed by an equal linear combination of *POO* and *ONN* ($C_1 = C_2 = ½$). Using (5.7), the variables C_5, C_6 and C_7 are equal to 1/3, regardless of the magnitudes of V_{po_avg} and V_{on_avg}. This shows that the V_{MV} are also formed by equal linear combinations of varying voltage vectors.

With $C_1 = C_2 = C_3 = C_4 = ½$ and $C_5 = C_6 = C_7 = 1/3$, the V_{SV} and V_{MV} for the inversion stage are formed by equitable combinations of voltage vectors that are presented in Tables 3.6 and 3.7, respectively. Therefore, the space vector diagram for the inversion stage, as shown in Figure 5.7, is identical to the diagram given in Figure 3.6. For each switching period, to synthesize a reference output voltage vector ($\overline{V}_{out}$), three nearest virtual vectors are selected based on the triangle in which the reference vector is located at the sampling instant. Referring to Figure 5.6, there are obviously five triangles (*T1 – T5*) within a sector. The duty cycle equations for the selected virtual vectors in each triangle are shown in Table 5.3, where the modulation index of the inversion stage, m_I, is equal to (5.8) and θ_{out} is the angle of the reference vector, $\overline{V}_{out}$, within the sector. To complete the modulation process of the inversion stage, the voltage vectors that form the selected virtual vectors are applied to the output according to the switching sequences shown in Table 5.4.

$$m_I = \frac{\sqrt{3} * V_{om}}{V_{pn\_avg}} \tag{5.8}$$

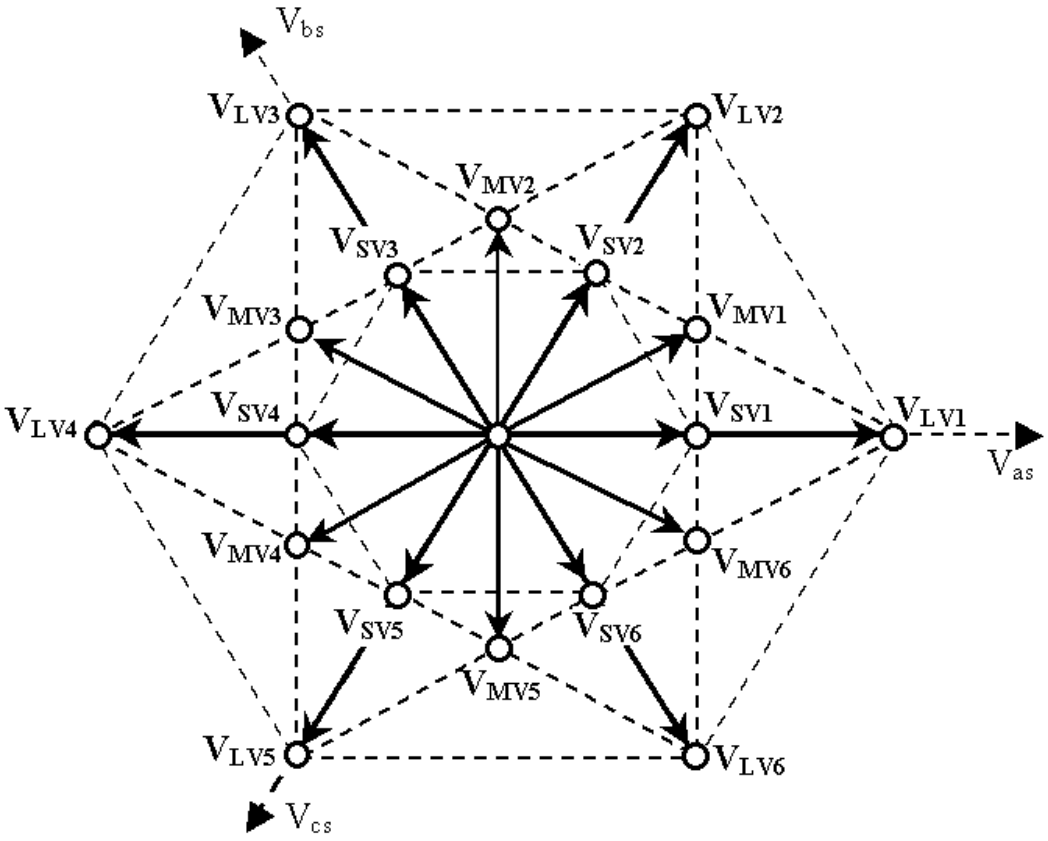


Figure 5.7: The space vector diagram for the inversion stage that is modulated using NTV SVM.

Triangle	d_x	d_y	d_z
T1 [ΔEFH]	$m_I\left(\sqrt{3}\cos\theta_{out}-\sin\theta_{out}\right)$	$2m_I\sin\theta_{out}$	$1-m_I\left(\sqrt{3}\cos\theta_{out}+\sin\theta_{out}\right)$
T2 [ΔFIH]	$2-m_I\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)$	$2-2\sqrt{3}m_I\cos\theta_{out}$	$3m_I\left(\sqrt{3}\cos\theta_{out}+\sin\theta_{out}\right)-3$
T3 [ΔFGI]	$2-m_I\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)$	$\sqrt{3}m_I\cos\theta_{out}-1$	$3m_I\sin\theta_{out}$
T4 [ΔGJI]	$0.5m_I\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)-1$	$2-2\sqrt{3}m_I\cos\theta_{out}$	$m_I\left(\sqrt{3}\cos\theta_{out}-\sin\theta_{out}\right)$
T5 [ΔHIJ]	$0.5m_I\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)-1$	$\sqrt{3}m_I\cos\theta_{out}-1$	$3-1.5m_I\left(\sqrt{3}\cos\theta_{out}+\sin\theta_{out}\right)$

Table 5.3: The duty cycle equations for the selected virtual vectors in each triangle.

Triangle	Sector	t_1			t_2			t_3			t_4			t_5			t_6			t_7		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T1	1	P	P	P	P	P	O	P	O	O	O	O	O	O	O	N	O	N	N	N	N	N
	2	P	P	P	P	P	O	O	P	O	O	O	O	O	O	N	N	O	N	N	N	N
	3	P	P	P	O	P	P	O	P	O	O	O	O	N	O	O	N	O	N	N	N	N
	4	P	P	P	O	P	P	O	O	P	O	O	O	N	O	O	N	N	O	N	N	N
	5	P	P	P	P	O	P	O	O	P	O	O	O	O	N	O	N	N	O	N	N	N
	6	P	P	P	P	O	P	P	O	O	O	O	O	O	N	O	O	N	N	N	N	N

Triangle	Sector	t_1			t_2			t_3			t_4			t_5		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T2	1	P	P	O	P	O	O	P	O	N	O	O	N	O	N	N
	2	P	P	O	O	P	O	O	P	N	O	O	N	N	O	N
	3	O	P	P	O	P	O	N	P	O	N	O	O	N	O	N
	4	O	P	P	O	O	P	N	O	P	N	O	O	N	N	O
	5	P	O	P	O	O	P	O	N	P	O	N	O	N	N	O
	6	P	O	P	P	O	O	P	N	O	O	N	O	O	N	N
T3	1	P	P	O	P	O	O	P	O	N	P	N	N	O	N	N
	2	P	P	O	P	P	N	O	P	N	O	O	N	N	O	N
	3	O	P	P	O	P	O	N	P	O	N	P	N	N	O	N
	4	O	P	P	N	P	P	N	O	P	N	O	O	N	N	O
	5	P	O	P	O	O	P	O	N	P	N	N	P	N	N	O
	6	P	O	P	P	N	P	P	N	O	O	N	O	O	N	N
T4	1	P	P	O	P	P	N	P	O	N	P	N	N	O	N	N
	2	P	P	O	P	P	N	O	P	N	N	P	N	N	O	N
	3	O	P	P	N	P	P	N	P	O	N	P	N	N	O	N
	4	O	P	P	N	P	P	N	O	P	N	N	P	N	N	O
	5	P	O	P	P	N	P	O	N	P	N	N	P	N	N	O
	6	P	O	P	P	N	P	P	N	O	P	N	N	O	N	N
T5	1	P	P	O	P	P	N	P	O	N	O	O	N	O	N	N
	2	P	P	O	O	P	O	O	P	N	N	P	N	N	O	N
	3	O	P	P	N	P	P	N	P	O	N	O	O	N	O	N
	4	O	P	P	O	O	P	N	O	P	N	N	P	N	N	O
	5	P	O	P	P	N	P	O	N	P	O	N	O	N	N	O
	6	P	O	P	P	O	O	P	N	O	P	N	N	O	N	N

Table 5.4: The switching sequences for the inversion stage of the three-level-output-stage matrix converter that is modulated using NTV SVM.

5.3.3 Synchronization between the rectification and inversion stages

In order to maintain the balance of input currents and output voltages within a switching period, the modulation pattern for the three-level-output-stage matrix converter has to combine the switching states of the rectification stage (I_γ and I_δ) and the inversion stage (V_x, V_y and V_z) uniformly. Let us consider an example where the vector $\overline{I}_{in}$ is located in sector 2 while $\overline{V}_{out}$ is located in *T4* of sector 1. For the rectification stage, the selected current vectors are: I_1 (= I_γ) and I_2 (= I_δ); the virtual vectors selected for the inversion stage are: V_{MV1} (= V_z), V_{LV1} (= V_y) and V_{LV2} (= V_x). Based on NTV SVM, these virtual vectors are formed using the voltage vectors: V1 (ONN), V2 (PNN), V3 (PON), V4 (PPO) and V5 (PPN). These voltage vectors are applied to the output according to the switching sequence highlighted in Table 5.4.

To ensure the minimum number of switching transitions, the selected voltage vectors for the inversion stage are arranged in a double-sided switching sequence but with unequal halves because each half should be applied to the rectification stage's switching sequence: $I_1 - I_2$. Based on this example, the modulation pattern for the three-level-output-stage matrix converter is shown in Figure 5.8. The time interval for each voltage vector of the inversion stage's switching sequence can be determined using equations (5.9) – (5.19).

$$t_{r1} = d_\gamma^R * T_{SW} \tag{5.9}$$

$$t_{i1} = \frac{1}{3} * d_\gamma^R * d_z * T_{SW} \tag{5.10}$$

$$t_{i2} = d_\gamma^R * d_x * T_{SW} \tag{5.11}$$

$$t_{i3} = \frac{1}{3} * d_\gamma^R * d_z * T_{SW} \tag{5.12}$$

$$t_{i4} = d_\gamma^R * d_y * T_{SW} \tag{5.13}$$

$$t_{i5} = \frac{1}{3} * d_\gamma^R * d_z * T_{SW} \tag{5.14}$$

$$t_{i6} = \frac{1}{3} * d_\delta^R * d_z * T_{SW} \tag{5.15}$$

$$t_{i7} = d_\delta^R * d_y * T_{SW} \tag{5.16}$$

$$t_{i8} = \frac{1}{3} * d_{\delta}^{R} * d_{z} * T_{SW} \tag{5.17}$$

$$t_{i9} = d_{\delta}^{R} * d_{x} * T_{SW} \tag{5.18}$$

$$t_{i10} = \frac{1}{3} * d_{\delta}^{R} * d_{z} * T_{SW} \tag{5.19}$$

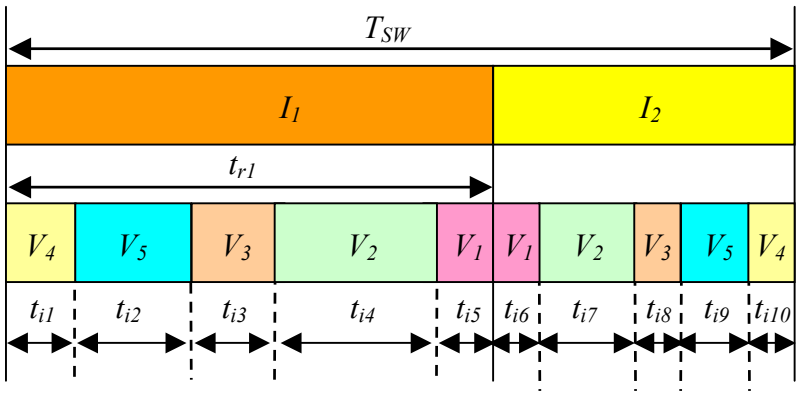


Figure 5.8: The modulation pattern of the three-level-output-stage matrix converter for the case where the reference vector, $\overline{I}_{in}$, is located in sector 2 while $\overline{V}_{out}$ is located in triangle *T4* of sector 1.

5.4 Simulation results

The three-level-output-stage matrix converter shown in Figure 5.1 has been simulated using SABER, based on the specifications presented in Appendix A. To comprehensively analyze the performance of this topology, the three-level-output-stage matrix converter has been operated at a high modulation index (V_{out_peak} = 270V) and a low modulation index (V_{out_peak} = 135V).

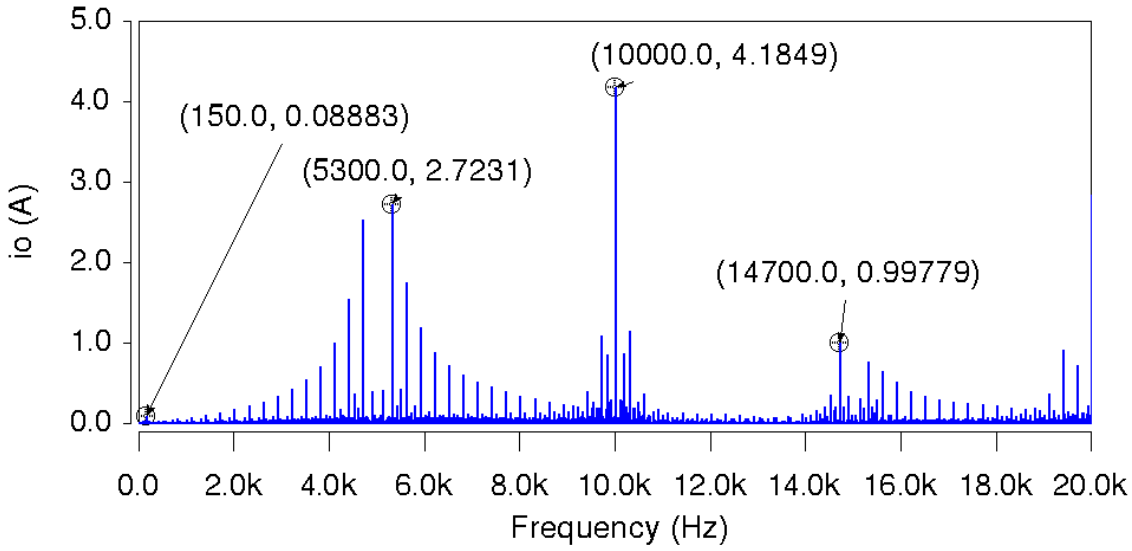
The effectiveness of the modulation strategy in maintaining the voltage levels of the input filter capacitors is evaluated first. As discussed earlier, the connection from the DC-link middle point '*o*' to the neutral-point of the star-connected input filter capacitors is essential but the neutral-point current, i_o, can cause the uneven changing voltage levels of the input filter capacitors. In order to maintain the correct voltage levels of the

input filter capacitors, the average neutral-point current over a switching period must be maintained at zero.

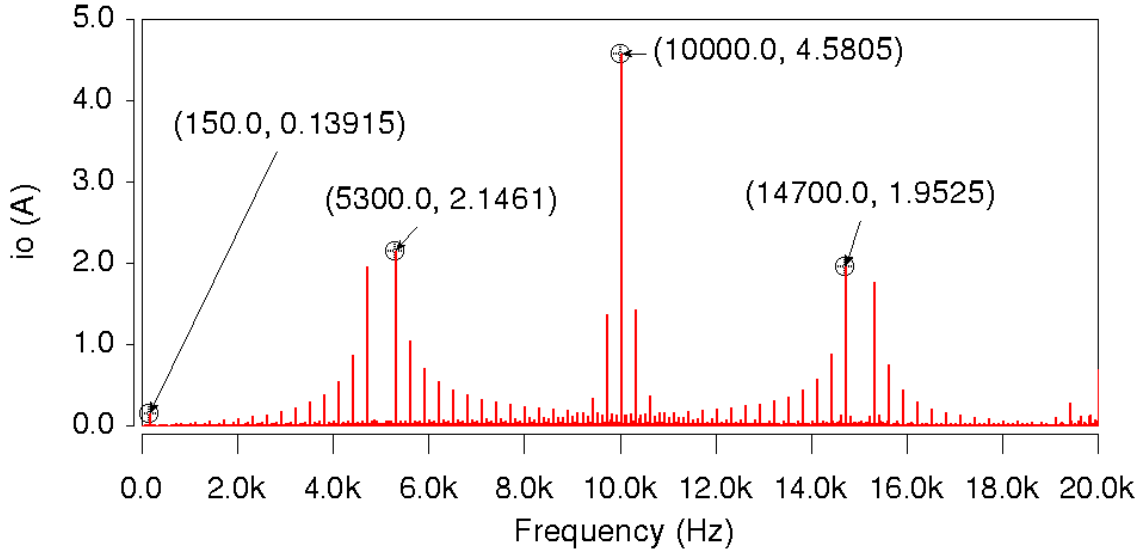
The spectra of i_o at high and low modulation index are shown in Figure 5.9. Both spectra clearly show that there is no significant harmonic around the input and output fundamental frequencies except the third order harmonic of the supply frequency (150Hz). The third order harmonic current is $0.09A_{pk}$ at high modulation index and $0.14A_{pk}$ at low modulation index. The slightly higher harmonic at low modulation index is due to the frequent use of small voltage vectors that can generate neutral point current. Due to the presence of this harmonic current, there is a fluctuation in the neutral-point potential, as shown in Figure 5.10. However, the fluctuations at both modulation indexes are comparatively small ($\pm$5V ≅ 1% of the supply voltages) so the voltage levels of the input filter capacitors remains balanced, as shown in Figure 5.11. These results clearly show that the modulation strategy is able to compensate for the neutral-point current and maintain the voltage levels of the input filter capacitors.

Besides the supply voltages, it is also crucial to analyse whether i_o affects the input current waveforms, especially at low modulation indexes. The input current waveforms and the spectra of the input current, i_A, are shown in Figures 5.12 and 5.13, respectively. As shown in Figure 5.12, the input currents are sinusoidal and balanced. Then, referring to their spectra presented in Figure 5.13, there are clearly some harmonics around fundamental frequency but the ripples are not significant (< 1% at both modulation indexes), which prove that the modulation strategy is able to modulate the three-level-output-stage matrix converter to generate a set of sinusoidal, balanced input currents despite the presence of neutral-point current.

Figure 5.14 presents the DC-link voltages provided by the rectification stage with the overall voltage transfer ratio of the three-level-output-stage matrix converter stepped from 0.4 to 0.8. As shown in Figure 5.14(a), maximum DC-link voltage, V_{pn}, is always provided by the rectification stage, despite the voltage transfer ratio is changed, so that the three-level-output-stage matrix converter can achieve maximum overall voltage transfer ratio. By transforming V_{pn} into dual voltage supplies, the inversion stage is supplied with V_{po} and V_{no}, which are clearly unequal, as shown in Figure 5.14(b).

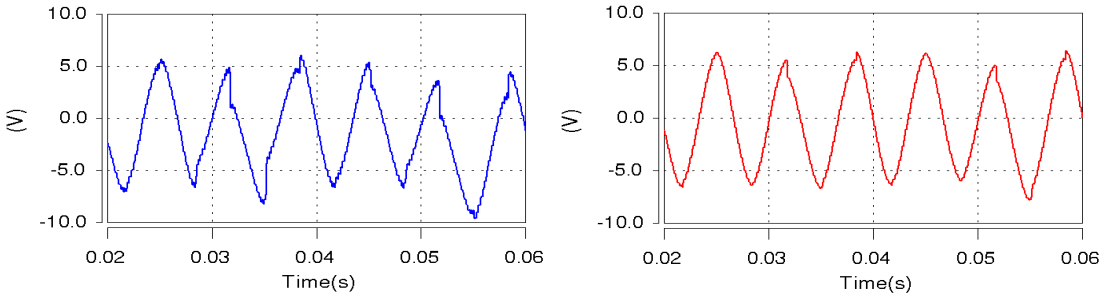


(a) High modulation index



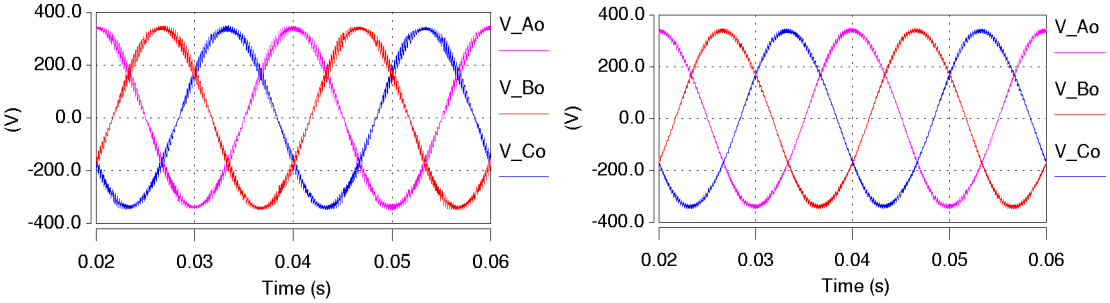
(b) Low modulation index

Figure 5.9: The spectra of the neutral-point current, i_o



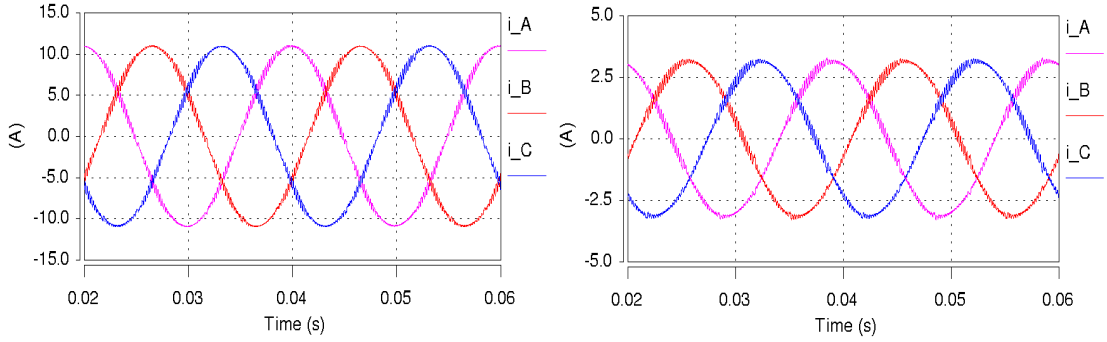
(a) High Modulation index (b) Low modulation index

Figure 5.10: The fluctuation of the neutral-point potential



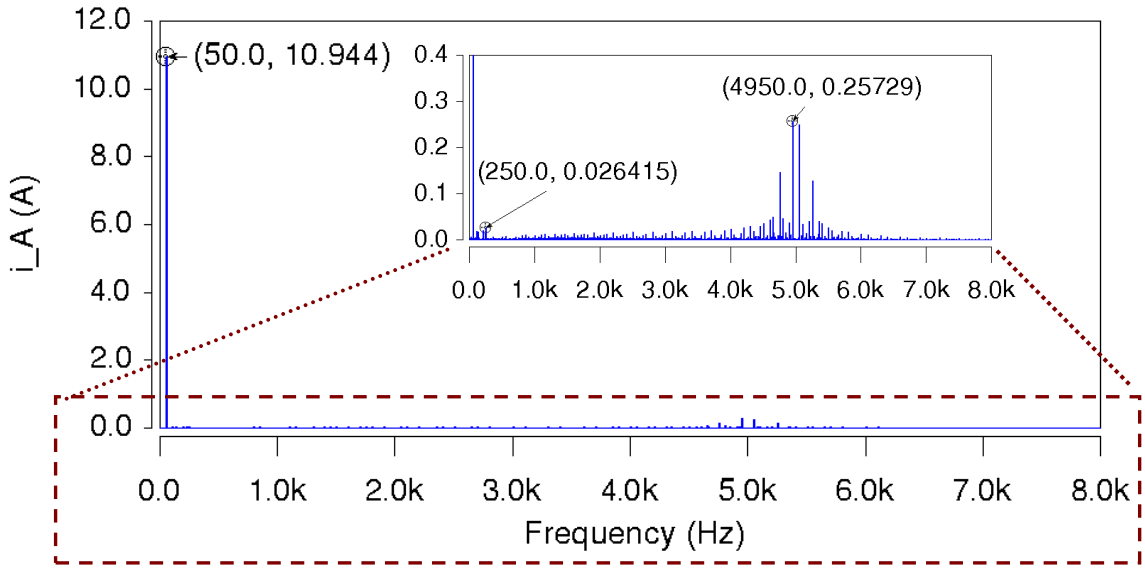
(a) High Modulation index (b) Low modulation index

Figure 5.11: The voltage levels of the input filter capacitors

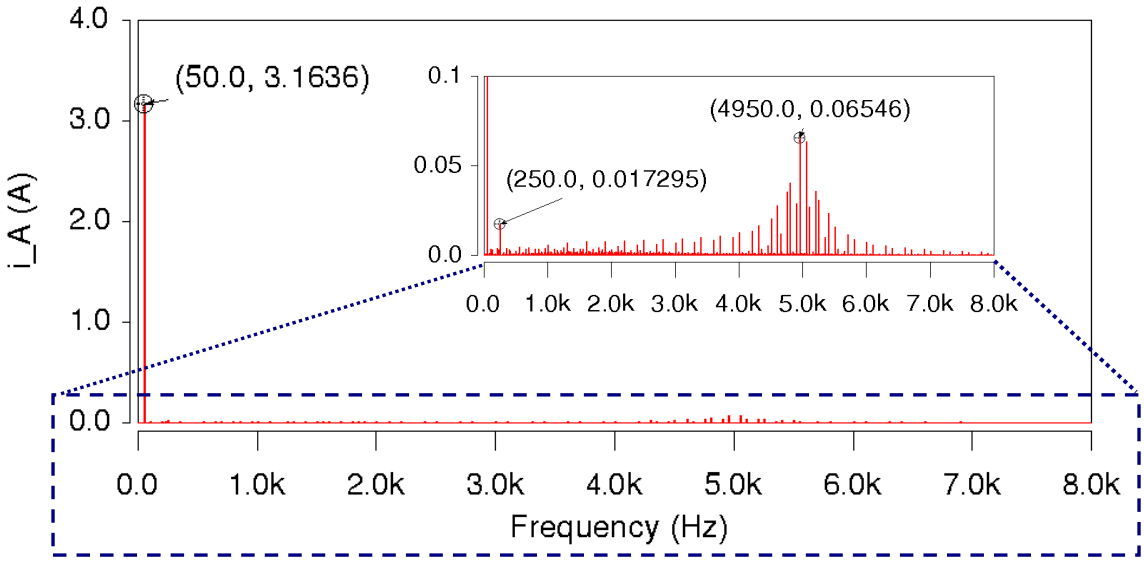


(a) High modulation index (b) Low modulation index

Figure 5.12: The input current waveforms



(a) High modulation index



(b) Low modulation index

Figure 5.13: The spectra of the input current i_A

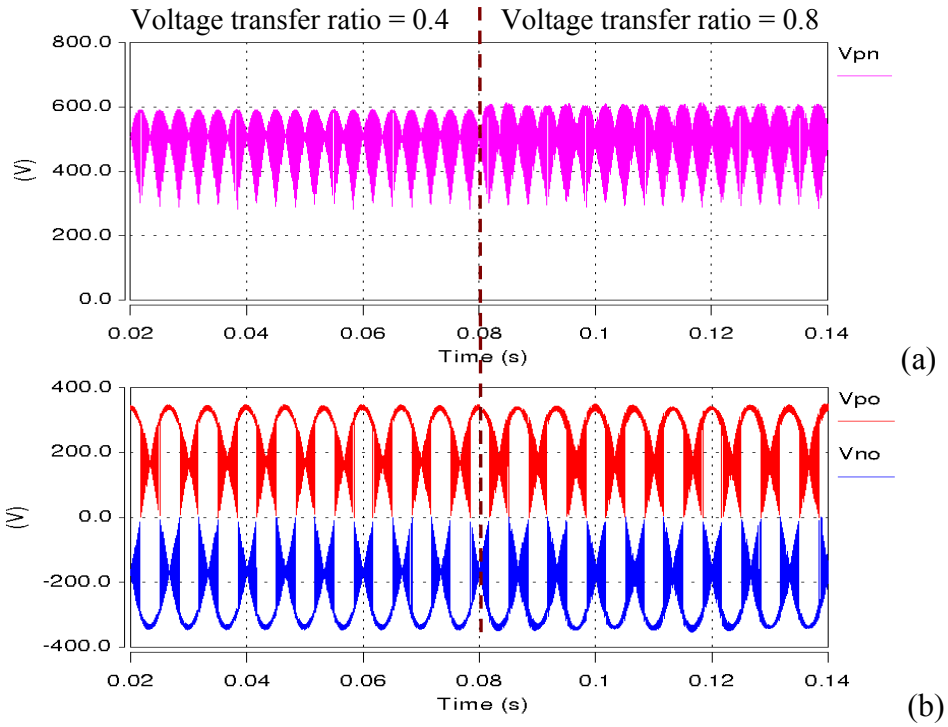


Figure 5.14: The DC-link voltages provided by the rectification stage (a) V_{pn} (b) V_{po} and V_{no}

To show that the three-level-output-stage matrix converter is capable of generating multilevel outputs, Figure 5.15 presents the output waveforms generated by this topology with the voltage transfer ratio stepped from 0.4 to 0.8. The output terminal voltage, shown in Figure 5.15(a), clearly illustrates how the three-level-output-stage matrix converter is modulated to apply the voltage levels to the output terminal '*a*' during the voltage transfer ratio transition. At high modulation indexes, the three-level-output-stage matrix converter obviously generates three distinctive voltage levels for V_{ao}, which consists of the positive (V_{po}) and negative envelope (V_{no}) of the rectified input voltages and the zero voltage level. As shown in Figure 5.15(b), a transient response of the output line-to-line voltage V_{ab}, when the voltage transfer ratio steps from 0.4 to 0.8, reveals the transition of the voltage waveform from three levels to five levels, which evidently proves the ability of the three-level-output-stage matrix converter to generate multilevel output voltages. To examine whether the voltage levels are properly applied to generate the desired outputs, the load currents of the three-level-output-stage matrix converter are shown in Figure 5.15(c). These currents are obviously balanced and sinusoidal.

In order to prove that the three-level-output-stage matrix converter generates higher quality output waveforms than the indirect matrix converter, the output line-to-line voltages for these two topologies are compared at high and low modulation indexes, as shown in Figures 5.16 and 5.17. At high modulation indexes, the output line-to-line voltage, V_{ab}, of the three-level-output-stage matrix converter, shown in Figure 5.16(a), consists of five distinctive voltage levels. By constructing the output waveform with multiple voltage levels, the harmonic contents can be reduced, shown by the spectrum in Figure 5.16(c). The output switching frequency harmonics for the three-level-output-stage matrix converter are obviously reduced, from 45V to 32V (f_{sw}) and 104V to 59V ($2f_{sw}$), when comparing the converter with the indirect matrix converter.

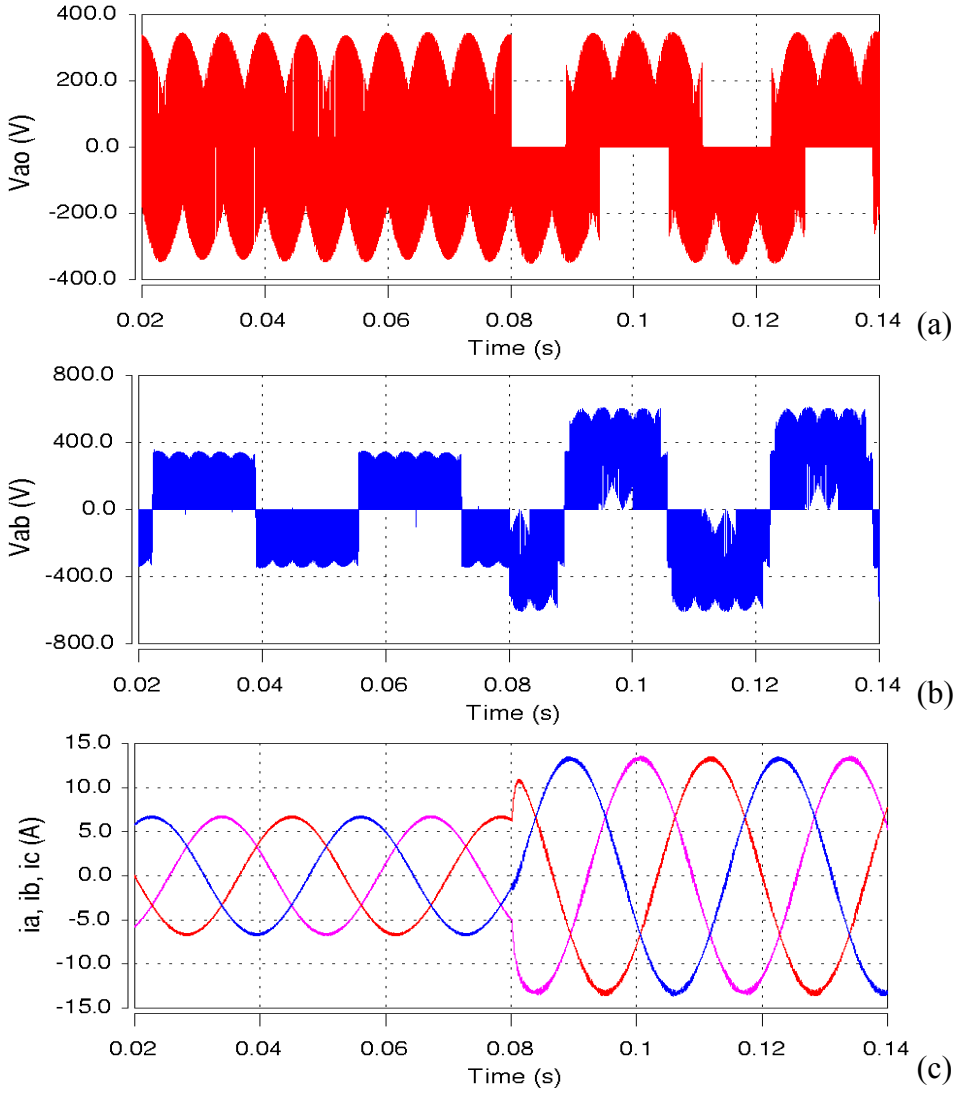


Figure 5.15: The output waveforms generated by the three-level-output-stage matrix converter when the voltage transfer ratio is stepped from 0.4 to 0.8.

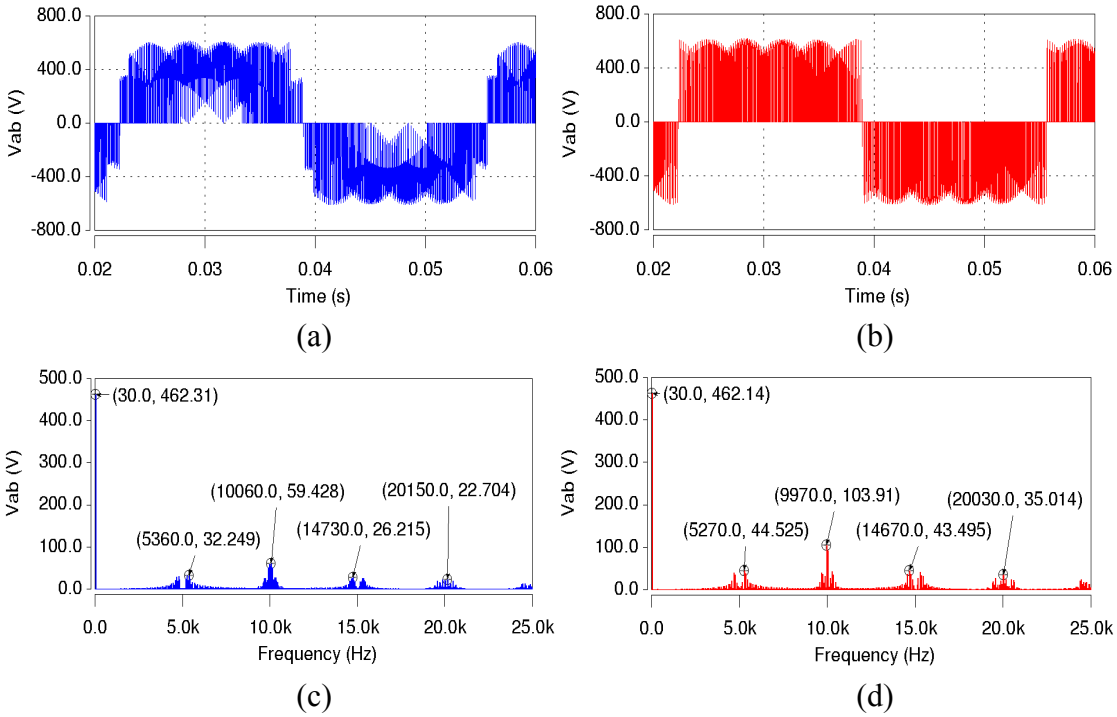


Figure 5.16. Output performance comparison between the three-level matrix converter (left) and the indirect matrix converter (right) at a high modulation index (V_{out_peak} = 270V): (a) (b) output line-to-line voltages (c)(d) output voltage spectra

At low modulation indexes, the output line-to-line voltage of the three-level-output-stage matrix converter, shown in Figure 5.17(a), has a typical three-level profile, which is similar to the indirect matrix converter (Figure 5.17b). However, the magnitude of the voltage level for the three-level-output-stage matrix converter is limited to the input line-to-neutral-point voltage instead of the input line-to-line voltage for the indirect matrix converter. Hence, the voltage ripple generated by the three-level-output-stage matrix converter is definitely lower than for the indirect matrix converter, leading to a reduced harmonic content. By comparing Figure 5.17(c) to Figure 5.17(d), the output voltage harmonics around the switching frequency for the three-level-output-stage matrix converter are reduced, from 19V to 9V (f_{sw}) and from 84V to 26V($2f_{sw}$). Based on the results presented in Figures 5.16 and 5.17, the three-level-output-stage matrix converter is proven able to generate higher quality output waveforms than the indirect matrix converter. In Chapter 7, the output performance comparisons between both topologies will be experimentally verified at realistic power levels.

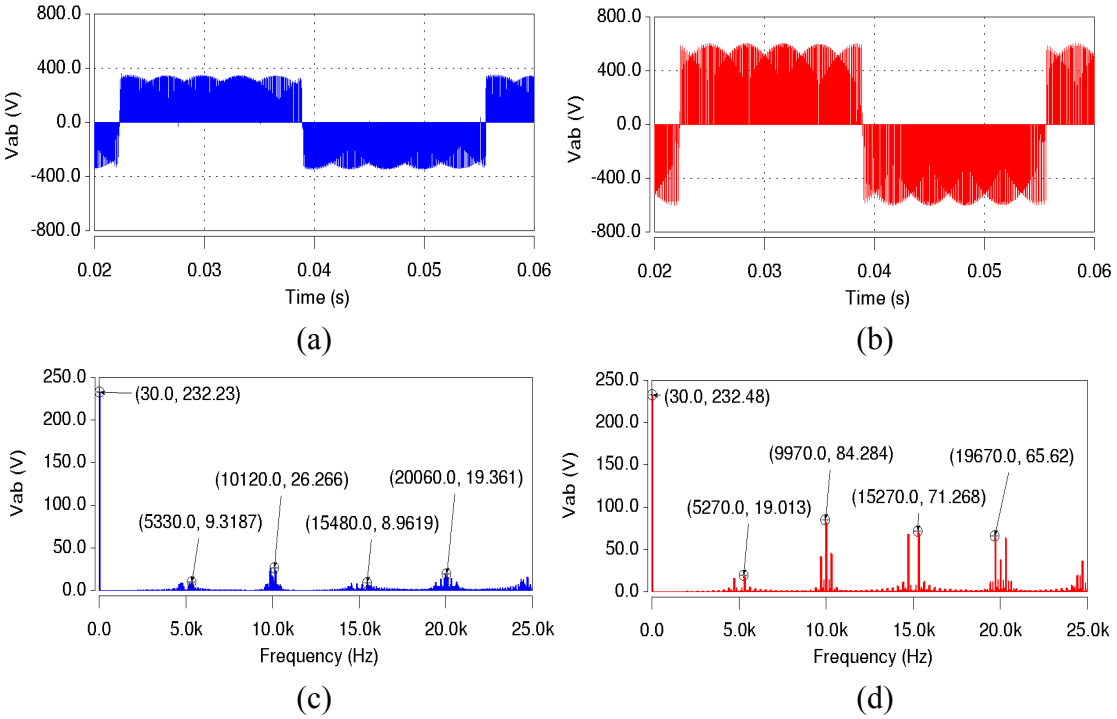


Figure 5.17. Output performance comparison between the three-level matrix converter (left) and the indirect matrix converter (right) at a low modulation index (V_{out_peak} = 135V): (a) (b) output line-to-line voltages (c)(d) output voltage spectra

5.5 Conclusions

In this chapter, an explanation of the operating principles and space vector modulation for the three-level-output-stage matrix converter has been given. Issues related to the neutral-point balancing problem and the unequal DC-link voltages for the three-level-output stage matrix converter, as well as associated control methods, have been discussed. Most importantly, the performance of the three-level-output-stage matrix converter has been analysed, which proves that the converter is able to generate multilevel output voltages and offers better performance than the indirect matrix converter in terms of harmonic content in the output waveforms.

Chapter 6

Indirect Three-level Sparse Matrix Converter

6.1 Introduction

The ability of the three-level-output-stage matrix converter to generate multilevel output voltages has been shown in Chapter 5. Even though this three-level matrix converter topology generates higher quality output waveforms than the indirect matrix converter, the high number of power semiconductor devices means that this topology has disadvantages in terms of cost and circuit complexity.

In order to make the multilevel matrix converter concept attractive in industrial applications, the indirect three-level sparse matrix converter has been proposed by the Author in [71]. It is a multilevel neutral-point-clamped matrix converter topology that integrates the simplified three-level neutral-point-clamped voltage source inverter concept, discussed in Chapter 4, into an indirect matrix converter topology. As shown in Figure 6.1, the circuit configuration of the indirect three-level sparse matrix converter is simpler than the three-level-output-stage matrix converter, given in Figure 5.1. Compared to the indirect matrix converter, only two additional unidirectional switches are required to be connected as an additional inverter leg (neutral-point commutator) in the DC-link in order to enhance its output voltage capability from the conventional two-level to three-level line-to-supply neutral voltage.

In this chapter, a space vector modulation strategy for the indirect three-level sparse matrix converter is described. First, the operating principles of the indirect three-level sparse matrix converter are discussed. Then a detailed explanation of the modulation strategy is given. Simulation results are presented to prove the effectiveness of the modulation strategy in allowing the converter to generate the desired input and output waveforms. Finally, the performance of the indirect three-level sparse matrix converter is compared with the indirect matrix converter and the three-level-output-stage matrix

converter to show that the indirect three-level sparse matrix converter has the advantages over these other topologies.

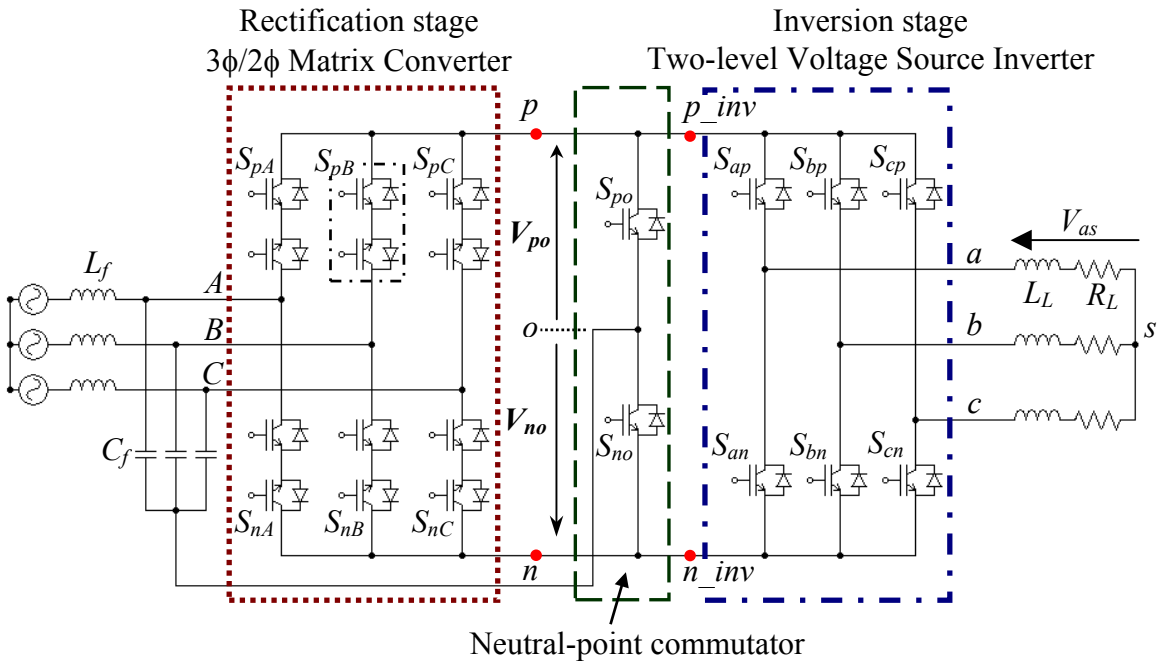


Figure 6.1: The indirect three-level sparse matrix converter circuit.

6.2 Circuit Topology

As shown in Figure 6.1, the indirect three-level sparse matrix converter consists of a rectification stage, a neutral-point commutator and a two-level voltage source inverter. Similar to the indirect matrix converter, the rectification stage is a three-phase to two-phase matrix converter that is used to build up a switching DC-link voltage, V_{pn}, for the inversion stage. At any instant, only two bi-directional switches in the rectification stage are turned on to connect an input line-to-line voltage to the DC-link. The positive voltage level is applied to the DC-link '*p*' terminal and negative voltage level to the '*n*' terminal, as shown in Table 6.1. Therefore, the rectification stage can be represented using two conducting switches, S_{py} and S_{ny} (y∈{A, B, C}), as shown in Figure 6.2.

Switching Combinations						Voltage levels applied to		V_{pn}
S_{pA}	S_{pB}	S_{pC}	S_{nA}	S_{nB}	S_{nC}	p	n	
1	0	0	0	1	0	$V_{po} = V_{Ao}$	$V_{no} = V_{Bo}$	V_{AB}
0	1	0	1	0	0	$V_{po} = V_{Bo}$	$V_{no} = V_{Ao}$	V_{BA}
0	1	0	0	0	1	$V_{po} = V_{Bo}$	$V_{no} = V_{Co}$	V_{BC}
0	0	1	0	1	0	$V_{po} = V_{Co}$	$V_{no} = V_{Bo}$	V_{CB}
0	0	1	1	0	0	$V_{po} = V_{Co}$	$V_{no} = V_{Ao}$	V_{CA}
1	0	0	0	0	1	$V_{po} = V_{Ao}$	$V_{no} = V_{Co}$	V_{AC}

Table 6.1: The switching combinations for the rectification stage (1 = ON, 0 = OFF)

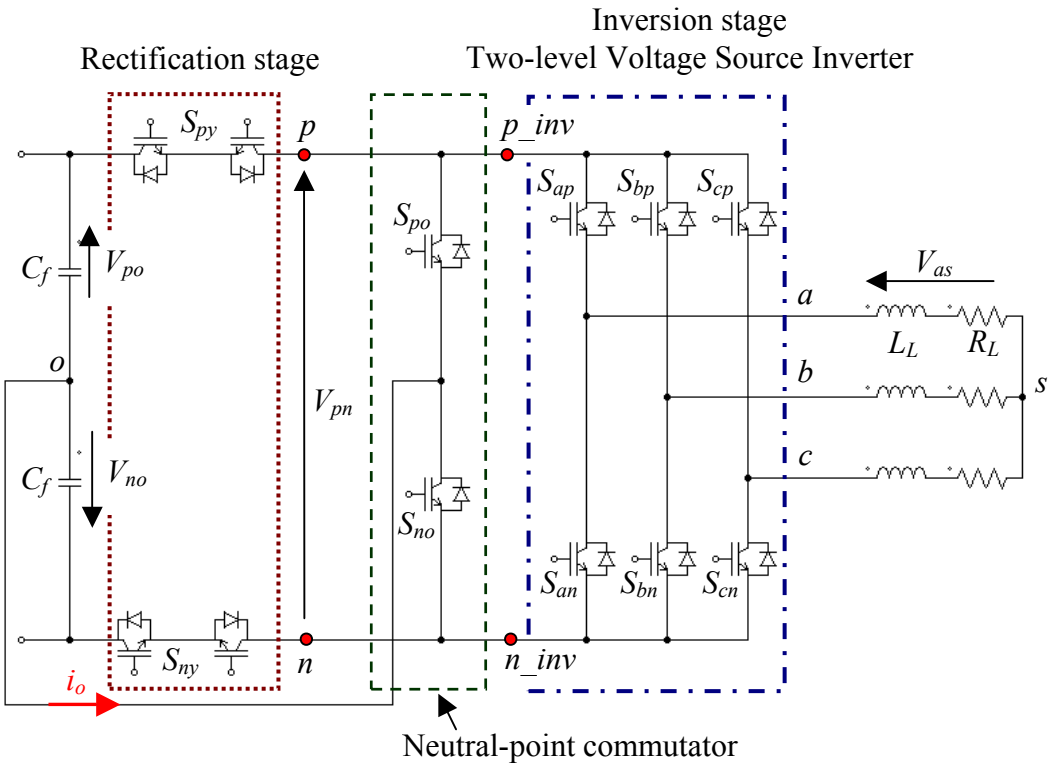


Figure 6.2: The equivalent state circuit for the indirect three-level sparse matrix converter with the rectification stage represented using two conducting switches (S_{py} and S_{ny})

By connecting the DC-link middle point '*o*' to the neutral-point of the star-connected input filter capacitors, the DC-link voltage, V_{pn}, is transformed into dual voltage supplies, V_{po} and V_{no}. The middle point '*o*' acts as a zero DC voltage neutral-point. The circuit given in Figure 6.2 clearly resembles the simplified three-level neutral-point-clamped voltage source inverter, where the combination of the rectification stage and neutral-point commutator is identical to the three-level dual buck stage. Using the DC-link middle point '*o*' as a reference, there are obviously three voltage levels available: V_{po}, $0V$ and V_{no}. At any instant, the inversion stage can only be operated using two voltage levels. Therefore, the rectification stage and neutral-point commutator have to be controlled, according to the switching combinations in Table 6.2, to supply two of the three voltage levels to the inversion stage's input terminals (*p_inv* and *n_inv*). To prevent DC-link short circuits, the switching states for the S_{py} and S_{ny} have to be opposite to those for S_{po} and S_{no} respectively.

Switching Combination				Voltage level applied to	
S_{py}	S_{po}	S_{no}	S_{ny}	*p_inv*	*n_inv*
ON	OFF	OFF	ON	V_{po}	V_{no}
OFF	ON	OFF	ON	$0V$	V_{no}
OFF	ON	ON	OFF	$0V$	$0V$
ON	OFF	ON	OFF	V_{po}	$0V$

Table 6.2: The switching combinations for the rectification stage and the neutral-point commutator (y∈{A, B, C})

The inversion stage can then be modulated to generate the three-level output according to the switching combinations presented in Table 6.3. The switches in each phase leg of the two-level voltage source inverter are modulated based on the following expression:

$$S_{xp} + S_{xn} = 1 \qquad x \in \{a, b, c,\} \tag{6.1}$$

where S_{xp} and S_{xn} are the switching functions of the top and bottom unidirectional switches, respectively. Referring to Table 6.3, each output terminal voltage (V_{xo}) of the inversion stage obviously has three possible voltage levels: V_{po}, 0V and V_{no}, which proves the converter's ability to generate multilevel outputs.

Rectifier/Neutral point Commutator				Voltage source inverter		Output terminal voltage, V_{xo}
S_{py}	S_{po}	S_{no}	S_{ny}	S_{xp}	S_{xn}	
ON	OFF	OFF	ON	ON	OFF	V_{po}
ON	OFF	ON	OFF	ON	OFF	V_{po}
ON	OFF	OFF	ON	OFF	ON	V_{no}
OFF	ON	OFF	ON	OFF	ON	V_{no}
OFF	ON	OFF	ON	ON	OFF	*0V*
OFF	ON	ON	OFF	ON	OFF	*0V*
OFF	ON	ON	OFF	OFF	ON	*0V*
ON	OFF	ON	OFF	OFF	ON	*0V*

Table 6.3: The switching combinations for the indirect three-level sparse matrix converter (x $\in$ {a, b, c} and y $\in$ {A, B, C})

With the ability to generate the three-level outputs, the indirect three-level sparse matrix converter is obviously able to generate higher quality output waveforms than the indirect matrix converter. Compared to the three-level-output-stage matrix converter, the simpler circuit configuration of the indirect three-levels sparse matrix converter is definitely an advantage. However, due to the ability to connect the output terminal(s) to the neutral-point, the indirect three-level sparse matrix converter inevitably has the neutral-point balancing problem. This problem could cause output voltage distortion if the neutral-point current, i_o, that flows to the input filter capacitors is not properly controlled. In the same way as for the three-level-output-stage matrix converter the unequal DC-link voltages, V_{po} and V_{no}, provided by the rectification stage have to be considered when modulating the indirect three-level sparse matrix converter.

To modulate the indirect three-level sparse matrix converter to generate a set of balanced and sinusoidal input and output waveforms, associated modulation/control methods have been proposed in [70, 71]. Proposed by the Author in [71], a space vector modulation strategy (SVM) is derived based on the mix of concepts of the indirect SVM applied to the indirect matrix converter and the SVM for the simplified three-level neutral-point-clamped voltage source inverter that was discussed in Chapter 4. This modulation strategy will be explained in detail in the following section.

6.3 Space Vector Modulation

Based on the strategy proposed in [71], the rectification stage of the indirect three-level sparse matrix converter is modulated using SVM to generate the dual DC-link voltages for the inversion stage. Having three voltage levels at the DC-link, the SVM strategy that was discussed in Chapter 4 is then applied to modulate the inversion stage to generate the desired outputs as well as control the rectification stage and neutral-point commutator to supply the required voltage levels to the inversion stage's terminals (*p_inv* and *n_inv*).

The modulation of each stage produces a combination of vectors to synthesise a reference vector of given amplitude and angle. After determining the vectors and their duty cycles, the modulation pattern of the indirect three-level sparse matrix converter then combines the switching states for both stages uniformly so that a correct balance of the input currents and output voltages can be obtained during each switching period.

6.3.1 The Rectification Stage

For the indirect three-level sparse matrix converter, the rectification stage not only has to generate the DC-link voltages for the inversion stage but also has to maintain a set of sinusoidal, balanced input currents with controllable displacement angle in respect to the input voltages. By applying SVM, as reviewed in Section 2.3.2.1, the input current vector, $\bar{I}_{in}$, is the reference vector for the rectification stage and can be expressed as:

$$\bar{I}_{in} = I_{im} e^{j(\omega_i t - \varphi_i)} = I_{im} \angle \theta_i \tag{6.2}$$

where I_{im} is the magnitude and θ_i (= $\omega_i t$ - φ_i) is the direction of the reference vector. $\omega_i t$ is the angle of the input voltages and φ_i is the displacement angle of the input currents with respect to the input voltages.

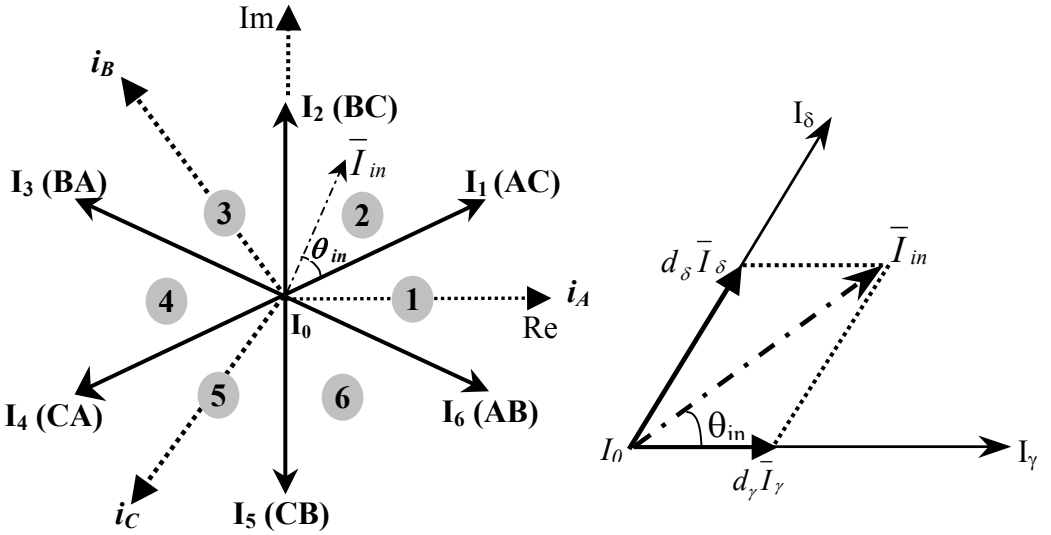
To synthesise a reference vector, $\bar{I}_{in}$, that rotates in the space vector diagram, as shown in Figure 6.3(a), two adjacent current vectors (I_γ and I_δ) and a zero current vector (I_0) are selected based on the sector where the $\bar{I}_{in}$ is located at the sampling instant. As shown in Figure 6.3(b), the proportion between the duty cycles of I_γ and I_δ defines the direction and the duty cycle of I_0 determines the magnitude of $\bar{I}_{in}$. The duty cycles for the vectors I_γ, I_δ and I_0 are determined using (6.3), where m_R is the modulation index of the rectification stage and θ_{in} is the angle of the reference vector within the sector.

$$d_\gamma = m_R \cdot \sin\left(\frac{\pi}{3} - \theta_{in}\right) \qquad d_\delta = m_R \cdot \sin(\theta_{in}) \qquad d_0 = 1 - d_\gamma - d_\delta \tag{6.3}$$

For the indirect three-level sparse matrix converter, the rectification stage is modulated to generate maximum DC-link voltage, V_{pn}, so that maximum V_{po} and V_{no} are provided for the inversion stage. For this reason, the modulation index, m_R, is set to unity (=1) and input displacement factor is controlled to zero (unity power factor). To simplify the overall modulation process, only the modulation on the inversion stage produces zero-vectors. Hence, the zero current vector is eliminated and the rectification stage's switching sequence only consists of the vectors I_γ and I_δ. By determining the duty cycles d_γ and d_δ (6.3) with the modulation index m_R = 1, the rectification stage's duty cycles are then adjusted using (6.4) to occupy the whole switching period.

$$d_\gamma{}^R = \frac{d_\gamma}{d_\gamma + d_\delta} \qquad d_\delta{}^R = \frac{d_\delta}{d_\gamma + d_\delta} \tag{6.4}$$

Due to the zero current vector cancellation, the average DC-link voltage over a switching period is not constant and needs to be determined using equation (6.5). With



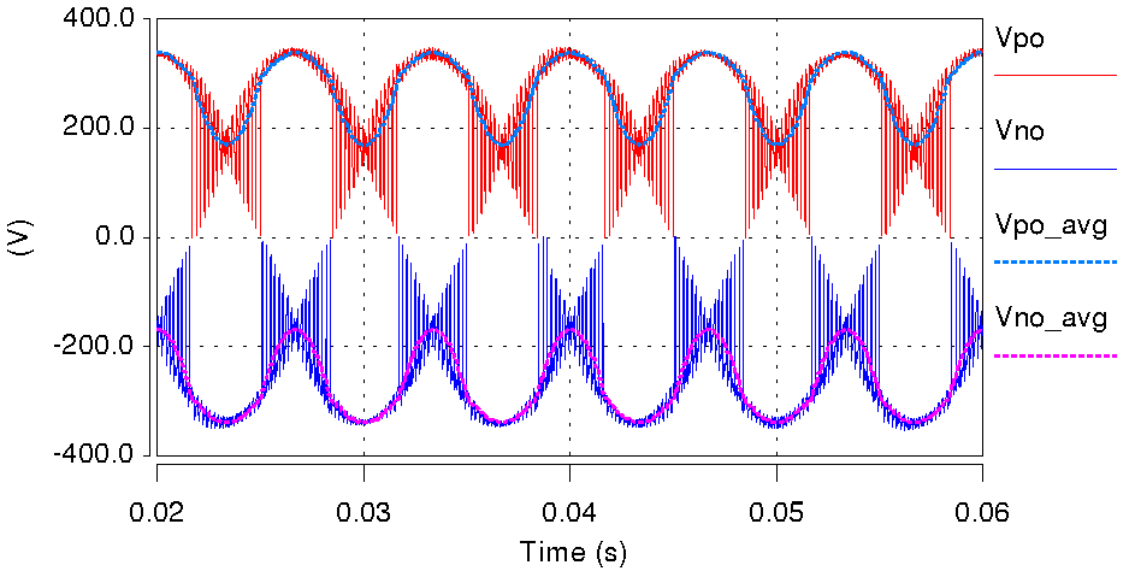
(a) (b)

Figure 6.3: (a) The space vector diagram for the rectification stage (b) To synthesise a reference vector in a given sector

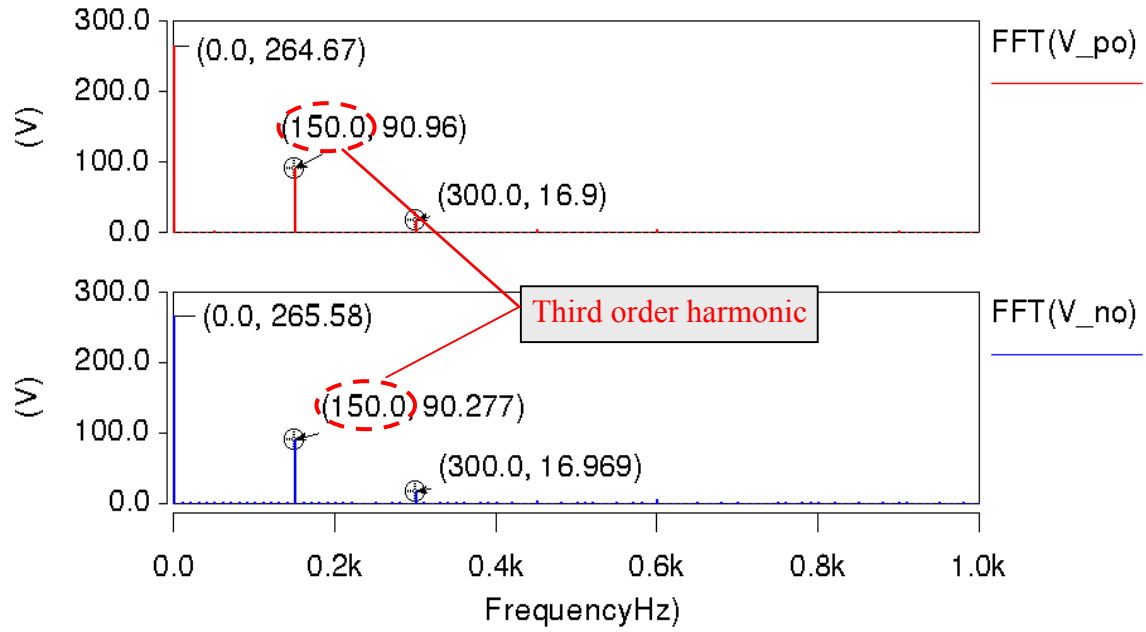
the maximum average DC-link voltage, V_{pn_avg}, supplied by the rectification stage, the modulation on the inversion stage controls the overall voltage transfer ratio of the converter.

$$V_{pn\_avg} = d_\gamma{}^R V_{l-l\gamma} + d_\delta{}^R V_{l-l\delta} \tag{6.5}$$

In order to have three voltage levels at the DC-links, V_{pn} is transformed into V_{po} and V_{no} by connecting the DC-link middle point '*o*' to the neutral-point of the input filter capacitor, as shown in Figure 6.1. However, the voltages V_{po} and V_{no} provided by the rectification stage are not equal, as shown in Figure 6.4(a). Referring to their spectra, shown in Figure 6.4(b), these DC-link voltages clearly consist of a DC component and a third order harmonic of the input frequency that is inherently included in the rectification stage's output when it is modulated using SVM. Similar to the three-level-output-stage matrix converter, for each switching period, the inversion stage of the indirect three-level sparse matrix converter is modulated based on the averages of V_{po} and V_{no}. Identifying that the third order harmonics for the DC-link voltages are 180^0 output of phase, as shown in Figure 6.4(a), the averages of V_{po} and V_{no} can be approximated as below:



(a) The DC-link voltage waveforms



(b) The spectra of the DC-link voltage waveforms

Figure 6.4. The DC-link voltages, V_{po} and V_{no}, provided by the rectification stage with a supply frequency of 50Hz.

$$V_{po\_avg} = \left(V_{pn\_avg} \Big/ 2 \right) + \left(\frac{V_{pn\_avg}}{6} \right) \cdot \cos(3 \cdot \omega_i \cdot t)$$

$$V_{no\_avg} = -\left(V_{pn\_avg} \Big/ 2 \right) + \left(\frac{V_{pn\_avg}}{6} \right) \cdot \cos(3 \cdot \omega_i \cdot t) \quad (6.6)$$

where ω_i is equal to $2\pi f_i$ with f_i = frequency of the supply voltages. The waveforms 'V_{po_avg}' and 'V_{no_avg}', shown in Figure 6.4(a), clearly resemble the low frequency DC-link voltages, V_{po} and V_{no}.

6.3.2 The Inversion Stage

By representing the rectification stage using two conducting switches, the indirect three-level sparse matrix converter resembles the simplified three-level neutral-point-clamped voltage source inverter. Therefore, based on V_{po_avg} and V_{no_avg}, the SVM strategy that was discussed in Chapter 4 can be applied to modulate the inversion stage to generate the multilevel output voltages as well as control the rectification stage and neutral-point commutator to supply the required voltage levels to the inversion stage's input terminals (*p_inv* and *n_inv*). However, as shown in Figure 6.4, the V_{po_avg} and V_{no_avg} provided by the rectification stage are not equal. In order to effectively modulate the inversion stage to generate the desired outputs, the effects of V_{po_avg} and V_{no_avg} on the voltage space vectors must be firstly examined. For this reason, the output voltages generated by the switching states of the inversion stage have to be determined.

Similar to the simplified three-level neutral-point-clamped voltage source inverter, by representing each DC-link voltage level with a switching state: $P = V_{po\_avg}$, O = 0V and $N = V_{no\_avg}$, the indirect three-level sparse matrix converter can generate twenty-one switching states that represent the voltage levels connected to the output terminals (*a*, *b* and *c*), as shown in Table 4.3. To facilitate explanation, only the switching states listed in Table 6.4 are analysed. The output phase voltages generated by each switching state are determined using equation (6.7), which is derived based on (4.2) but expressed in terms of V_{po_avg} and V_{on_avg} (= $-V_{no\_avg}$). m_{x1} and m_{x2} represent the switch combinations (S_{py} & S_{xp}) and (S_{ny} & S_{xn}), which is one when both switches in the combination are 'on' or zero otherwise. Referring to Table 6.4, the output phase voltages generated by each

switching state clearly depend on the connected DC-link voltage and the instantaneous value. For example, switching state *POO* applies only the V_{po_avg} to the output. As a result, the output phase voltages generated by *POO* is apparently different to *ONN*, which uses only the V_{on_avg}. However, when $V_{po\_avg} = V_{on\_avg}$, the output voltages generated by *POO* and *ONN* would be identical, as shown in Table 4.3.

$$V_{as} = \left(\tfrac{1}{3}\right)\left[V_{po\_avg}\left(2 \cdot m_{a1} - m_{b1} - m_{c1}\right) - V_{on\_avg}\left(2 \cdot m_{a2} - m_{b2} - m_{c2}\right)\right]$$

$$V_{bs} = \left(\tfrac{1}{3}\right)\left[V_{po\_avg}\left(2 \cdot m_{b1} - m_{a1} - m_{c1}\right) - V_{on\_avg}\left(2 \cdot m_{b2} - m_{a2} - m_{c2}\right)\right]$$

$$V_{cs} = \left(\tfrac{1}{3}\right)\left[V_{po\_avg}\left(2 \cdot m_{c1} - m_{a1} - m_{b1}\right) - V_{on\_avg}\left(2 \cdot m_{c2} - m_{a2} - m_{b2}\right)\right] \qquad (6.7)$$

Using space vector transformation (4.4), the output phase voltages generated by these switching states can be converted into voltage space vectors, shown in Table 6.4. As an example, these voltage space vectors for the case where $V_{po\_avg} > V_{on\_avg}$ are shown in Figure 6.5. Compared to Figure 4.3, the small voltage vectors (SVV) are obviously affected by the unequal DC-link voltages. At any instant, except when $V_{po\_avg} = V_{on\_avg}$, each redundant switching state of a SVV (e.g. V_1) generates different magnitude of voltage vector (V_{1A} and V_{1B}) due to the use of different DC-link voltages. The large voltage vectors (V_2 and V_4) for the indirect three-level sparse matrix converter are not affected because $V_{po\_avg} + V_{on\_avg}$ is equal to V_{pn_avg}.

Conventionally, to synthesize the reference output vector ($\overline{V}_{out}$) of the inversion stage, three nearest voltage vectors are selected based on the triangle that the reference vector is located in at the sampling instant. However, the SVVs with varying magnitudes complicate the process of synthesizing $\overline{V}_{out}$. In order to simplify this process, the redundant switching states of each SVV pair are linearly combined to form a virtual small voltage vector (V_{SV}) with fixed magnitude and direction, as shown in Figure 6.6. C_1 to C_4 are used to control the active time of these varying voltage vectors within the combinations. At any instant, the magnitudes of V_{SV} are set at $V_{pn\_avg}/3$, which are obtained using even DC-link voltages ($V_{po\_avg} = V_{on\_avg} = V_{pn\_avg}/2$). In order to maintain V_{SV}, C_1 to C_4 are adjusted according to the magnitudes of SVVs at the sampling instant.

			Output phase voltages			Output voltage space vectors		
a	*b*	*c*	V_{as}	V_{bs}	V_{cs}	$\overline{V}$	Magnitude	Angle
P	P	P	0	0	0	V_0	0	0
O	O	O	0	0	0			
N	N	N	0	0	0			
P	O	O	$\frac{2}{3}\cdot V_{po\_avg}$	$-\frac{1}{3}\cdot V_{po\_avg}$	$-\frac{1}{3}\cdot V_{po\_avg}$	V_{1A}	$\frac{2}{3}\cdot V_{po\_avg}$	0
O	N	N	$\frac{2}{3}\cdot V_{on\_avg}$	$-\frac{1}{3}\cdot V_{on\_avg}$	$-\frac{1}{3}\cdot V_{on\_avg}$	V_{1B}	$\frac{2}{3}\cdot V_{on\_avg}$	0
P	N	N	$\frac{2}{3}(V_{po\_avg}+V_{on\_avg})$	$-\frac{1}{3}(V_{po\_avg}+V_{on\_avg})$	$-\frac{1}{3}(V_{po\_avg}+V_{on\_avg})$	V_2	$\frac{2}{3}\cdot(V_{po\_avg}+V_{on\_avg})$	0
P	P	O	$\frac{1}{3}\cdot V_{po\_avg}$	$\frac{1}{3}\cdot V_{po\_avg}$	$-\frac{2}{3}\cdot V_{po\_avg}$	V_{3A}	$\frac{2}{3}\cdot V_{po\_avg}$	π/3
O	O	N	$\frac{1}{3}\cdot V_{on\_avg}$	$\frac{1}{3}\cdot V_{on\_avg}$	$-\frac{2}{3}\cdot V_{on\_avg}$	V_{3B}	$\frac{2}{3}\cdot V_{on\_avg}$	π/3
P	P	N	$\frac{1}{3}(V_{po\_avg}+V_{on\_avg})$	$\frac{1}{3}(V_{po\_avg}+V_{on\_avg})$	$-\frac{2}{3}(V_{po\_avg}+V_{on\_avg})$	V_4	$\frac{2}{3}\cdot(V_{po\_avg}+V_{on\_avg})$	π/3

Table 6.4: The output phase voltages and voltage space vectors generated by the switching states of the inversion stage.

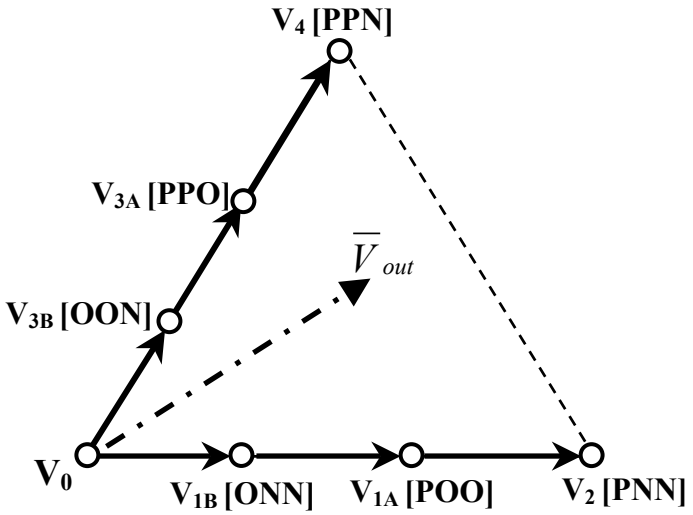


Figure 6.5: The voltage vectors generated by the unequal DC-link voltages for the case where $V_{po\_avg} > V_{on\_avg}$

- $|\mathbf{V_{SV1}}| = |\mathbf{V_{SV3}}| = V_{pn\_avg}/3$
- $|\mathbf{V_{V2}}| = |\mathbf{V_{V4}}| = 2V_{pn\_avg}/3$
- $\theta_{VSV1}, \theta_{V2} = 0$
- $\theta_{VSV3}, \theta_{V4} = \pi/3$

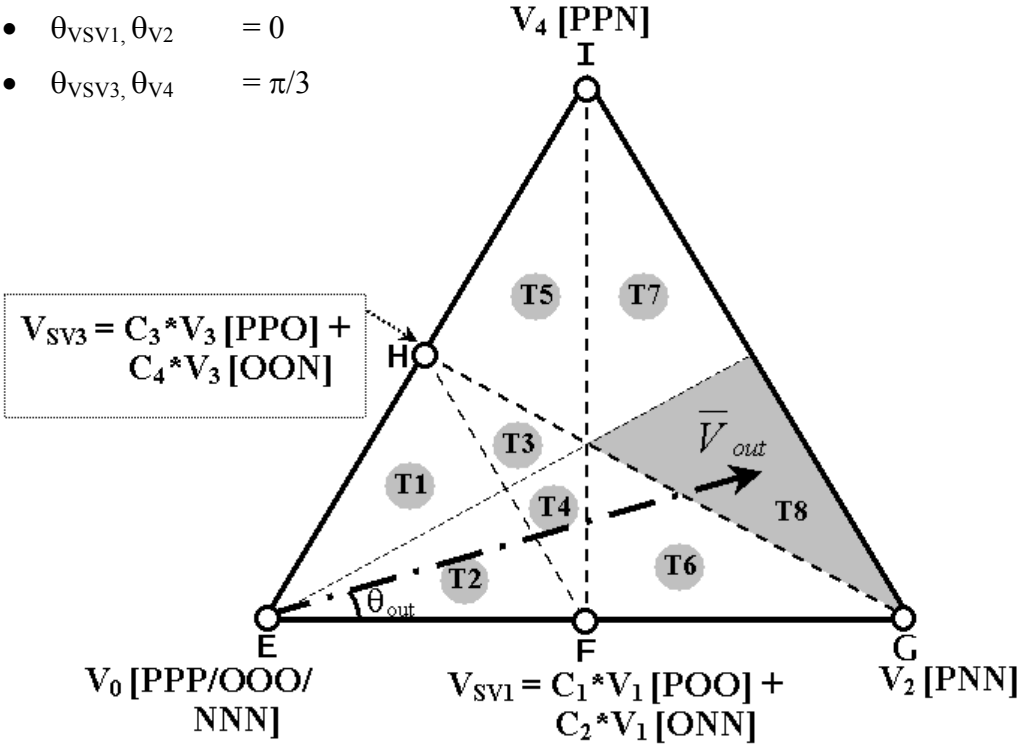


Figure 6.6: The sector 1 of the space vector diagram for the indirect three-level sparse matrix converter

The equations of calculating C_1 to C_4 are presented in (6.8), where the effects of unequal DC-link voltages are taken into consideration in the calculations.

$$C_1 = C_3 = \left(\frac{V_{on\_avg} - \left[V_{pn\_avg} \big/ 2 \right]}{V_{on\_avg} - V_{po\_avg}} \right), \qquad C_2 = C_4 = \left(\frac{\left[V_{pn\_avg} \big/ 2 \right] - V_{po\_avg}}{V_{on\_avg} - V_{po\_avg}} \right) \tag{6.8}$$

To determine how C_1 to C_4 vary due to the unequal DC-link voltages, equations (6.6) are substituted into (6.8), where $V_{on\_avg} = - V_{no\_avg}$. Due to the 180^o phase displacement of the third order harmonics of the DC-link voltages, $C_1 = C_2 = C_3 = C_4 = ½$, as shown below:

$$C_1 = C_3 = \left(\frac{\frac{V_{pn\_avg}}{2} - \frac{V_{pn\_avg}}{6}\cos(\theta) - \left[V_{pn\_avg} \middle/ 2 \right]}{\frac{V_{pn\_avg}}{2} - \frac{V_{pn\_avg}}{6}\cos\theta - \frac{V_{pn\_avg}}{2} - \frac{V_{pm\_avg}}{6}\cos\theta} \right) = \frac{-\frac{V_{pn\_avg}}{6}\cos\theta}{-\frac{2V_{pn\_avg}}{6}\cos\theta} = \frac{1}{2}$$

This result clearly shows that V_{SV} are formed with equal linear combinations of SVVs, although the unequal DC-link voltages affect the magnitudes of SVVs. This is because, when forming V_{SV}, the effect of V_{po_avg} on one voltage vector is balanced by the effect of V_{on_avg} on another. For example, when $V_{po\_avg} > V_{on\_avg}$, the magnitude of *POO* is increased but, due to the 180° phase displacement of V_{on_avg}, the magnitude of *ONN* is decreased. Hence, to achieve the correct magnitude of V_{SV1}, the vector is formed by an equal combination of *POO* and *ONN* ($C_1 = C_2 = ½$). Table 6.5 shows the voltage vector combinations that form the virtual small voltage vectors for the inversion stage of the indirect three-level sparse matrix converter.

Having a set of vectors with fixed magnitude and direction, the space vector diagram for the inversion stage, as shown in Figure 6.7, is similar to the diagram given in Figure 4.2. Hence, the procedure of synthesizing the reference vector, $\overline{V}_{out}$, for the inversion stage of the indirect three-level sparse matrix converter is similar to the procedure described in Section 4.3, where the three nearest voltage vectors are selected based on the triangle in which the reference vector is located at the sampling instant. The duty cycle equations for the selected vectors in each triangle are shown in Table 6.6, where the modulation index of the inversion stage, m_I, is equal to (6.9) and θ_{out} is the angle of the reference vector within the sector. The selected vectors are applied to the output according to the switching sequences presented in Tables 6.7 to 6.9. With $C_1 = C_2 = C_3 = C_4 = ½$, the SVVs that form the virtual small voltage vectors are equally applied within the switching sequences. For example, if V_{SV1} is selected for an interval t_{SV}, *POO* and *ONN* are equally active for $½*t_{SV}$.

$$m_I = \frac{\sqrt{3} * V_{om}}{V_{pn\_avg}} \tag{6.9}$$

Virtual Small Vector			Vector Combination	
Vector	Magnitude	Angle		
V_{SV1}	$\frac{2}{3} V_{pn\_avg}$	0	ONN	POO
V_{SV3}	$\frac{2}{3} V_{pn\_avg}$	$\pi/3$	PPO	OON
V_{SV5}	$\frac{2}{3} V_{pn\_avg}$	$2\pi/3$	NON	OPO
V_{SV7}	$\frac{2}{3} V_{pn\_avg}$	π	OPP	NOO
V_{SV9}	$\frac{2}{3} V_{pn\_avg}$	$-2\pi/3$	NNO	OOP
V_{SV11}	$\frac{2}{3} V_{pn\_avg}$	$-\pi/3$	POP	ONO

Table 6.5: The voltage vector combination for each virtual small voltage vector

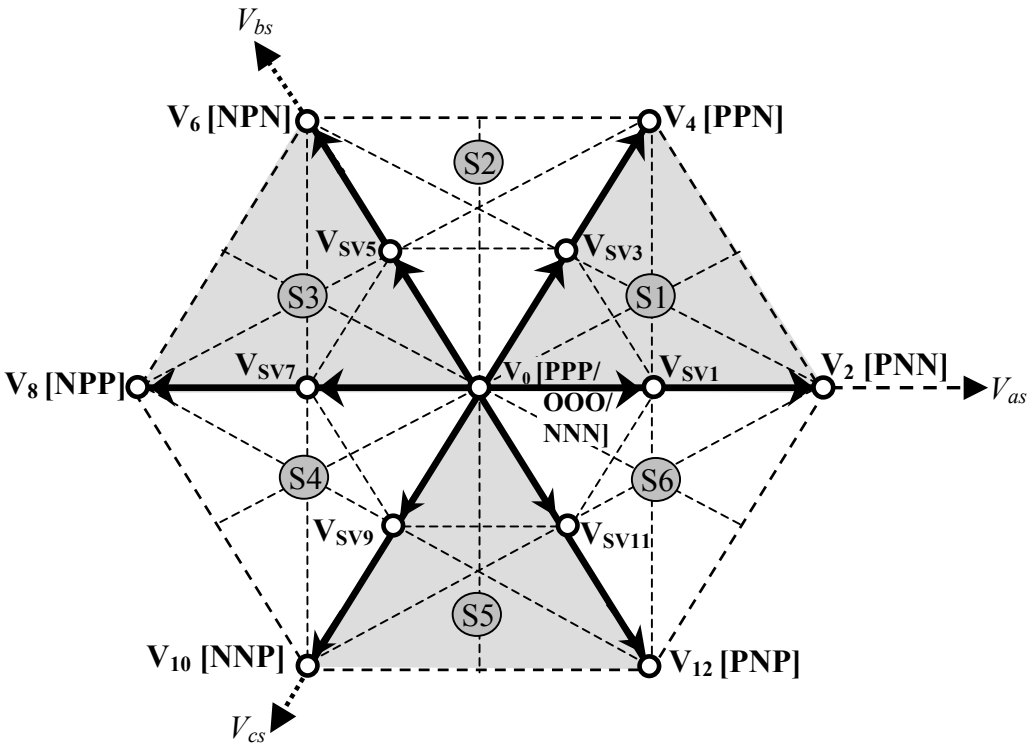


Figure 6.7: The space vector diagram for the inversion stage of the indirect three-level sparse matrix converter

Triangle	Duty cycle equations
T1/T2 (ΔEFH)	• $d_{V0} = 1 - m_I\left(\sqrt{3}\cdot\cos\theta_{out} + \sin\theta_{out}\right)$ • $d_{VSV1} = m_I\left(\sqrt{3}\cdot\cos\theta_{out} - \sin\theta_{out}\right)$ • $d_{VSV3} = 2\cdot m_I\cdot\sin\theta_{out}$
T3/T5 (ΔFHI)	• $d_{VSV1} = m_I\left(\sqrt{3}\cdot\cos\theta_{out} - \sin\theta_{out}\right)$ • $d_{VSV3} = 2 - 2\cdot\sqrt{3}\cdot m_I\cdot\sin\theta_{out}$ • $d_{V4} = m_I\left(\sqrt{3}\cdot\cos\theta_{out} + \sin\theta_{out}\right) - 1$
T4/T6 (ΔFHG)	• $d_{VSV1} = 2 - m_I\left(\sqrt{3}\cdot\cos\theta_{out} + 3\sin\theta_{out}\right)$ • $d_{V2} = m_I\left(\sqrt{3}\cdot\cos\theta_{out} + \sin\theta_{out}\right) - 1$ • $d_{VSV3} = 2\cdot m_I\cdot\sin\theta_{out}$
T7 (ΔHIG)	• $d_{V2} = 0.5\cdot m_I\left(\sqrt{3}\cdot\cos\theta_{out} - \sin\theta_{out}\right)$ • $d_{VSV3} = 2 - m_I\left(\sqrt{3}\cdot\cos\theta_{out} + \sin\theta_{out}\right)$ • $d_{V4} = 0.5\cdot m_I\left(\sqrt{3}\cdot\cos\theta_{out} + 3\cdot\sin\theta_{out}\right) - 1$
T8 (ΔFGI)	• $d_{VSV1} = 2 - m_I\left(\sqrt{3}\cdot\cos\theta_{out} + 3\sin\theta_{out}\right)$ • $d_{V2} = \sqrt{3}\cdot m_I\cdot\cos\theta_{out} - 1$ • $d_{V4} = m_I\cdot\sin\theta_{out}$

Table 6.6: The duty cycle equations for the selected vectors in each triangle

Triangle	Sector	t_1			t_2			t_3			t_4			t_5			t_6			t_7		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T1/T2 (ΔEFH)	1	P	P	P	P	P	O	P	O	O	O	O	O	O	O	N	O	N	N	N	N	N
	2	P	P	P	P	P	O	O	P	O	O	O	O	O	O	N	N	O	N	N	N	N
	3	P	P	P	O	P	P	O	P	O	O	O	O	N	O	O	N	O	N	N	N	N
	4	P	P	P	O	P	P	O	O	P	O	O	O	N	O	O	N	N	O	N	N	N
	5	P	P	P	P	O	P	O	O	P	O	O	O	O	N	O	N	N	O	N	N	N
	6	P	P	P	P	O	P	P	O	O	O	O	O	O	N	O	O	N	N	N	N	N

Table 6.7: The switching sequences for triangles T1 and T2

Triangle	Sector	t_1			t_2			t_3			t_4			t_5		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T3/T5 (ΔFHI)	1	P	O	O	P	P	O	P	P	N	O	O	N	O	N	N
	2	P	P	O	O	P	O	N	P	N	N	O	N	O	O	N
	3	O	P	O	O	P	P	N	P	P	N	O	O	N	O	N
	4	O	P	P	O	O	P	N	N	P	N	N	O	N	O	O
	5	O	O	P	P	O	P	P	N	P	O	N	O	N	N	O
	6	P	O	P	P	O	O	P	N	N	O	N	N	O	N	O
T4/T6 (ΔFHG)	1	P	P	O	P	O	O	P	N	N	O	N	N	O	O	N
	2	O	P	O	P	P	O	P	P	N	O	O	N	N	O	N
	3	O	P	P	O	P	O	N	P	N	N	O	N	N	O	O
	4	O	O	P	O	P	P	N	P	P	N	O	O	N	N	O
	5	P	O	P	O	O	P	N	N	P	N	N	O	O	N	O
	6	P	O	O	P	O	P	P	N	P	O	N	O	O	N	N

Table 6.8: The switching sequences for triangles T3 to T6

Triangle	Sector	t_1			t_2			t_3			t_4		
		a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*
T7 (ΔHIG)	1	P	P	O	P	P	N	P	N	N	O	O	N
	2	O	P	O	N	P	N	P	P	N	N	O	N
	3	O	P	P	N	P	P	N	P	N	N	O	O
	4	O	O	P	N	N	P	N	P	P	N	N	O
	5	P	O	P	P	N	P	N	N	P	O	N	O
	6	P	O	O	P	N	N	P	N	P	O	N	N
T8 (ΔFGI)	1	P	O	O	P	N	N	P	P	N	O	N	N
	2	P	P	O	P	P	N	N	P	N	O	O	N
	3	O	P	O	N	P	N	N	P	P	N	O	N
	4	O	P	P	N	P	P	N	N	P	N	O	O
	5	O	O	P	N	N	P	P	N	P	N	N	O
	6	P	O	P	P	N	P	P	N	N	O	N	O

Table 6.9: The switching sequences for triangles T7 and T8

By applying the redundant switching states of SVVs to the output equally, the neutral-point balancing problem of the indirect three-level sparse matrix converter can be controlled. As shown in Table 6.3, each output terminal of the inversion stage can be connected to the DC-link middle point '*o*' for the zero DC-voltage level (V_{xo} = 0V). Whenever the output terminal is connected to point '*o*', the neutral-point current, i_o, can cause uneven charging or discharging of the input filter capacitors, depending on the loading condition. Without proper control, the uneven changing voltage levels of the input capacitors would affect the DC-link voltages generated by the rectification stage, which would have an impact on the ability of the inversion stage to generate proper multilevel outputs, causing output voltage distortion. In order to maintain the input capacitor voltages, the average neutral-point current over a switching period must be maintained at zero. As shown in Table 4.5, the redundant switching states of a SVV connect the same output phase current to the neutral point but with opposite sign. Hence, by equally applying the redundant switching states of a SVV, the i_o can be balanced, keeping the average neutral-point current over a switching period to zero.

Knowing the voltage vectors to be applied to the output, the rectification stage and neutral-point commutator can now be controlled, according to the switching combination in Table 6.2, to supply the required voltage levels to the inversion stage's input terminals, *p_inv* and *n_inv*. For example, switching state *POO* requires the voltage level *P* at the terminal '*p_inv*' and *O* at the terminal '*n_inv*'. Hence, as shown in Table 6.2, switches S_{py} and S_{no} are turned on. For *PNN* the switches S_{py} and S_{ny} are turned on to supply the voltage level *P* to terminal '*p_inv*' and *N* to terminal '*n_inv*'.

6.3.3 Synchronization between the rectification and inversion stages

In order to maintain the balance of the input currents and output voltages within a switching period, the modulation pattern for the indirect three-level sparse matrix converter has to combine the switching states of the rectification stage and inversion stage uniformly. Consider an example where the vector $\overline{I}_{in}$ is located in sector 2 while $\overline{V}_{out}$ is located in *T8* of sector 1. For the rectification stage, the selected current vectors are: I_1 (= I_γ) and I_2 (= I_δ); the voltage vectors selected for the inversion stage are: V_{SV1}

(*POO/ONN*), V_2 (*PNN*) and V_4 (*PPN*). These voltage vectors are applied to the output according to the switching sequence highlighted in Table 6.9.

To ensure the minimum number of switching transitions, the selected voltage vectors for the inversion stage are arranged in a double-sided switching sequence with unequal halves, because each half should be applied to the rectification stage's switching sequence: $I_1 - I_2$. The resulting modulation pattern for the indirect three-level sparse matrix converter is shown in Figure 6.8. The modulation pattern given in Figure 6.8 clearly illustrates how the DC-link voltage levels are applied to the inversion stage's input terminals according to the selected voltage and current vectors within each switching period. The time interval for each voltage vector of the inversion stage's switching sequence can be determined using equations (6.10) – (6.18).

$$t_{r1} = d_{\gamma}^{R} * T_{SW} \tag{6.10}$$

$$t_{i1} = \tfrac{1}{2} * d_{\gamma}^{R} * d_{VSV1} * T_{SW} \tag{6.11}$$

$$t_{i2} = d_{\gamma}^{R} * d_{V4} * T_{SW} \tag{6.12}$$

$$t_{i3} = d_{\gamma}^{R} * d_{V2} * T_{SW} \tag{6.13}$$

$$t_{i4} = \tfrac{1}{2} * d_{\gamma}^{R} * d_{VSV1} * T_{SW} \tag{6.14}$$

$$t_{i5} = \tfrac{1}{2} * d_{\delta}^{R} * d_{VSV1} * T_{SW} \tag{6.15}$$

$$t_{i6} = d_{\delta}^{R} * d_{V2} * T_{SW} \tag{6.16}$$

$$t_{i7} = d_{\delta}^{R} * d_{V4} * T_{SW} \tag{6.17}$$

$$t_{i8} = \tfrac{1}{2} * d_{\delta}^{R} * d_{VSV1} * T_{SW} \tag{6.18}$$

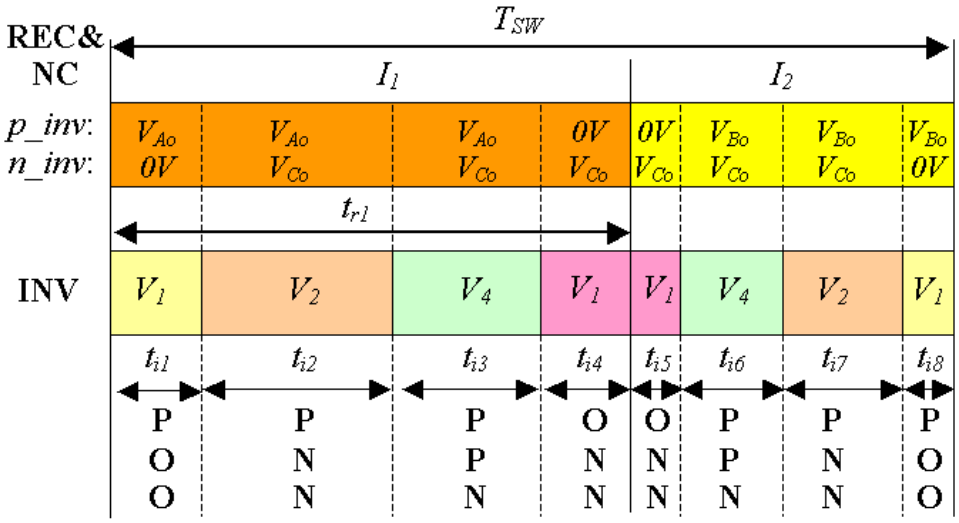


Figure 6.8: The modulation pattern of the indirect three-level sparse matrix converter for the case where the reference vector, $\overline{I}_{in}$, is located in sector 2 while $\overline{V}_{out}$ is located in triangle *T8* of sector 1.

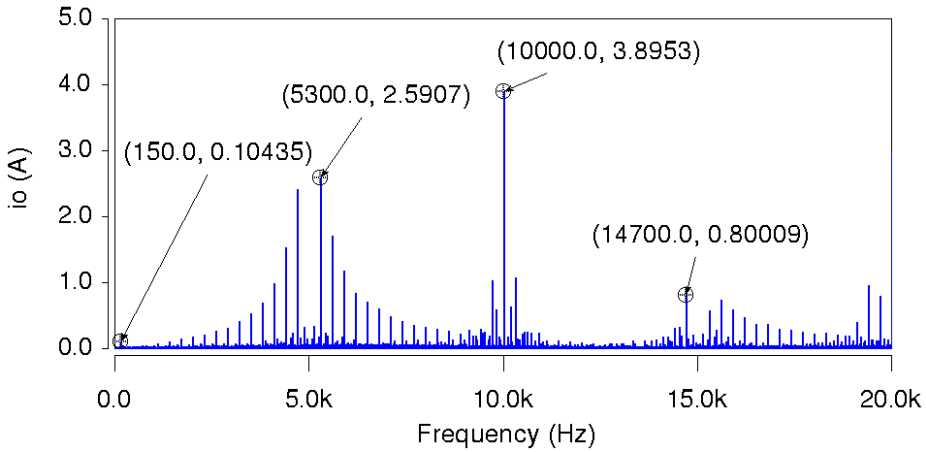
6.4 Simulation results

The indirect three-level sparse matrix converter shown in Figure 6.1 has been simulated using SABER, based on the specifications presented in Appendix A. To analyze the performance of this topology, the indirect three-level sparse matrix converter has been operated at a high modulation index (V_{out_peak} = 270V) and a low modulation index (V_{out_peak} = 135V).

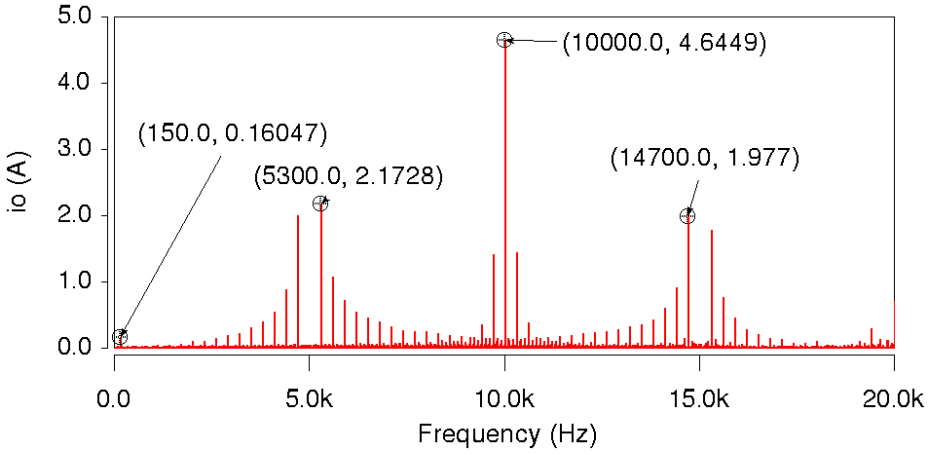
In the same way as in Section 5.5, the effectiveness of the modulation strategy in maintaining the voltage levels of the star-connected input filter capacitors is evaluated first. As discussed in the previous section, the average neutral-point current over a switching period must be maintained at zero in order to keep the voltage levels of the input filter capacitors from changing unevenly. The spectra of the neutral-point current, i_o, at high and low modulation indexes are shown in Figure 6.9. Similar to the three-level-output-stage matrix converter, both spectra of i_o show no significant harmonic current around the fundamental frequency except the third order harmonic of the supply frequency (= 150Hz). The third order harmonic current is $0.1A_{pk}$ at a high modulation index and $0.2A_{pk}$ at a low modulation index. The slightly higher harmonic at low

modulation index is due to the frequent use of small voltage vectors that generate the neutral point current.

Due to this third order harmonic, there is a fluctuation in the neutral-point potential, as shown in Figure 6.10. However, the fluctuations at both modulation indexes are comparatively small ($\pm$5V ≅ 1% of the supply voltages). Hence, as shown in Figure 6.11, the voltage levels of the input filter capacitors referenced to the neutral-point remain balanced. Based on these results, the modulation strategy is shown to be able to compensate for the neutral-point current and maintain the voltage levels of the input filter capacitors. Therefore, the indirect three-level sparse matrix converter can be operated without causing any significant unbalanced DC – link conditions.

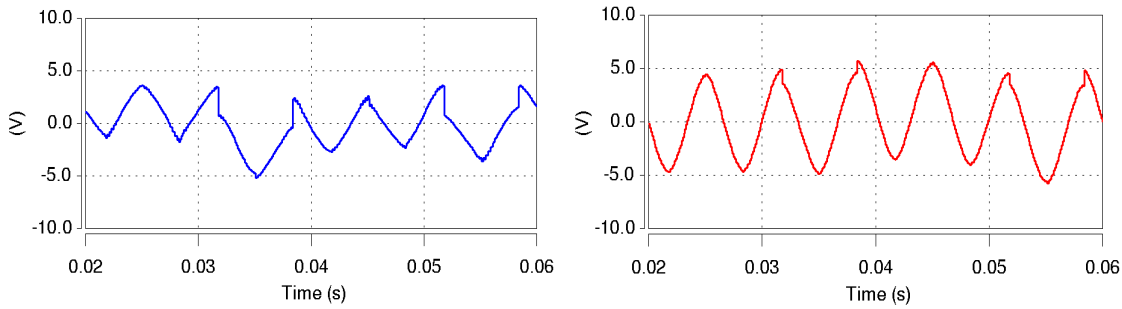


(a) High modulation index



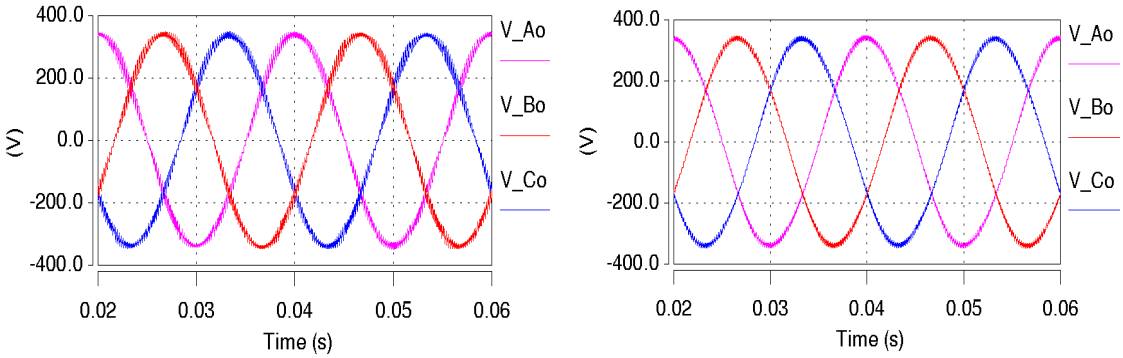
(b) Low modulation index

Figure 6.9: The spectra of the neutral-point current, i_o



(a) High modulation index (b) Low modulation index

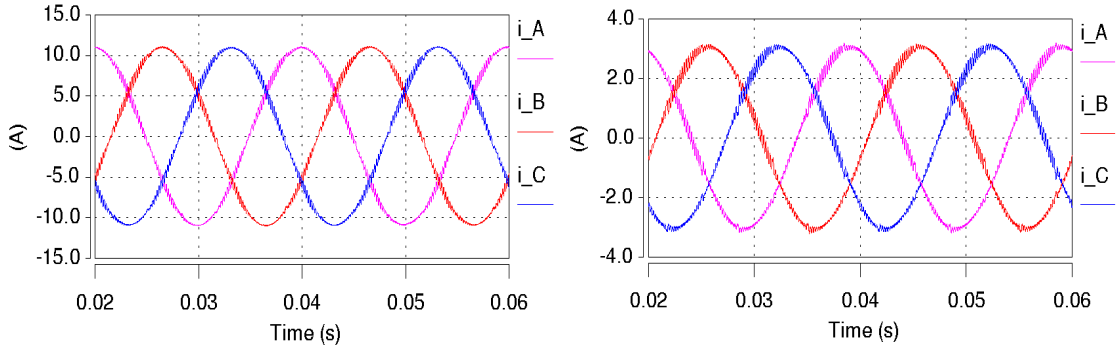
Figure 6.10: The fluctuation in the neutral-point potential



(a) High modulation index (b) Low modulation index

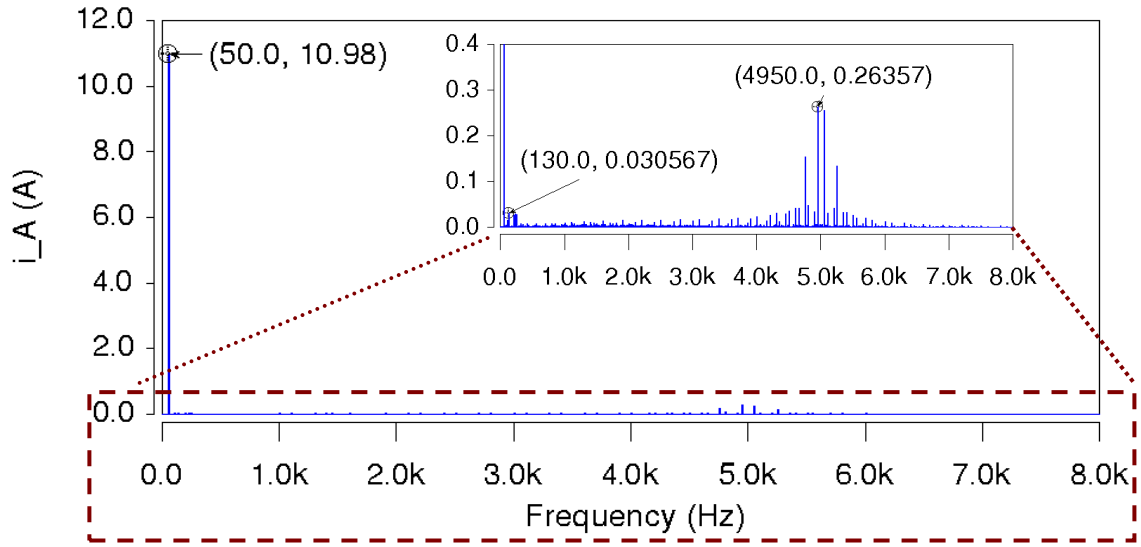
Figure 6.11: The input voltages referenced to the neutral-point

Besides the supply voltages, it is also important to analyse whether i_o affects the input currents, especially at low modulation indexes. The input current waveforms and the spectra of the input current, i_A, are shown in Figures 6.12 and 6.13 respectively. Referring to the input current waveforms, the modulation strategy is able to modulate the indirect three-level sparse matrix converter to generate a set of sinusoidal, balanced input currents. Referring to the spectra shown in Figure 6.13, there are obviously some current ripples around fundamental frequency but the ripples are not of significant magnitude (< 1% of fundamental at both modulation indexes).

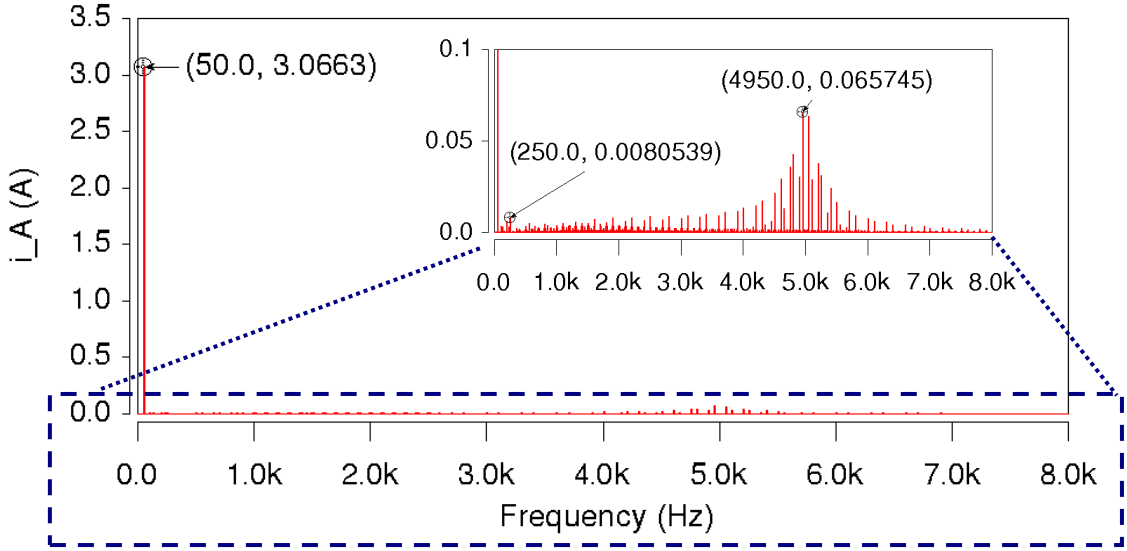


(a) High modulation index (b) Low modulation index

Figure 6.12: The input current waveforms



(a) High modulation index



(b) Low modulation index

Figure 6.13: The spectra of the input current, i_A

Figure 6.14 presents the waveforms generated by the inversion stage of the indirect three-level sparse matrix converter as the voltage transfer ratio is stepped from 0.4 to 0.8. The waveforms shown in this figure consist of the DC-link voltage (V_{pn}); the potentials at the DC – link terminal referenced to the neutral-point (V_{po} and V_{no}); the output terminal voltage (V_{ao}); the output line-to-line voltage (V_{ab}); and the load currents (i_a, i_b and i_c). As discussed in Section 6.3.1, the rectification stage is controlled to provide three voltage levels at the DC-links: V_{po}, 0V and V_{no}. However, at any instant, the inversion stage can only be operated with two voltage levels. Therefore, depending on the selected voltage vectors, the rectification stage and neutral-point commutator provide the required voltage levels to the inversion stage. During the voltage transfer ratio transition, there is a noticeable increase in the DC-link voltage, V_{pn}, as shown in Figure 6.14(a). This is because, to generate higher output voltages at high modulation indexes, the rectification stage and neutral-point commutator constantly connect the input line-to-line voltages (e.g. V_{AB}) to the inversion stage's terminals, '*p_inv*' and '*n_inv*', instead of the input line-to-neutral-point voltages (e.g. V_{Ao}) that are mostly used at low modulation indexes. The switching in V_{po} and V_{no}, shown in Figure 6.14(b), clearly reveal the operations of the rectification stage and neutral-point commutator to control the voltage levels supplied to the inversion stage.

The output terminal voltage, V_{ao}, shown in Figure 6.14(c), clearly shows the ability of the indirect three-level sparse matrix converter to generate three distinctive voltage levels at the output terminals. These levels are the positive and negative envelope of the rectified input voltages and the zero voltage level. Then, as shown in Figure 6.14(d), a transition of the output line-to-line voltage, V_{ab}, from three levels to five levels shows that the indirect three-level sparse matrix converter is able to generate multilevel output voltages. To examine whether the voltage levels are properly applied to generate the desired outputs, the load currents of the indirect three-level sparse matrix converter are shown in Figure 6.14(e). These currents are obviously balanced and sinusoidal.

6.5 Performance evaluation of the indirect three-level sparse matrix converter

To make the indirect three-level sparse matrix converter attractive in industrial applications, this converter must have advantages over the indirect matrix converter and

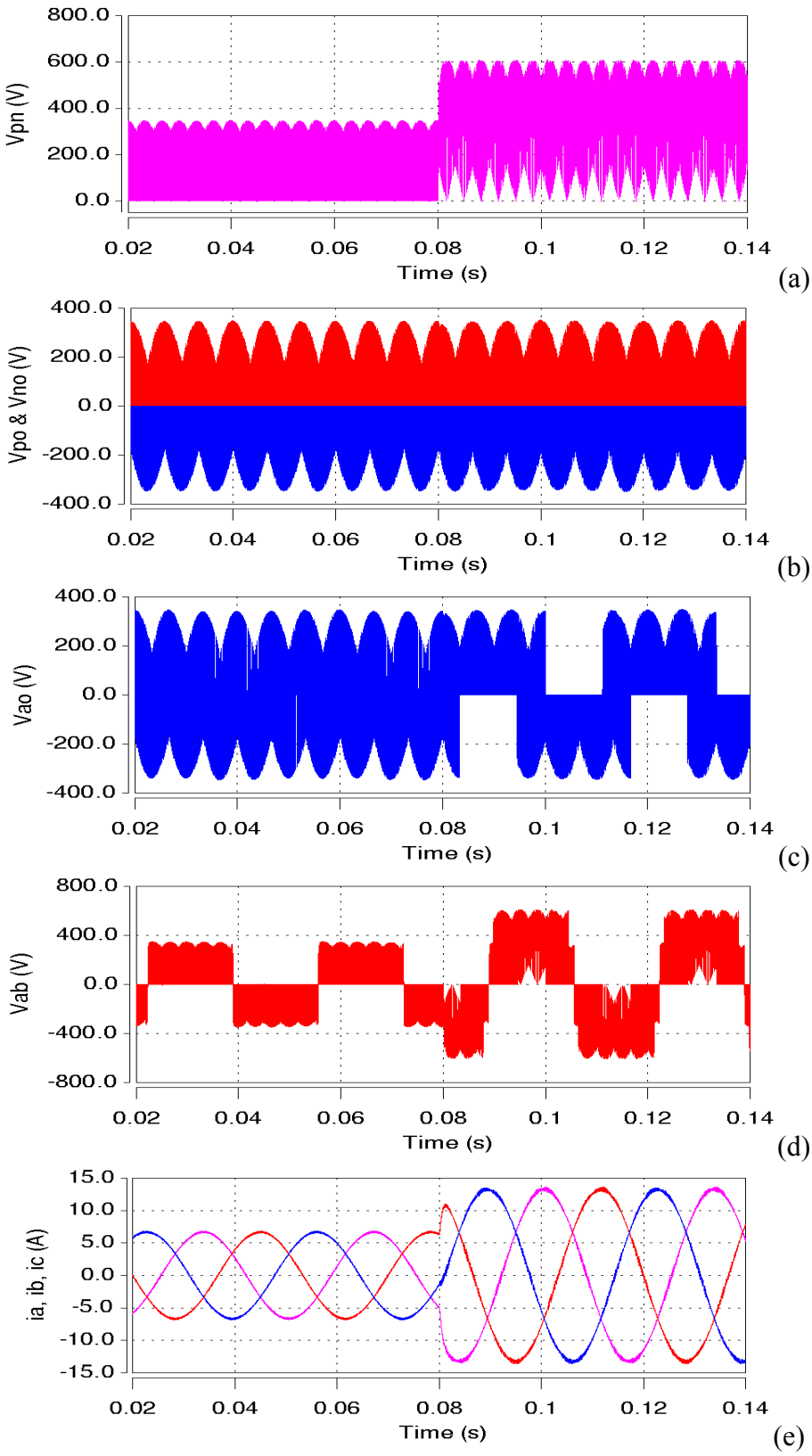


Figure 6.14: The output waveforms generated by the inversion stage of the indirect three-level sparse matrix converter with the voltage transfer ratio stepped from 0.4 to 0.8

the three-level-output-stage matrix converter. Having the ability to generate multilevel output voltages, as shown in Figure 6.14, the indirect three-level sparse matrix converter is obviously able to generate higher quality output waveforms than the indirect matrix converter, which is also modulated using space vector modulation based on the identical specifications. At high modulation indexes, shown in Figure 6.15, the indirect three-level sparse matrix converter evidently generates five distinctive voltage levels for the output line-to-line voltage, V_{ab}. By constructing the output waveforms with multiple voltage levels, the output switching frequency harmonics for the indirect three-level sparse matrix converter are obviously reduced, as shown in Figure 6.15(c). Compared to the indirect matrix converter, the output switching frequency harmonics are reduced from 45V to 30V (f_{sw}) and 104V to 46V ($2f_{sw}$).

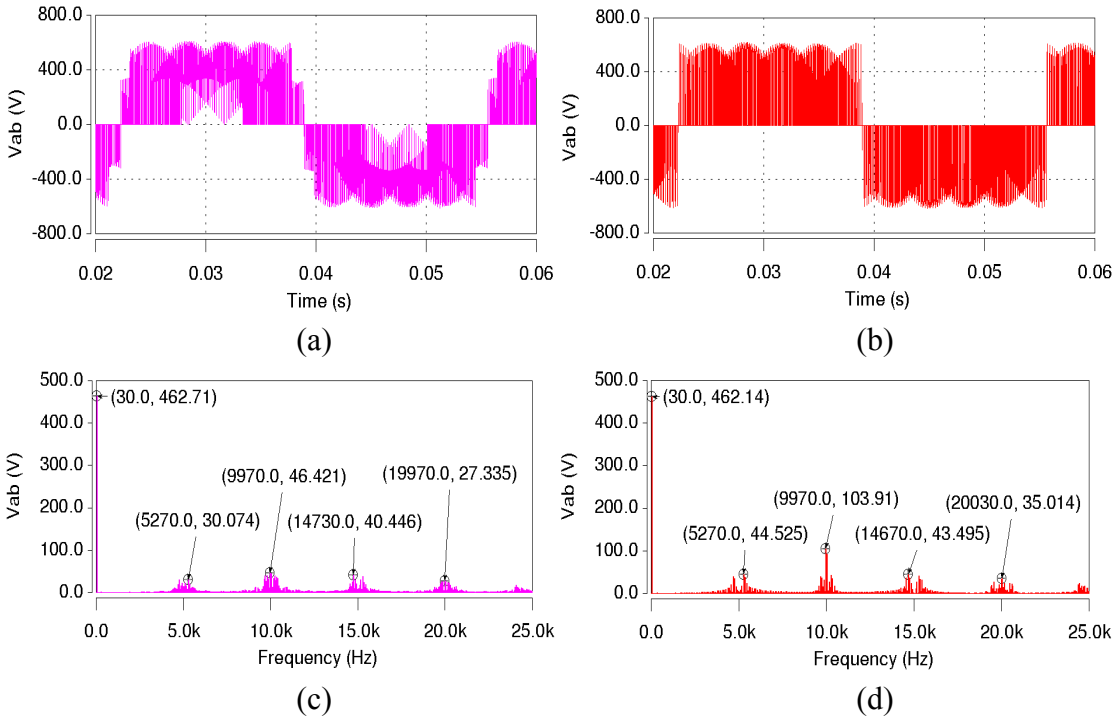


Figure 6.15: Output performance comparison between the indirect three-level sparse matrix converter (left) and the indirect matrix converter (right) at a high modulation index (V_{out_peak} = 270V): (a) (b) output line-to-line voltages (c)(d) output voltage spectra

At low modulation indexes, the indirect three-level sparse matrix converter is able to construct the low output voltage waveforms with smaller voltage levels. As shown in Figure 6.16(a), the magnitude of V_{ab} for the indirect three-level sparse matrix converter is limited to the input phase-to-neutral voltages instead of the line-to-line input voltages for the indirect matrix converter, shown in Figure 6.16(b). As a result, the voltage ripples are lower and the output harmonic content is reduced. By comparing Figure 6.16(c) to Figure 6.16(d), the output switching frequency harmonics for the indirect three-level sparse matrix converter are obviously reduced, from 19V to 10V (f_{sw}) and from 84V to 18V($2f_{sw}$). Based on the results shown in Figures 6.15 and 6.16, the indirect three-level sparse matrix converter is proven to have better output performance than the indirect matrix converter in terms of harmonic content.

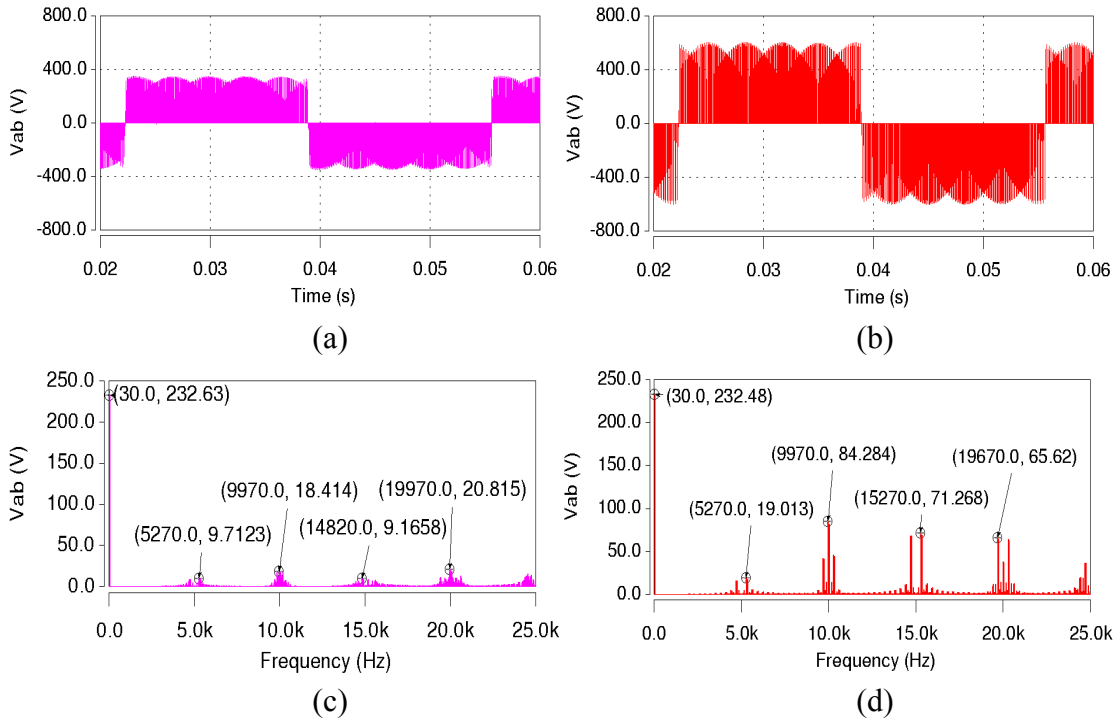


Figure 6.16: Output performance comparison between the indirect three-level sparse matrix converter (left) and the indirect matrix converter (right) at a low modulation index (V_{out_peak} = 135V): (a) (b) output line-to-line voltages (c)(d) output voltage spectra

After proving the indirect three-level sparse matrix converter has the advantage over the indirect matrix converter in terms of output performance, it is interesting to determine how this topology performs compared to the three-level-output-stage matrix converter. Both multilevel matrix converters similarly integrate a three-level neutral-point-clamped converter concept to an indirect matrix converter topology. The only difference is that the indirect three-level sparse matrix converter has simpler circuit configuration, as shown in Figure 6.1, while the three-level-output-stage matrix converter is much complicated but is able to achieve the medium voltage vectors that connect each output terminal to different voltage level. In this comparison, both the multilevel matrix converter topologies are modulated using space vector modulations, discussed in Sections 5.3 and 6.3, respectively. To effectively compare the harmonic contents generated by both topologies, the total harmonic distortion (THD) for the output line-to-line voltage, V_{ab}, of both multilevel matrix converter topologies are calculated and presented in Figure 6.17, where the fundamental output frequency is 30Hz and the number of harmonics included in the THD calculation is 1000 (up to 30kHz). In this figure, the THD for V_{ab} of the indirect matrix converter is also presented.

Referring to Figure 6.17, the three-level matrix converter topologies are shown to have a better output performance than the indirect matrix converter in terms of the harmonic contents in the output waveforms. Comparing the indirect three-level sparse matrix converter to the three-level-output-stage matrix converter, the THD for both multilevel matrix converter topologies are obviously similar at low voltage transfer ratios (< 0.5). This similarity is because the modulation of the inversion stages for both topologies are identical, only the small voltage vectors and zero voltage vectors are used to synthesize the reference output vector. However, at high voltage transfer ratios (>0.5), the ability to achieve the medium voltage vectors enables the three-level-output-stage matrix converter to synthesize the reference output vector with a better selection of the nearest three space vectors, compared to the indirect three-level sparse matrix converter, reducing the harmonic content in the output waveforms. As shown in Figure 6.17, the difference in THD between the multilevel topologies at high voltage transfer ratios is noticeable. The THD for the indirect three-level sparse matrix converter is clearly higher than the three-level-output-stage matrix converter. The decrease in the difference in THD, when the voltage transfer ratio approaches 0.8, is because the large voltage vectors of both multilevel matrix converters get more dominant in synthesizing the

reference output vector. As a result, the THD for both multilevel topologies as well as the indirect matrix converter converge when the voltage transfer ratio reaches 0.8.

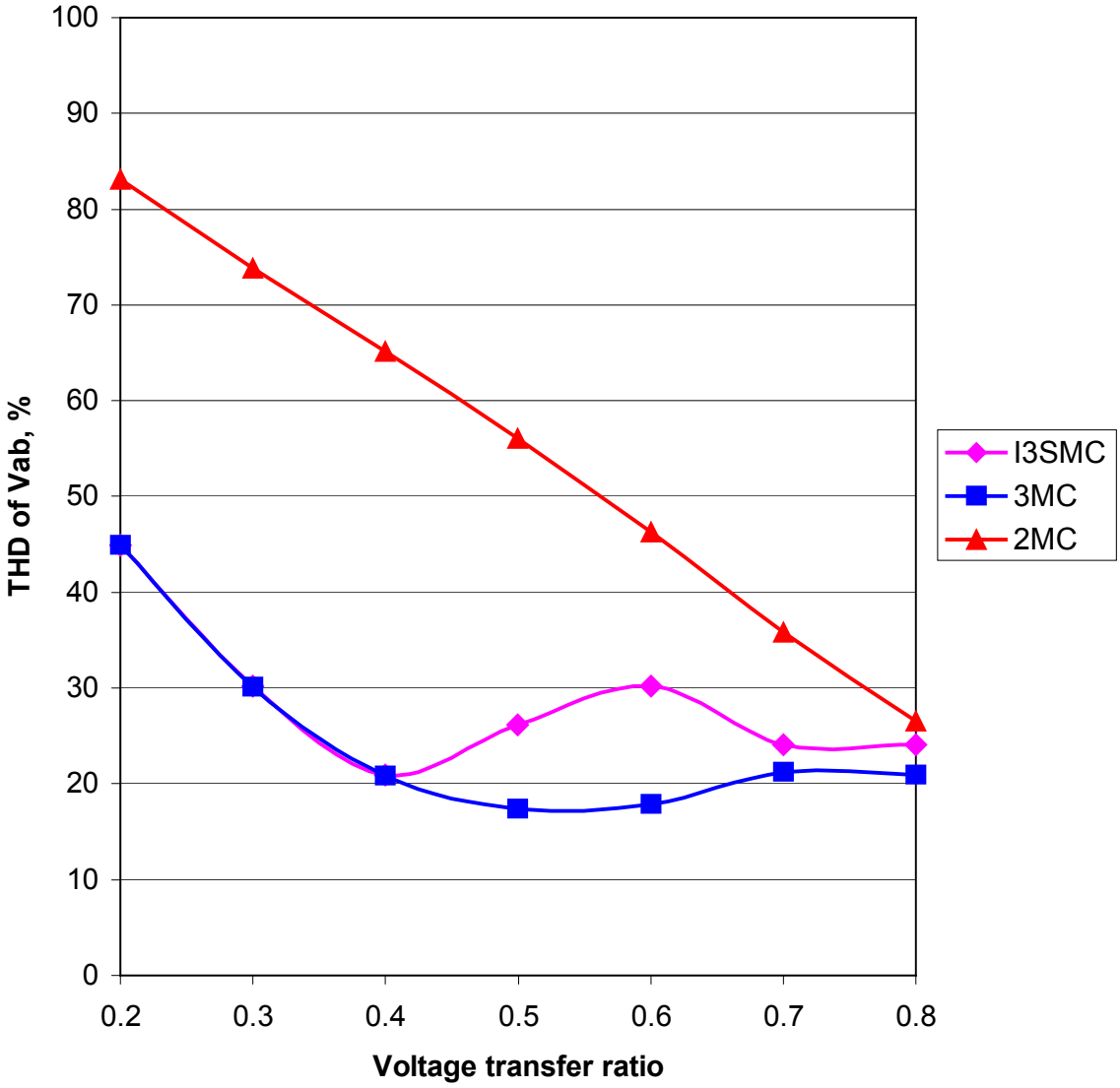


Figure 6.17: The THD for the output line-to-line, V_{ab}, of the indirect three-level sparse matrix converter (pink), the three-level-output-stage matrix converter (blue) and the indirect matrix converter (red).

By having better quality output voltage waveforms in terms of harmonic content, the distortion in the load current for the three-level matrix converters is also reduced, as shown in Figure 6.18. The THD for the load current of the three-level matrix converters is obviously lower than the indirect matrix converter, especially at low voltage transfer ratios (< 0.5). This gives an advantage to the three-level matrix converters when the

load provides low filtering inductances. Besides that, by having lower switching ripple in the load current, the current stress on the semiconductor devices for the converters can be minimized.

Based on Figures 6.17 and 6.18, in terms of output performance, the three-level-output-stage matrix converter is superior to the indirect three-level sparse matrix converter and the indirect matrix converter. However, its complicated circuit configuration is undoubtedly a major drawback. On the other hand, the indirect three-level sparse matrix converter has simpler circuit configuration and is able to generate comparable quality output waveforms to the three-level-output-stage matrix converter, giving the converter the advantage over the three-level-output-stage matrix converter.

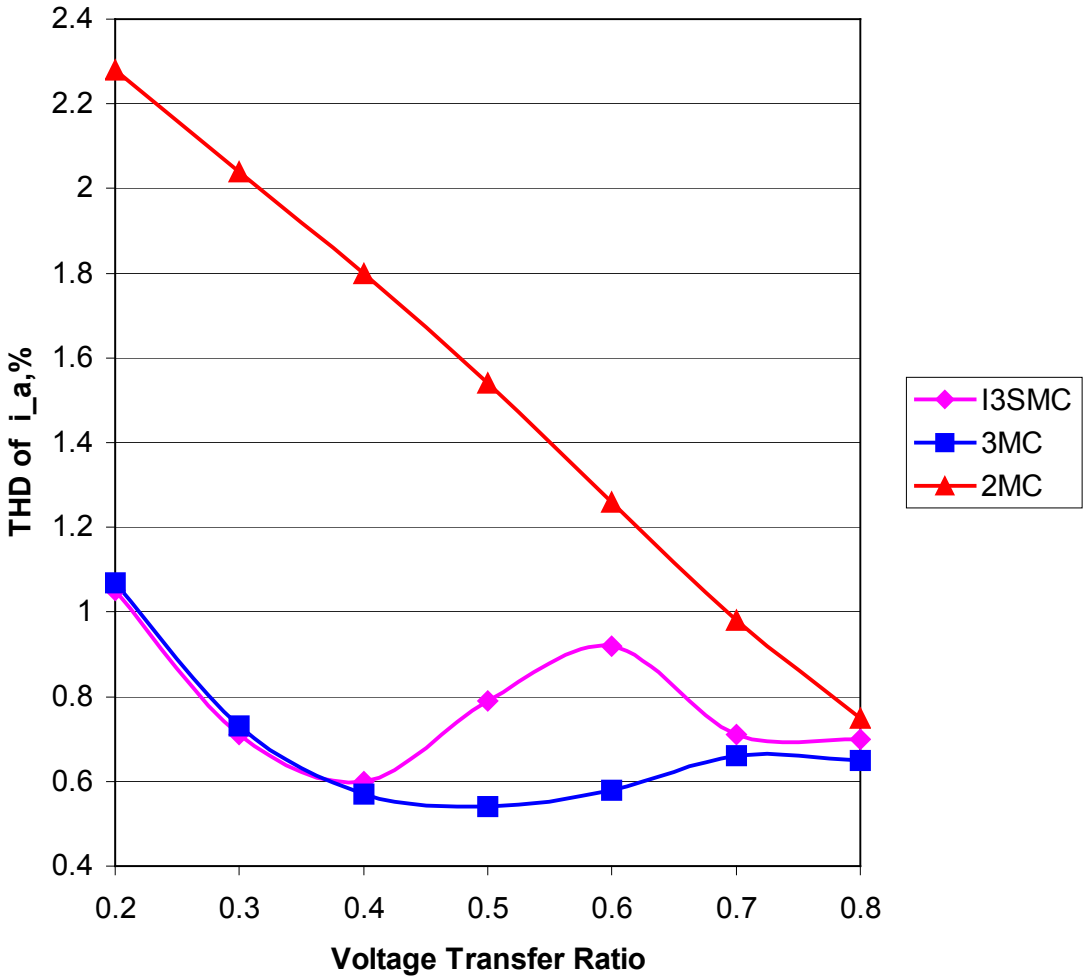


Figure 6.18: The THD for the output current, i_a, of the indirect three-level sparse matrix converter (pink), the three-level-output-stage matrix converter (blue) and the indirect matrix converter (red).

Besides the output performance, the input performance of the indirect three-level sparse matrix converter is also evaluated and compared to the three-level-output-stage matrix converter and indirect matrix converter. As discussed in Section 2.4.3, a low pass LC filter is required to filter out the switching frequency harmonic in the input current of the matrix converter. In this work, the switching frequency of the converter is 5k*Hz* so a low pass LC filter with 2k*Hz* cutoff frequency is used. To investigate whether the amount of filtering is sufficient to meet the required power quality, Figure 6.19 shows the frequency-weighted total harmonic distortion (WTHD) for the unfiltered input current, i_A', of the three-level and indirect matrix converters, where the fundamental input frequency (f_1) is 50*Hz* and the number of harmonics included in the WTHD calculation is 40 (up to 2k*Hz*). The input current WTHD was calculated using equation (6.19) [76]:

$$WTHD = \sqrt{\sum_{n=2}^{n\_\max} \left(\frac{f_1}{f_n}\right)\left(\frac{I(f_n)}{I(f_1)}\right)^2} \tag{6.19}$$

As shown in Figure 6.19, the harmonic distortions in the i_A' of the three-level converters are higher than the indirect matrix converter, especially at low voltage transfer ratios. This is due to the discontinuity in the DC-link current when the three-level matrix converters generate the small and zero voltage vectors. As discussed in Section 2.3.2.1, the rectification stage is modulated based on the assumption that the DC-link current is constant and continuous. However, when the small voltage vector (e.g. *ONN*) or the zero voltage vector (e.g. *PPP*) is applied, there is no current flowing through one (e.g. DC-link '*p*') or both of the DC-links, which inevitably affects the ability of the rectification stage to properly synthesize the input currents. Referring to Figure 6.19, the distortion in the input current for the three-level matrix converters obviously increases when the voltage transfer ratio gets lower. This is because the small and zero voltage vectors get more dominant in synthesizing the reference output voltage vector.

Nevertheless, the harmonic distortion in the unfiltered input current for the three-level matrix converters is relatively low (< 1%). This result evidently shows that the low pass filter with 2kHz cutoff frequency is sufficient for this application. Therefore, a set of sinusoidal and balanced input currents, as shown in Figures 5.12 and 6.12 respectively, can be generated at the supply side of the three-level matrix converters.

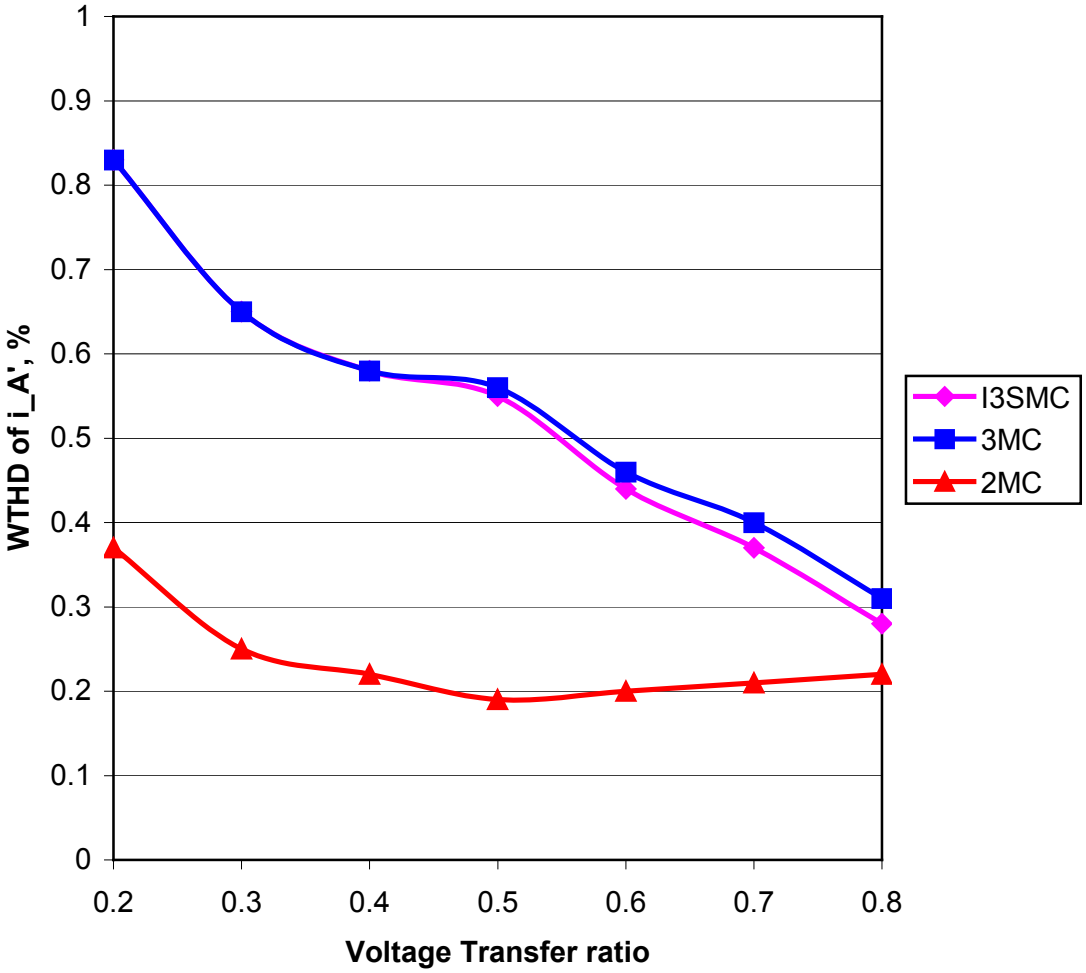


Figure 6.19: The WTHD for the unfiltered input current, i_A', of the indirect three-level sparse matrix converter (pink), the three-level-output-stage matrix converter (blue) and the indirect matrix converter (red).

6.6 Conclusions

In this chapter, an explanation about the operating principles and space vector modulation for the indirect three-level sparse matrix converter has been given. Issues related to the neutral-point balancing problem and the unequal DC-link voltages, as well as associated control methods, have been discussed. Even though having simpler circuit configuration, the indirect three-level sparse matrix converter is proven able to generate multilevel output voltages: three distinctive levels for the output terminal voltages and five levels for the output line-to-line voltages. In addition, the indirect three-level sparse matrix converter is able to generate a set of sinusoidal and balanced input currents, although the presence of the neutral-point current.

The output performance comparisons between the indirect three-level sparse matrix converter and indirect matrix converter clearly show that the indirect three-level sparse matrix converter is able to generate higher quality outputs in terms of harmonic contents. Compared to the three-level-output-stage matrix converter, the output performances for both multilevel topologies are comparable. As a result, in terms of circuit configuration, the indirect three-level sparse matrix converter definitely has the advantage over the three-level-output-stage matrix converter.

Chapter 7

Converter Implementation and Experimental Results

7.1 Introduction

After evaluating the performance of the three-level matrix converter topologies using SABER, it is essential to experimentally validate the simulation results using a prototype converter at realistic power levels. This chapter presents the hardware implementation as well as the experimental results from the three-level matrix converter topologies. To begin with, the overall structures of the converter prototypes are described. Then, the design of each circuit is explained in detail. Finally, the experimental results of the prototypes, which were tested at different modulation indexes, are analyzed. By showing that the experimental results correspond well to the simulations, the three-level matrix converters can be verified to have better output performance than the indirect matrix converter in terms of harmonic content in the output waveforms.

7.2 Hardware implementation

7.2.1 Overall structure of the prototype converter

To validate the simulation results, prototypes of the indirect three-level sparse matrix converter and three-level-output-stage matrix converter were built. As shown in Figure 7.1, the overall structure of the prototypes consists of five parts: the control platform, the measurement circuits, the gate drives, the power circuits and the protection circuits.

The control platform comprises of a digital signal processor (DSP) board and a field programmable gate array (FPGA) board. The DSP is the central processing unit that performs all modulation calculations and control functions. The interface between the

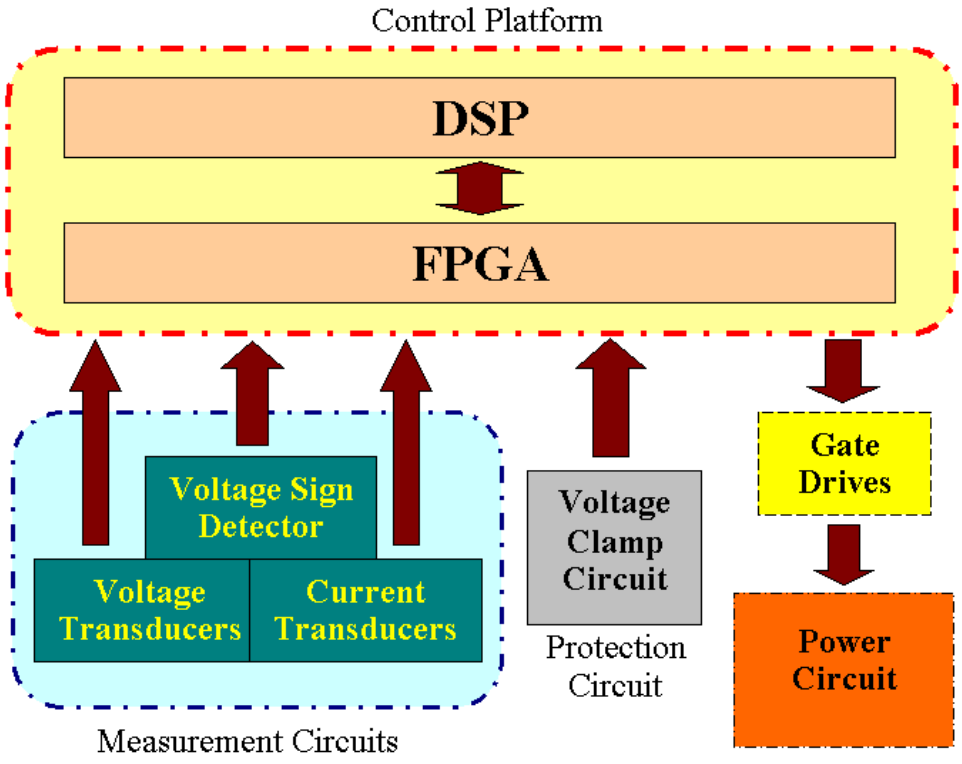


Figure 7.1: The overall structure of the converter prototypes

DSP and other circuits is the FPGA board; this board handles the following tasks:

- Receiving data from the measurement circuits and performing analogue – to – digital (A/D) conversion.
- Sends the switching signals to the gate drives, according to the modulation demands from the DSP.
- Protecting the power circuit by turning off all switching devices when the protection circuit signals an over-voltage or over-current condition.
- Performing the four-step and dead-time current commutation procedures.

The measurement circuits provide the input data required by the control platform to perform the converter modulation. The magnitudes of the input phase voltages are needed in the modulation strategy to determine the duty cycles for the switching devices

and are measured using voltage transducers. To commutate current between the bi-directional switches in the rectification stage, the relative input voltage magnitude based commutation technique is applied. Voltage sign detection circuits are used to compare the relative magnitudes of the input voltages and provide an input for the control platform to enable the correct commutation sequence.

Based on the measured input voltages, the control platform performs necessary calculations and then sends out the switching signals to the gate drives. The gate drives provide electrical isolation between the control platform and the power circuit. Using the gate drives, the control platform is able to drive the high voltage switching devices using low voltage control signals.

The prototype power circuits have been built for the three-level matrix converter topologies discussed in Chapters 5 and 6. The input filters and loads (resistor plus inductor) are connected to the input and output terminals of the power circuit, respectively. The protection circuit is a clamp circuit that provides over-voltage protection for the power circuit. To ensure the power circuit does not operate at over the maximum current level, the control platform monitors the load currents by using current transducers, providing additional protection for the prototype.

7.2.2 Control Platform

As shown in Figure 7.1, the control platform consists of a DSP board and a FPGA board. For this prototype, the TMS320C6713 DSP is used as the central processing unit. Operating at 225MHz, the TMS320C6713 DSP is able to perform a million operations and instructions per second, offering sufficient processing capability required for this application. To interface the DSP with other circuits, a FPGA board powered by the ProAsic A500K050 FPGA chip (manufactured by Actel), shown in Figure 7.2, is used. This FPGA board has been designed and developed by the University of Nottingham to control matrix converters for aerospace applications [72]. Due to the flexible design of this FPGA board, the FPGA control software can be easily modified to control other power converter topologies.

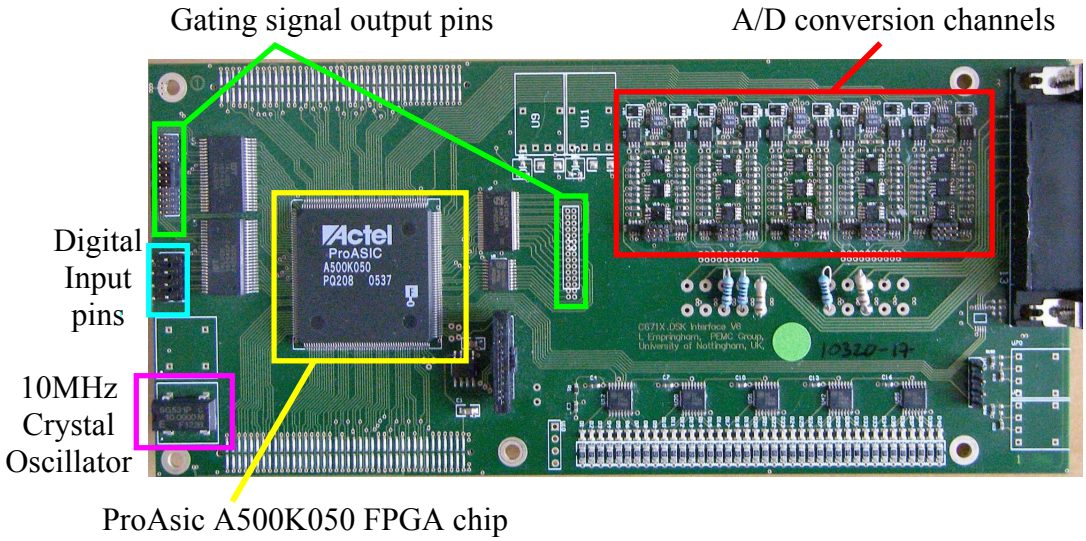


Figure 7.2: The FPGA board used for this prototype

In order to gather sufficient data for effective modulation and protection, the FPGA board provides 10 channels for A/D conversions and 11 channels for digital inputs. Figure 7.3 shows the measured variables connected to the FPGA board in this prototype. Operated with a clock frequency of 10 MHz, the FPGA continuously retrieves data from the 12-bit A/D conversion channels and digital input channels, then passes the information to the DSP for processing. By interpreting control signals from the DSP, the FPGA determines the sequence of the switching signals to be transmitted to the gate drives through the output pins.

To safely commutate current between the switching devices of the converter, the FPGA is programmed to perform associated commutation procedures: the relative input voltage magnitude based commutation strategy for the bi-directional switches (rectification stage) and the dead-time commutation strategy for the unidirectional switches (inversion stage). The concept of these commutation strategies has been explained in Section 2.4.2. By using the VHDL (Very-high-speed integrated circuit Hardware Description Language) and logic gates, the state machines for both commutation strategies can be programmed into the FPGA. For the indirect three-level sparse matrix converter, an additional three-step relative voltage magnitude based commutation strategy, which was proposed by Author in [71], is required to ensure the

safe commutations between the bi-directional switches in the rectification stage and the unidirectional switches in the neutral point commutator.

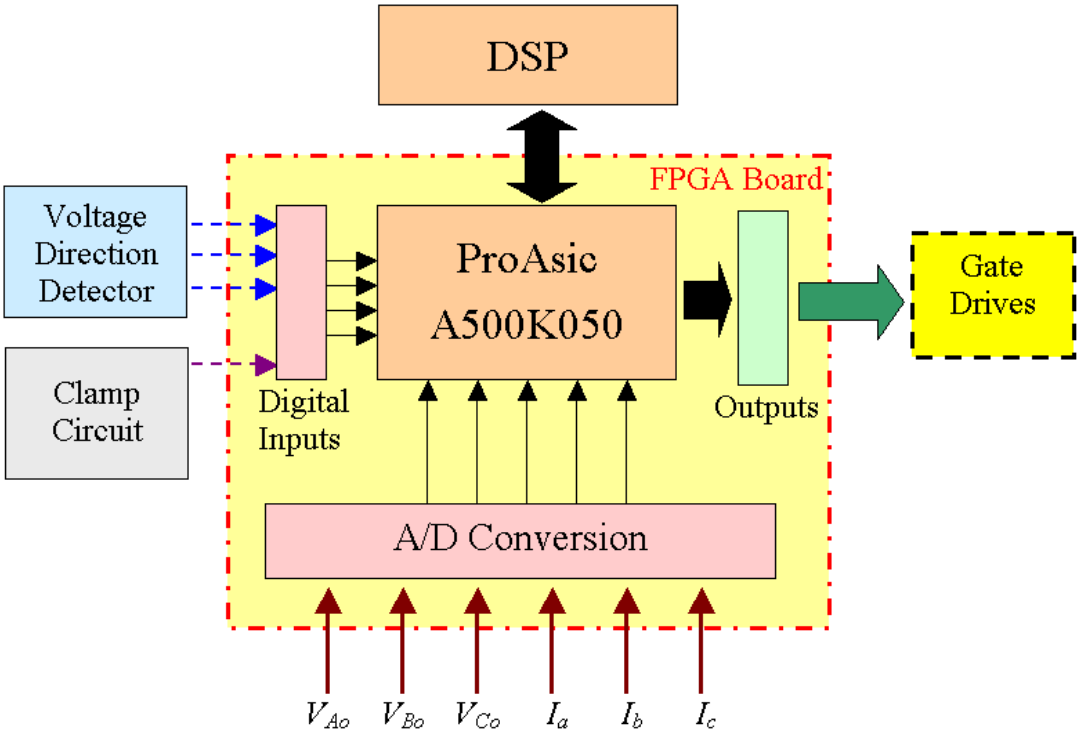


Figure 7.3: The inputs and outputs of the FPGA board

7.2.2.1 The three-step relative voltage magnitude based commutation strategy

Similar to the four-step relative input voltage magnitude based commutation technique, the concept of this strategy is to form a freewheeling path in each switch cell involved in commutation based on the relative magnitudes of the input voltages. The schematic diagram for the upper DC-link of the rectification stage and the neutral point commutator, shown in Figure 7.4, is used to explain the principle of this commutation strategy. V_{in_p} is the input phase voltage (V_{Ao}, V_{Bo} or V_{Co}) applied to the DC-link point '*p*'; V_o is the neutral-point voltage at the DC-link middle point '*o*'; and V_{p_inv} is the voltage applied to the inversion stage's terminal '*p_inv*'. Under steady state condition, the bi-directional switch cell (Cell A) of the rectification stage are initially turned 'on' so $V_{p\_inv} = V_{in\_p}$. When a commutation to the neutral-point commutator (Cell B) is

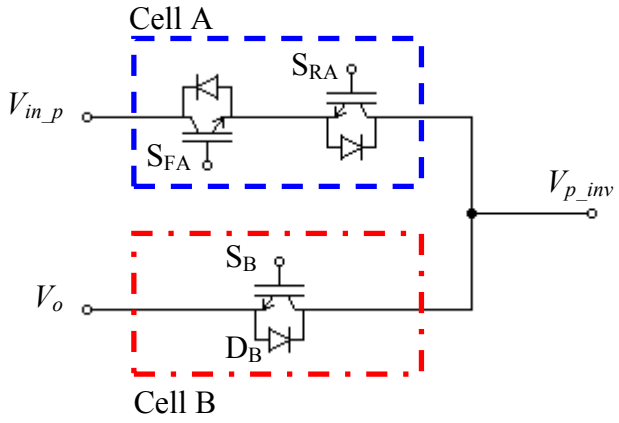
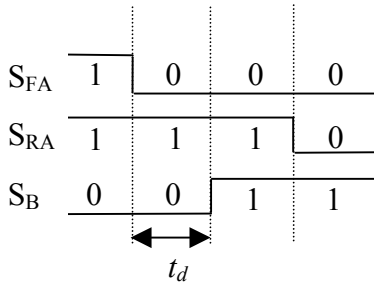


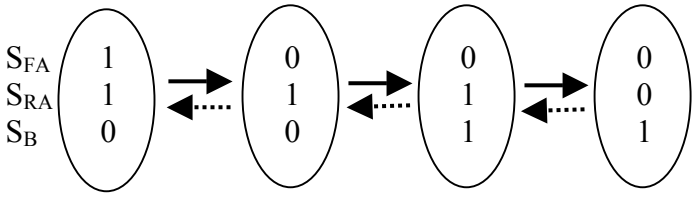
Figure 7.4: The schematic diagram for the upper DC-link of the rectification stage (Cell A) and the neutral-point commutator (Cell B).

required, the relative magnitudes of the input voltages applied to the switches are determined. For the upper DC-link of the indirect three-level sparse matrix converter, V_{in_p} is always larger than V_o because the rectification stage is modulated to supply only the positive voltage level to the DC-link point '*p*'.

Since V_{in_p} is larger than V_o, switch S_{RA} and diode D_B are the freewheeling devices in Cells A and B, respectively. With the freewheeling paths available in both cells, the commutation sequence begins by turning off the non-freewheeling switch, S_{FA}, in the outgoing cell, Cell A. Then the non-freewheeling device, S_B, of the incoming cell, Cell B, is turned on. Finally, to complete the commutation process, the freewheeling device, S_{Aa2}, is gated off. As shown in Figure 7.5(a), a time gap, t_d, is required between each switching state change. By completing the commutation sequence, V_o is now connected to the terminal '*p_inv*' so $V_{p\_inv} = V_o$. The state diagram for this commutation sequence is shown in Figure 7.5(b). Similarly, the three – step commutation strategy is applied to the lower DC-link of the rectification stage and neutral-point commutator but with slight modification because V_{in_n} is now smaller than V_o. Figure 7.6 shows the schematic diagram for the lower DC-link while Figure 7.7 shows the state diagram of the commutation sequence for the lower DC-link.



(a) Timing diagram



(b) States diagram

Figure 7.5: The three-step relative magnitude voltage based commutation strategy for the upper DC-link of the indirect three-level sparse matrix converter

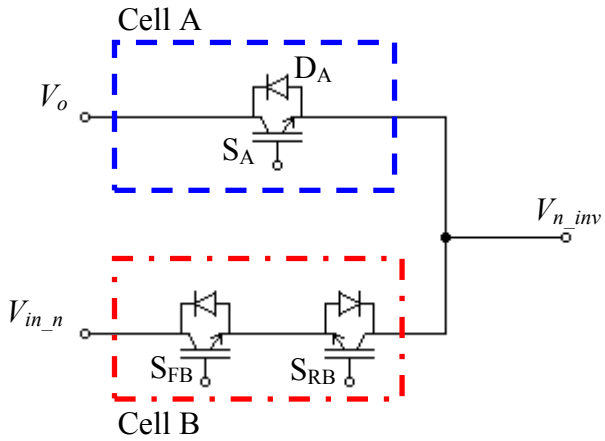


Figure 7.6: The schematic diagram for the lower DC-link of the rectification stage (Cell A) and the neutral-point commutator (Cell B).

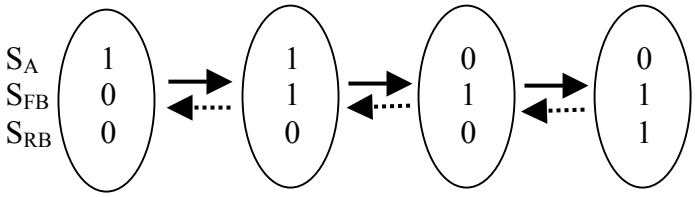


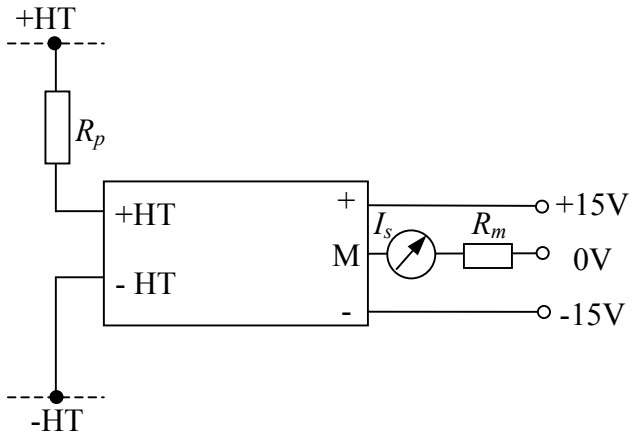
Figure 7.7: The states diagram of the three-step commutation strategy for the lower DC-link of the indirect three-level sparse matrix converter.

7.2.3 Measurement circuits

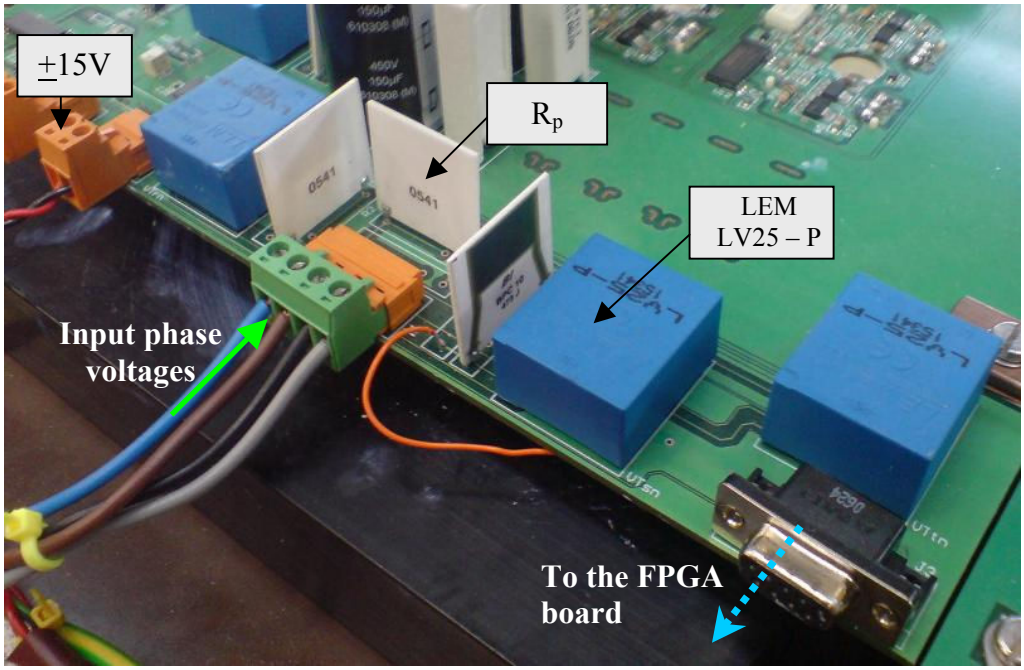
As shown in Figure 7.1, the measurement circuits comprise of voltage transducers, current transducers and the voltage direction detection circuits. According to the modulation strategy, the input currents generated by the three-level matrix converter topologies are synchronized with the input voltages. As a result, the magnitude of the input phase voltages referenced to the neutral-point of the input filters (V_{Ao}, V_{Bo} and V_{Co}) are required to determine the reference angle of the input current vector as well as the duty cycles for the switching devices. To measure the input phase voltages, transducers, LEM LV25-P, are used.

The schematic diagram of the voltage measurement circuit for this prototype is shown in Figure 7.8(a). The nominal primary voltage of the voltage transducer is set as 250V(rms). A primary resistor, R_p, is used to generate a primary current linearly proportional to the measured voltage. In order to achieve a 10mA(rms) primary nominal current for the voltage transducer, a 25kΩ R_p was selected. Based on the primary current, the voltage transducer uses the Hall Effect to generate a secondary current, I_s, with the conversion ratio of 2500:1000. A measurement resistor (R_m) is then used to generate an isolated output voltage signal, proportional to I_s, for the FPGA. Knowing that the secondary nominal current is 25mA(rms), a 200Ω R_m is used because each A/D conversion channel expects an input signal within the range of $\pm$5V. Figure 7.8(b) shows a picture of the voltage measurement circuit board that was built for this prototype. The measurement resistors were soldered on the FPGA board, which can be seen below the A/D converters in Figure 7.2.

To ensure the prototype converter does not operate at over the maximum current level, the control platform has to continuously monitor the load currents (i_a, i_b and i_c) using three current transducers, LEM LAH-25NPs. The connection of the current transducer for this prototype is shown in Figure 7.9. The current transducer uses the Hall Effect to generate a secondary current, I_s, with the conversion ratio 1:1000 to the primary current. Knowing that the secondary nominal current for the current transducer is 25mA(rms), a 200Ω R_m is used to generate a voltage signal, which is within the range of $\pm$5V, for the A/D conversion channel on the FPGA board.



(a) The schematic diagram



(b) The circuit board

Figure 7.8: The voltage measurement circuit

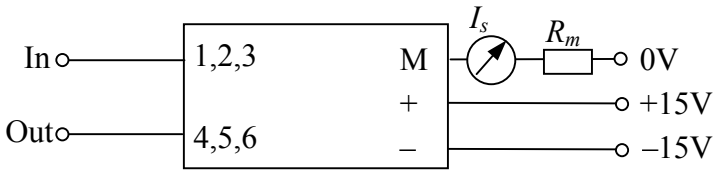


Figure 7.9: The connection of the current transducer

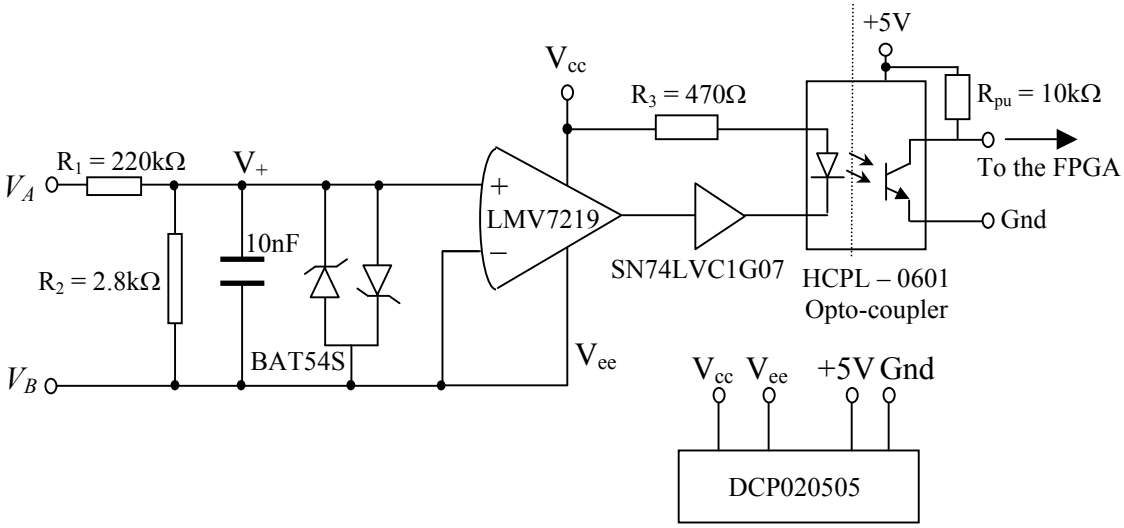
In order to apply the relative input voltage magnitude based commutation strategy to the rectification stage, three voltage direction detection circuits were built to determine the signs of the input line-to-line voltages applied to the bi-directional switches. The schematic diagram of a voltage direction detection circuit for this prototype is shown in Figure 7.10(a).

As shown in Figure 7.10(a), the potential divider (R_1 and R_2) generates an output voltage (V_+) that is a fraction of the input voltage for the comparator. For this case the input voltage is V_{AB}. By using the back-to-back schottky diodes, V_+ is limited to $\pm$0.7V and is used as a non-inverting input for the comparator. This non-inverting input is compared with the inverting input, which is connected to the common 'ground' (V_B), to determine the voltage direction. For the case where $V_A > V_B$, the comparator generates a high logic signal. A capacitor is connected across the inputs of the comparator to filter out the high frequency jittering that occurs at the zero crossing of the current.

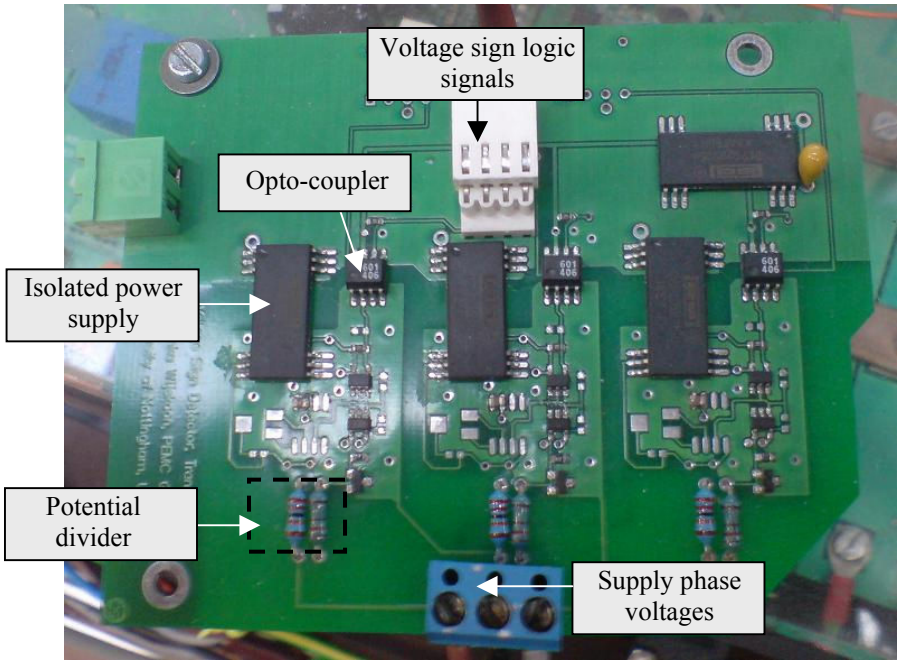
Due to the use of an input phase voltage as reference (ground) for the voltage direction detection circuit, an isolated power supply (DCP020505) is needed to supply the circuit. An opto-coupler is also needed to provide the electrical isolation between the high input voltages and the control platform. A buffer, SN74LVC1G07, is used to drive the opto-coupler in order to generate the logic signal for the FPGA according to the comparator's output state. Figure 7.10(b) shows the voltage direction detection circuits built for this prototype.

7.2.4 Gate drive circuits

Gate signal is required for every power semiconductor controlled device to drive it into turn-on or turn-off operation. The gate drive circuit requirement for each device varies, depending on the type of device and its voltage and current rating. For this prototype, the IGBT switching devices are used to construct the three-level matrix converter topologies. Similar to MOSFET, the IGBT is a voltage-controlled switching device that requires very small current during the switching period so it has simple gate-drive requirements. Nevertheless, due to the internal capacitances of the IGBT, the gate drive circuit must have the source and sink capabilities in order to charge and discharge the internal capacitances during the switching operations.



(a) Schematic circuit



(b) Circuit board

Figure 7.10: The voltage direction detection circuit

To construct the prototype three-level matrix converters, the rectification stage and inversion stage both require switch cells: the common-emitter bi-directional switch cell for the rectification stage and the unidirectional switch for the inversion stage. Hence, two types of gate drive circuit are required, as discussed in the following section.

7.2.4.1 The bi-directional switch cell

The schematic diagram of the gate drive circuit for a bi-directional switch cell of the rectification stage is shown in Figure 7.11. To control a bi-directional switch cell constructed with two IGBTs, the control platform is required to send two gating signals. Due to the high voltage operating range of the switch cell, a dual-channel opto-coupler (HCPL – 315J) is essential to provide the electrical isolation between the control platform and the high voltage output stage. An isolated power supply (DCP020515) is used to supply voltage to the gate drive circuit. As shown in Figure 7.11, a buffer chipset (SN74LVC1G07) is used for each input channel of the opto-coupler. By connecting a 470Ω pull-up resistor between the 5V supply voltage and the buffer output pin, the open-drain buffer is able to drive the opto-coupler to generate signal for the gate drive circuit according to the FPGA gate signal.

As mentioned earlier, the four – step commutation strategy is used to commutate current between the bi-directional switches. Based on the turn-on and turn-off time of the switching devices, a suitable time gap is introduced between each switch state change. However, if the time gap is too long, the total required switching time to complete the commutation sequence would be increased, affecting the effectiveness of the modulation in controlling the converter output waveforms. To overcome this problem, the turn-on and turn-off time of the IGBT have to be reduced so that the shorter possible time gap is used. For this gate drive circuit, two methods have been applied to reduce the turn-on and turn-off time of the IGBT: the complementary emitter followers Q1 and Q2 (push – pull configuration) are applied to enhance the source and sink capabilities of the gate drive circuit and the bipolar signals (+15V and –15V) are used to gate the IGBTs. Figure 7.12 shows the gate drive circuit for a bi-directional switch cell.

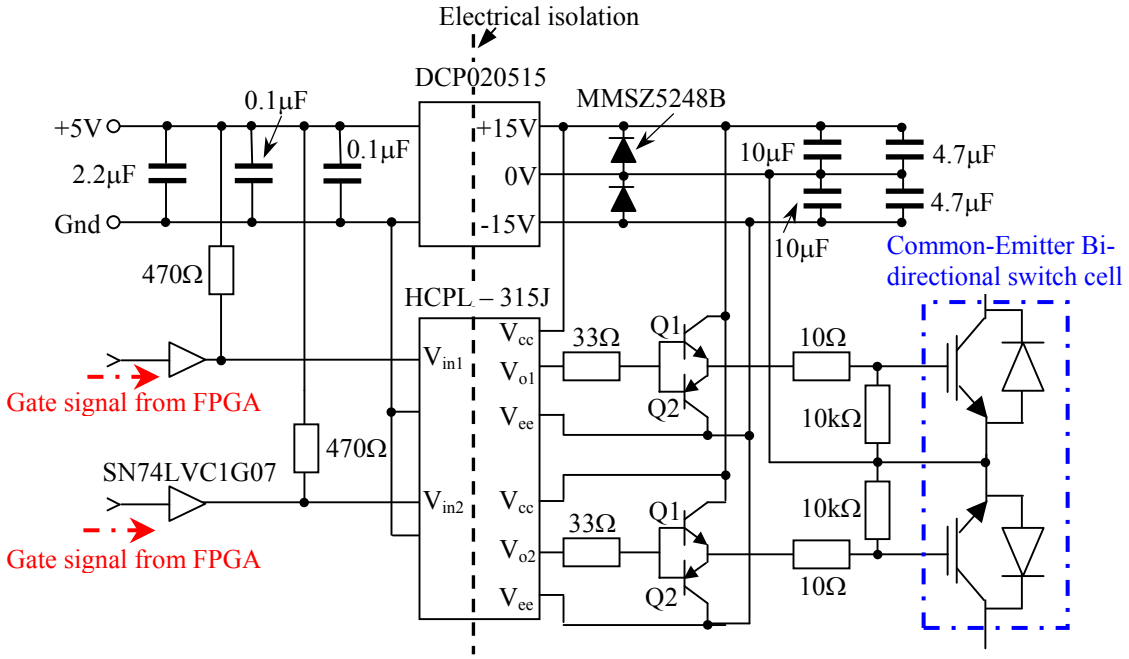


Figure 7.11: The schematic diagram of the gate drive circuit for a bi-directional switch cell in the rectification stage.

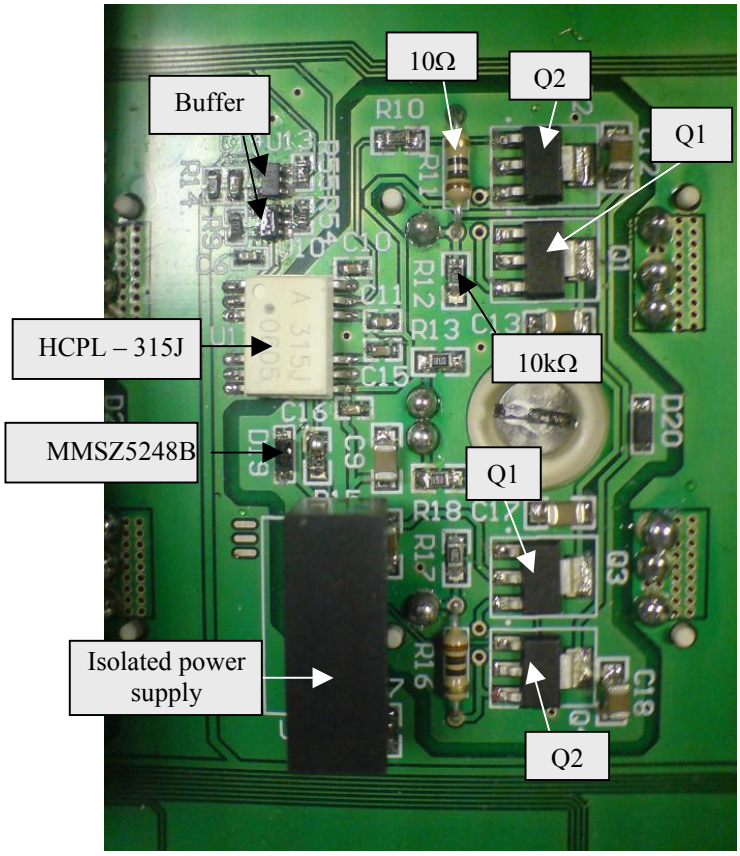


Figure 7.12: The gate drive circuit for a bi-directional switch cell in the rectification stage.

7.2.4.2 The unidirectional switch

A diagram of the gate drive circuit for a unidirectional switch of the inversion stage is shown in Figure 7.13. An opto-coupler (HCPL – 312) and an isolated power supply (DCP020515) are required. Compared to Figure 7.11, the gate drive circuit for the unidirectional switch cell is simpler because only one gating signal is required. Due to the presence of natural freewheeling path (anti-parallel connected diode) for each IGBT, a simple dead-time current commutation strategy can be used for the unidirectional switches of the inversion stage. The use of a short time gap for only one switch state change in the commutation sequence should not greatly affect the modulation on the converter in most applications.

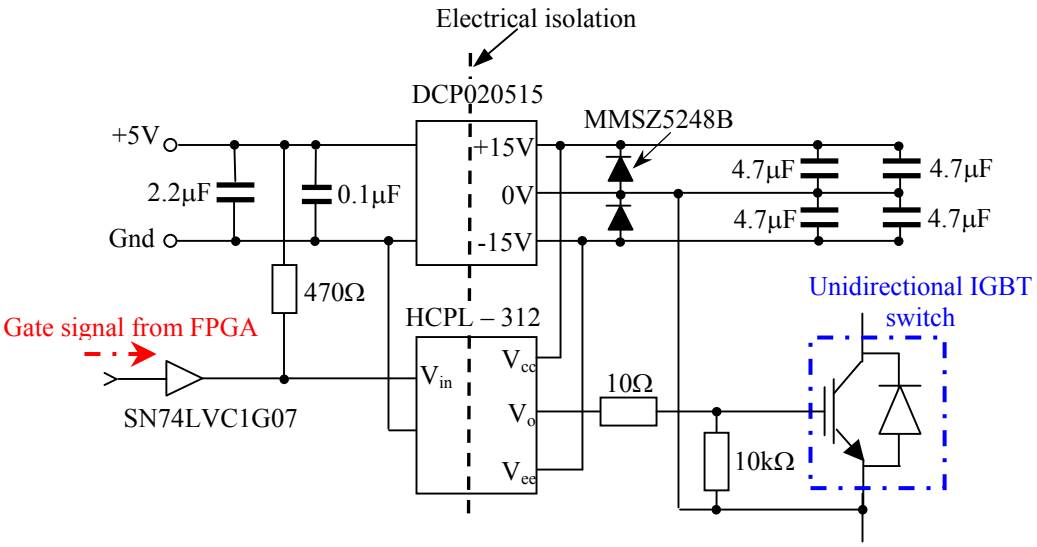


Figure 7.13: The gate drive circuit for the unidirectional IGBT switches in the inversion stage.

7.2.5 The power and protection circuits

The power circuits considered in this section are the three-level matrix converter topologies that were discussed in Chapters 5 and 6. For this experimental work, a 5kW converter prototype was built for each three-level matrix converter topology. As discussed in Chapters 5 and 6, each three-level matrix converter topology consists of a rectification stage and an inversion stage, where the circuit configuration for the rectification stage is the same for both topologies. To be cost and time efficient, only one rectification stage was built and shared by the inversion stages of both topologies.

To construct a three-phase to two-phase matrix converter as the rectification stage for the three-level matrix converter topologies, six SK60GM123 IGBT modules (60A/1200V), manufactured by SEMIKRON, are used. Each IGBT module is a common-emitter bi-directional switch cell, as discussed in Section 2.4.1. The IGBT modules were soldered on a custom-designed six-layer printed circuit board (PCB), where the input (three-phase voltage supply) and output terminals (DC-link points: *p*, *o* and *n*) of the rectifier are placed on either side of the PCB, as shown in Figure 7.14. The top layer of this multi-layer PCB is the signal plane that consists of the gate drive circuits, the gate signal tracks and the DC voltage supply tracks. Each gate drive circuit is built close to its respective IGBT module to ensure smooth commutation process and reduce any parasitic effects. The input filter capacitors are connected close to the input terminals on the PCB in order to reduce the stray inductance in the device conductive loops.

To connect the IGBT modules to the input and output terminals, the three inner layers of the PCB are used as the power planes. Each power plane provides the power rails that depict the input voltage connections, the neutral-point track (*o*), the positive (*p*) and negative (*n*) DC-links. The neutral-point plane provides a connection from the DC-link middle point '*o*' to the neutral-point of the star-connected input filter capacitors. By using the power planes the connection inductance to the IGBT modules is minimized. The first inner layer closest to the top layer is used as a ground plane so that radiated noises from the signal tracks and power planes is mainly confined within the substrate between the planes and the ground plane instead of being coupled to one another.

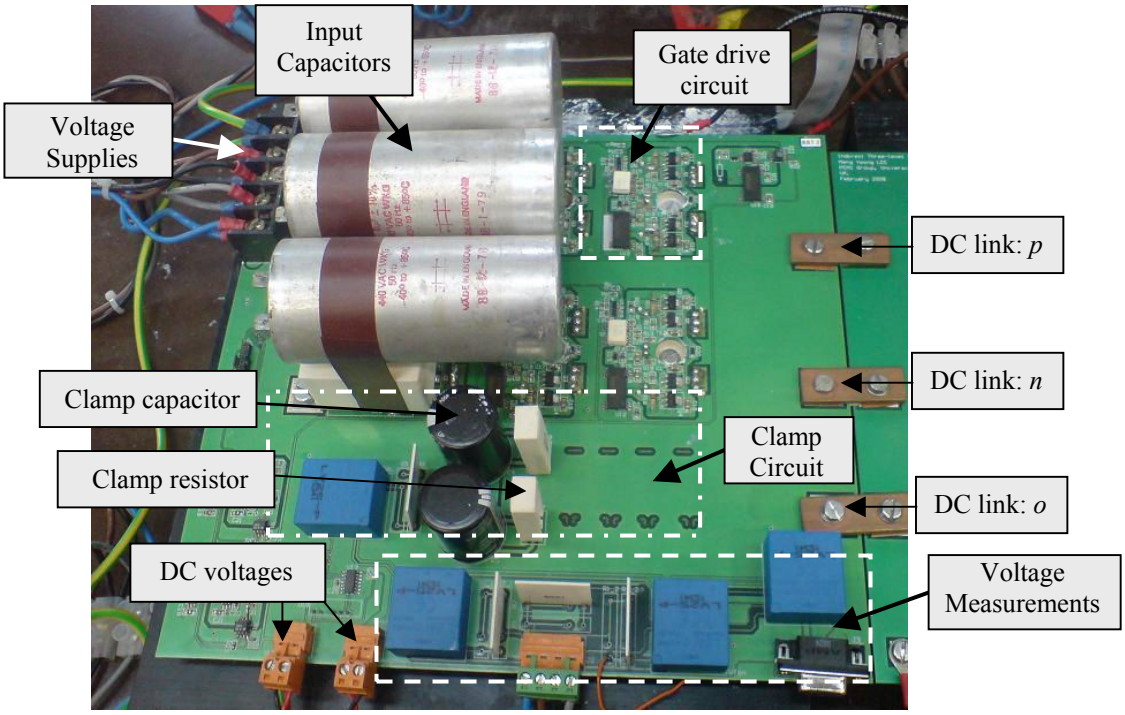


Figure 7.14: The rectification stage circuit board

As shown in Figure 7.14, a clamp circuit is built on the PCB of the rectification stage. The clamp circuit is the protection circuit that limits the over-voltage level on both the supply side and the load side in order to ensure the safe operation of the converter. Even though there is a connection from the DC-link middle point '*o*' to the neutral point of the input capacitors, the clamp circuit configuration for the indirect matrix converter topology, shown in Figure 2.18, can be applied to the three-level matrix converter topologies. This is because, during over-voltage, the diodes that provide the current paths to the DC-link point '*o*' (at the inversion stage) are reverse-biased by the positive voltage level applied to the *p*-terminal and the negative voltage level applied to the *n*-terminal of the DC-links.

For this prototype, eight 8EWF12S fast recovery diodes were used to construct the clamp circuit, which have been placed at the bottom layer of the PCB. Each diode has a rating of 1200V and 8A. During over-voltage, the converter is shut down and the fast-recovery diodes provide paths for the current to charge up two series-connected

electrolytic capacitors of 150 μ F, 450V. The stored energy from the inductance of the load is then dissipated by the 47k Ω resistor that is connected in parallel with each capacitor. To detect an over-voltage, a detection circuit was built to monitor the clamp circuit's DC-link voltage. Referring to Figure 7.15, the DC-link voltage of the clamp circuit is measured using a LEM LV25-P voltage transducer. The reference voltage for the transducer is the non-inverting input of a comparator. A maximum value of 700V has been set for this converter. The comparator would generate a high logic signal for the FPGA if the clamp circuit's DC-link voltage is larger than 700V.

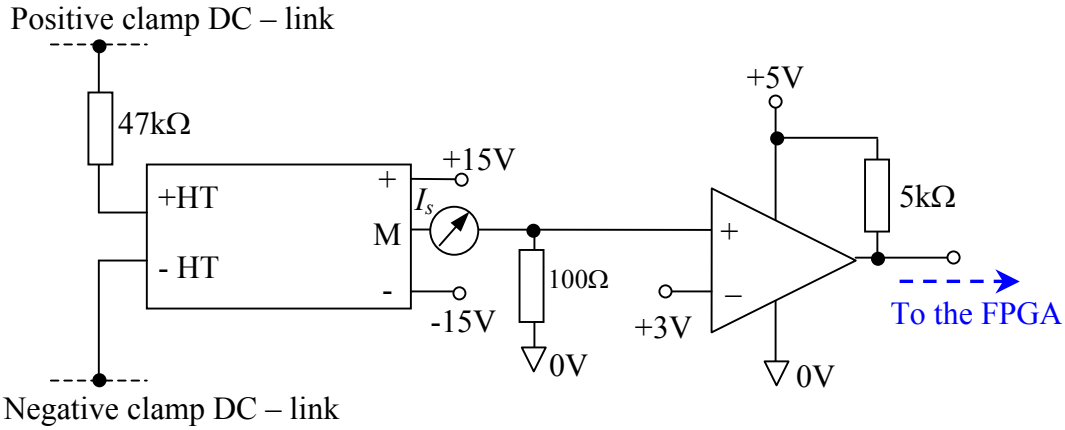


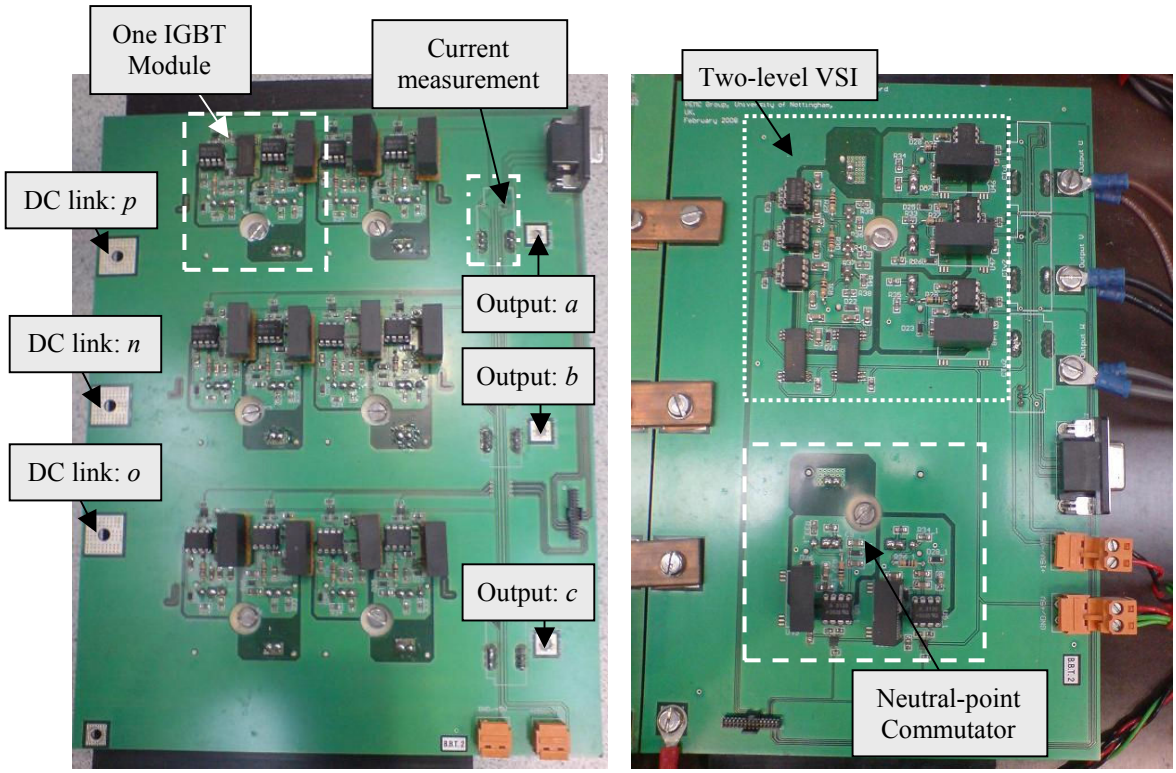
Figure 7.15: The over-voltage detection circuit

Due to the different circuit configuration of the inversion stage of each three-level matrix converter topology, two custom-designed four-layer PCBs were built, as shown in Figures 7.16(a) and 7.16(b). For both PCBs, the top and bottom layers are signal planes that consist of the gate drive circuits, the gate signal tracks and the DC voltage supplies tracks. The two inner layers of the PCB are used as the ground and power plane.

For the three-level-output-stage matrix converter the circuit configuration of the three-level neutral point clamped voltage source inverter stage requires six SK40GB123 IGBT modules and six 30EPF12 clamping diodes, as shown in Figure 7.16(a). Each SK40GB123 IGBT module comprises two series-connected IGBT. For the indirect three-level sparse matrix converter the circuit configuration of the inversion stage is

simpler and more compact. The two-level voltage source inverter can be easily constructed using just one SK30GB123ET IGBT module with one SK40GB123 IGBT module acting as the neutral-point commutator.

A picture of the three-level matrix converter prototype is presented in Figure 7.17. To connect the rectification stage to the inversion stage, short copper bars are bolted between the output terminals of the rectifier and the input terminals of the inverter. Heatsinks are attached to the IGBT modules for cooling purposes.



(a) (b)

Figure 7.16: The PCB of the inversion stage (a) the three-level-output-stage matrix converter and (b) the indirect three-level sparse matrix converter

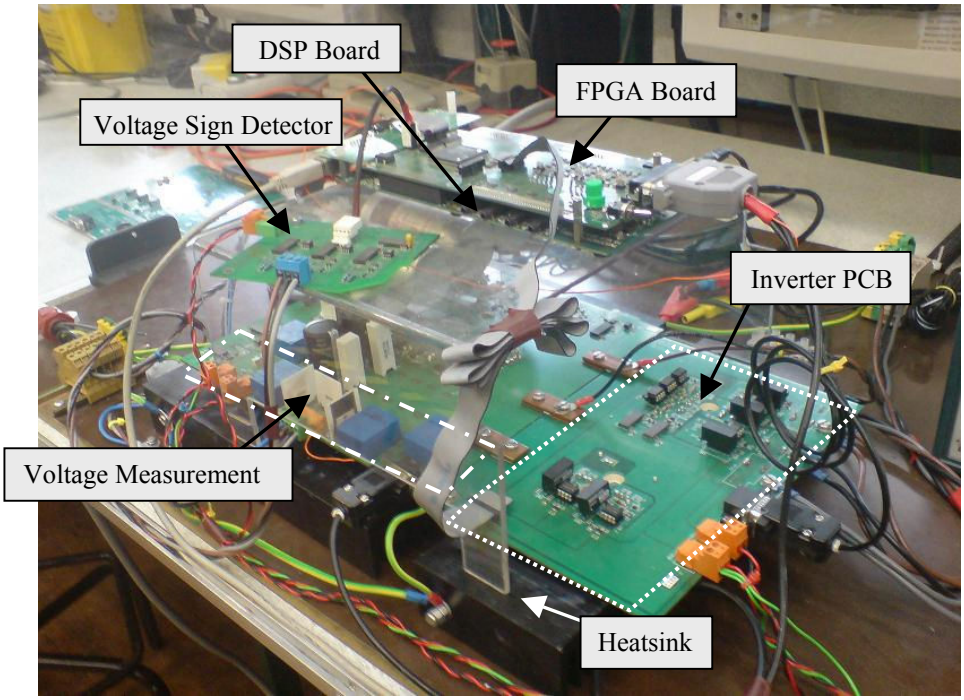


Figure 7.17: The overview of a 5kW three-level matrix converter prototype

7.3 Experimental Validation

The prototypes were tested at realistic power levels in the laboratory to prove the abilities of the three-level matrix converters to generate multilevel output voltages as well as maintain a set of sinusoidal and balanced input currents. In addition, to show that the three-level matrix converter topologies are able to generate higher quality output waveforms, the experimental results for the indirect matrix converter topology are generated for comparison. By disabling the gating signals to the neutral-point commutator, the prototype of the indirect three-level sparse matrix converter can be operated as an indirect matrix converter topology.

Using a 156V(rms) supply, the converter prototypes were tested at different modulation indexes using a balanced, star-connected resistor plus inductor load. The experimental parameters are:

- Input: V_{in_rms} = 156V, f_i = 50Hz
- Input filter: L_f = 0.633mH, C_f = 10μF
- Load: R_L = 20Ω, L_L =10mH
- Output frequency: f_{out} = 30Hz
- Switching frequency: f_{sw} = 5kHz

7.3.1 Output performance evaluation

In this section the output performances of the three-level matrix converter topologies are evaluated. To show the ability of the three-level matrix converter topologies to generate multilevel output voltages Figures 7.18 and 7.19 present the experimental waveforms with the voltage transfer ratios are equal to 0.4 and 0.8. The experimental waveforms, shown in both figures, consist of the DC-link voltage (V_{pn}); the potentials at the DC – link terminals referenced to the neutral-point (V_{po} and V_{no}); the output terminal voltage (V_{ao}); the output line-to-line voltage (V_{ab}) and the load currents (i_a, i_b and i_c).

For the three-level-output-stage matrix converter, the rectification stage generates maximum DC-link voltage (V_{pn}) for the inversion stage. This voltage is shown in Figures 7.18(a) and 7.18(b), which are the same despite the voltage transfer ratio is changed. This result shows the inversion stage controls the overall voltage transfer ratio of this three-level matrix converter topology. To provide the dual voltage supplies required by the inversion stage, V_{pn} is transformed into V_{po} and V_{no}. Due to the presence of third order input frequency harmonics, V_{po} and V_{no} are clearly unequal, as shown in Figures 7.18(c) and 7.18(d).

The output terminal voltage (V_{ao}), shown in Figures 7.18(e) and 7.18(f), clearly demonstrates how the three-level-output-stage converter applies the DC-link voltage levels (V_{po}, $0V$ or V_{no}) to the output terminal 'a' when the voltage transfer ratio is 0.4 and 0.8. At high voltage transfer ratios the three-level-output-stage matrix converter evidently generates three distinctive voltage levels for V_{ao}, as shown in Figure 7.18(f).

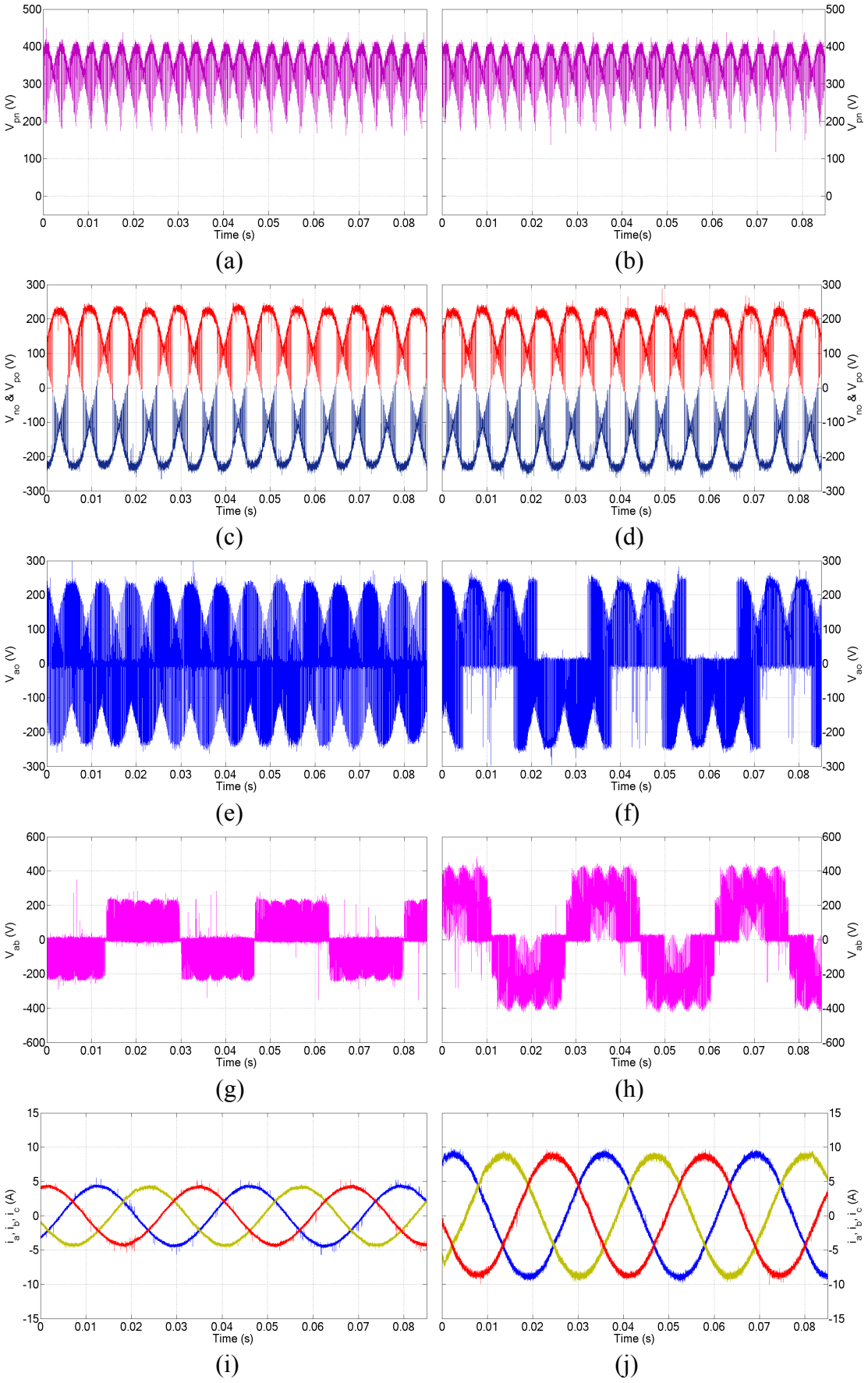


Figure 7.18: The experimental waveforms generated by the three-level-output-stage matrix converter when the voltage transfer ratio is 0.4 (left) and 0.8 (right).

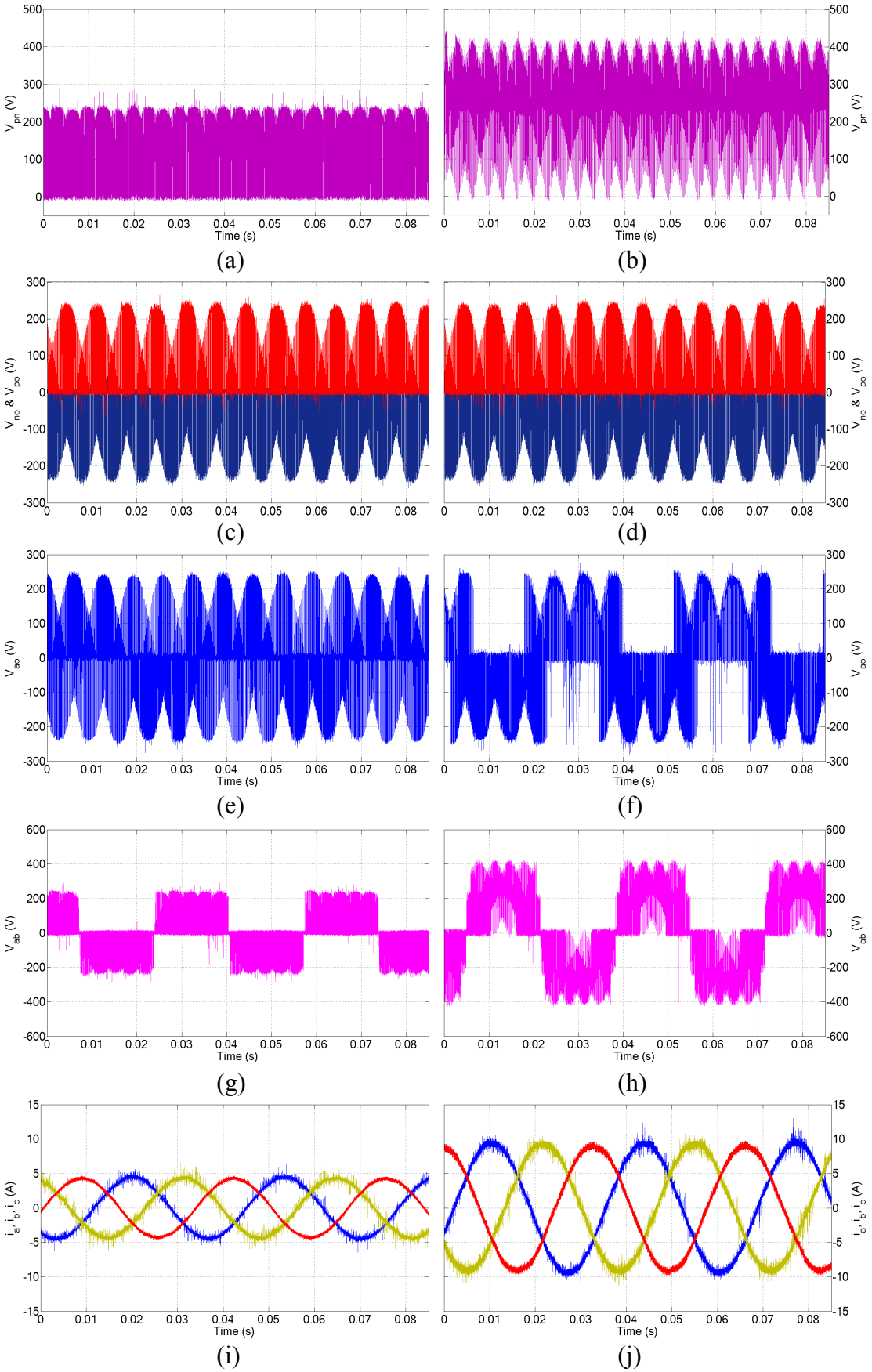


Figure 7.19: The experimental waveforms generated by the indirect three-level sparse matrix converter when the voltage transfer ratio is 0.4 (left) and 0.8 (right).

Having the ability to generate three voltage levels at each output terminal, the three-level-output-stage matrix converter is able to generate five line-to-line output voltage levels at high voltage transfer ratios, shown in Figure 7.18(h). At low voltage transfer ratios the output line-to-line voltage, V_{ab}, for the converter has a three-level profile, shown in Figure 7.18(g). The magnitude is limited to the input line-to-neutral point voltages. The load current waveforms presented in Figures 7.18(i) and 7.18(j) are sinusoidal and balanced, proving the effectiveness of the modulation strategy in controlling the three-level-output-stage matrix converter.

For the indirect three-level sparse matrix converter, the rectification stage is also modulated to generate maximum DC-link voltage (V_{pn}) and provide three voltage levels at the DC-link: V_{po}, 0V and V_{no}. However, at any instant, the inversion stage can only be operated with two voltage levels. Therefore, according to the selected voltage vectors, the rectification stage and neutral point commutator are switched to provide the required voltage levels to the inversion stage. Referring to Figure 7.19(b), the increase in V_{pn} when the voltage transfer ratio is 0.8 is because the rectification stage constantly connects the input line-to-line voltages (V_{AB}, V_{BC} and V_{CA}) to the inverter terminals (*p_inv* and *n_inv*), enabling the inversion stage to generate higher output voltages at high voltage transfer ratios. At low voltage transfer ratios only the input line-to-neutral point voltages (V_{Ao}, V_{Bo} and V_{Co}) are connected so the magnitude of V_{pn} is limited to the peak levels of the input phase voltages, as shown in Figure 7.19(a). The switching in V_{po} and V_{no}, shown in Figures 7.19(c) and 7.19(d), clearly reveal the operation of the rectification stage and neutral-point commutator to control the voltage levels supplied to the inversion stage.

The output terminal voltage V_{ao}, shown in Figure 7.19(f), shows the ability of the indirect three-level sparse matrix converter to generate three distinct voltage levels at the output terminal. Therefore, similar to the three-level-output-stage matrix converter, the indirect three-level sparse matrix converter is able to generate a transition from three levels to five levels in the output line-to-line voltage (V_{ab}) when the voltage transfer ratio is changed from 0.4 to 0.8, as shown in Figures 7.19(g) and 7.19(h). The load current waveforms presented in Figures 7.19(i) and 7.19(j) clearly show the modulation strategy is able to control the indirect three-level sparse matrix converter topology to generate a set of sinusoidal and balanced output waveforms.

The experimental results shown in Figures 7.18 and 7.19 can be compared to the simulation results given in Figures 5.15 and 6.14 respectively. To show that the three-level matrix converter topologies generate higher quality output waveforms than the indirect matrix converter the output line-to-line voltage (V_{ab}) and output voltage spectrum for each topology is compared to one another at a high modulation index (V_{out_rms} = 125V) and a low modulation index (V_{out_rms} = 62V), as shown in Figures 7.20 and 7.21 respectively.

As shown in Figure 7.20, the three-level matrix converter topologies generate five distinctive voltage levels for V_{ab} at high modulation indexes, while the indirect matrix converter only generates three levels. Therefore, referring to the output voltage spectra, the output switching frequency harmonics for the three-level matrix converters are lower than the indirect matrix converter. When comparing the three-level-output-stage matrix converter to the indirect matrix converter, the output harmonics for this multilevel matrix converter, shown in Figure 7.20(b), are reduced from 20V to 16V (f_{sw}) and 51V to 33V ($2f_{sw}$). For the indirect three-level sparse matrix converter, the output harmonics are improved from 20V to 16V (f_{sw}) and 51V to 35V ($2f_{sw}$), when compared to the indirect matrix converter.

At a low modulation index, the output line-to-line voltages for the three-level matrix converters have a three-level profile, as shown in Figure 7.21. This waveform is similar to the indirect matrix converter (Figure 7.21e) but the magnitudes of the voltage levels are limited to the peak levels of the input line-to-neutral point voltages. Therefore, the output switching frequency harmonics for the three-level matrix converters are significantly reduced. Compared to the indirect matrix converter, the output switching frequency harmonics for the three-level-output-stage matrix converter, shown in Figure 7.21(b), are reduced from 9V to 7V (f_{sw}) and from 52V to 15V($2f_{sw}$). The output voltage switching frequency harmonics for the indirect three-level sparse matrix converter, shown Figure 7.21(d), are reduced from 9V to 5V (f_{sw}) and from 52V to 14V($2f_{sw}$).

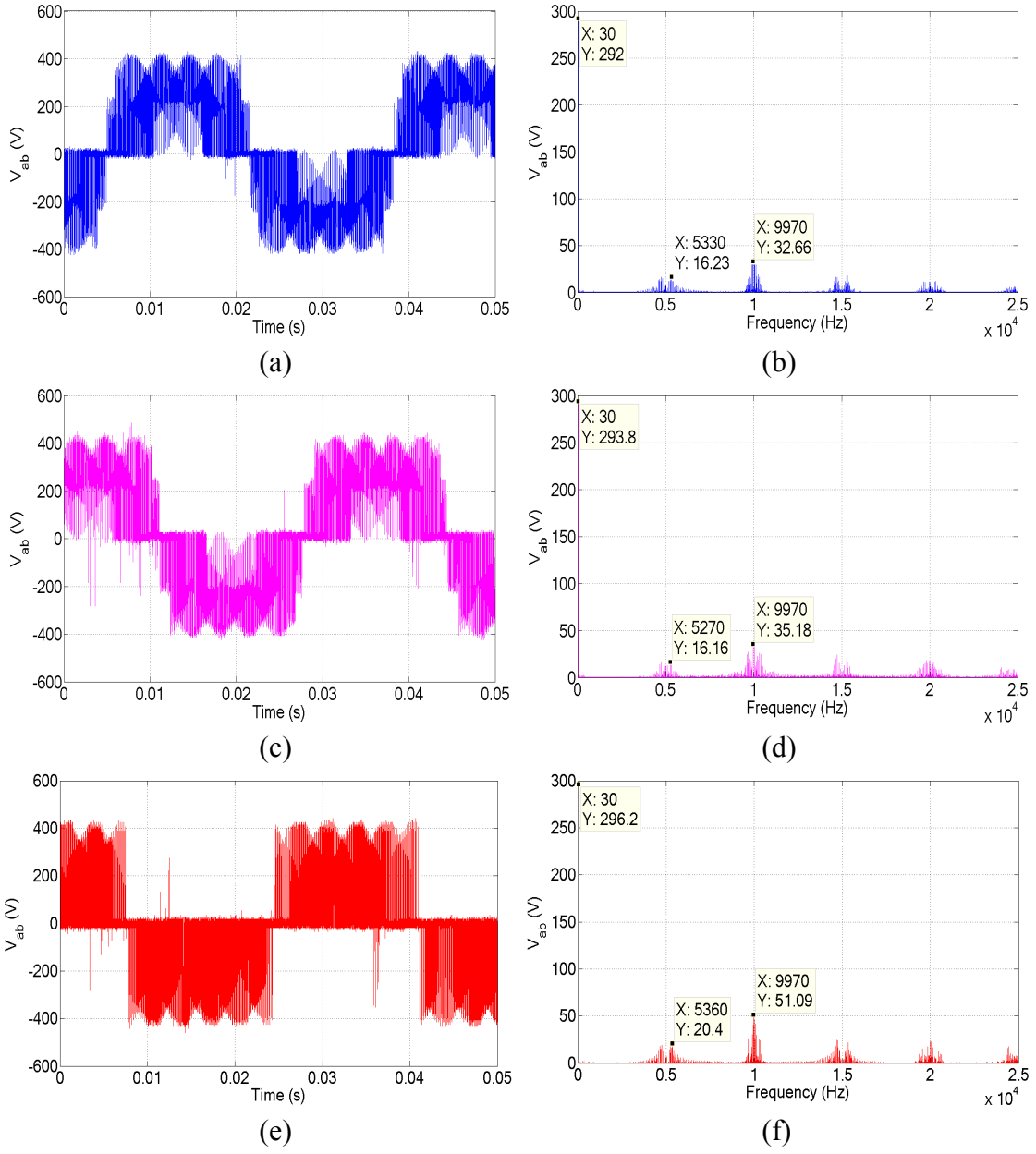


Figure 7:20: The output line-to-line voltages and output voltage spectra (a)(b) the three-level-output-stage matrix converter, (c)(d) the indirect three-level sparse matrix converter and (e)(f) the indirect matrix converter at a high modulation index (V_{out_rms} = 125V).

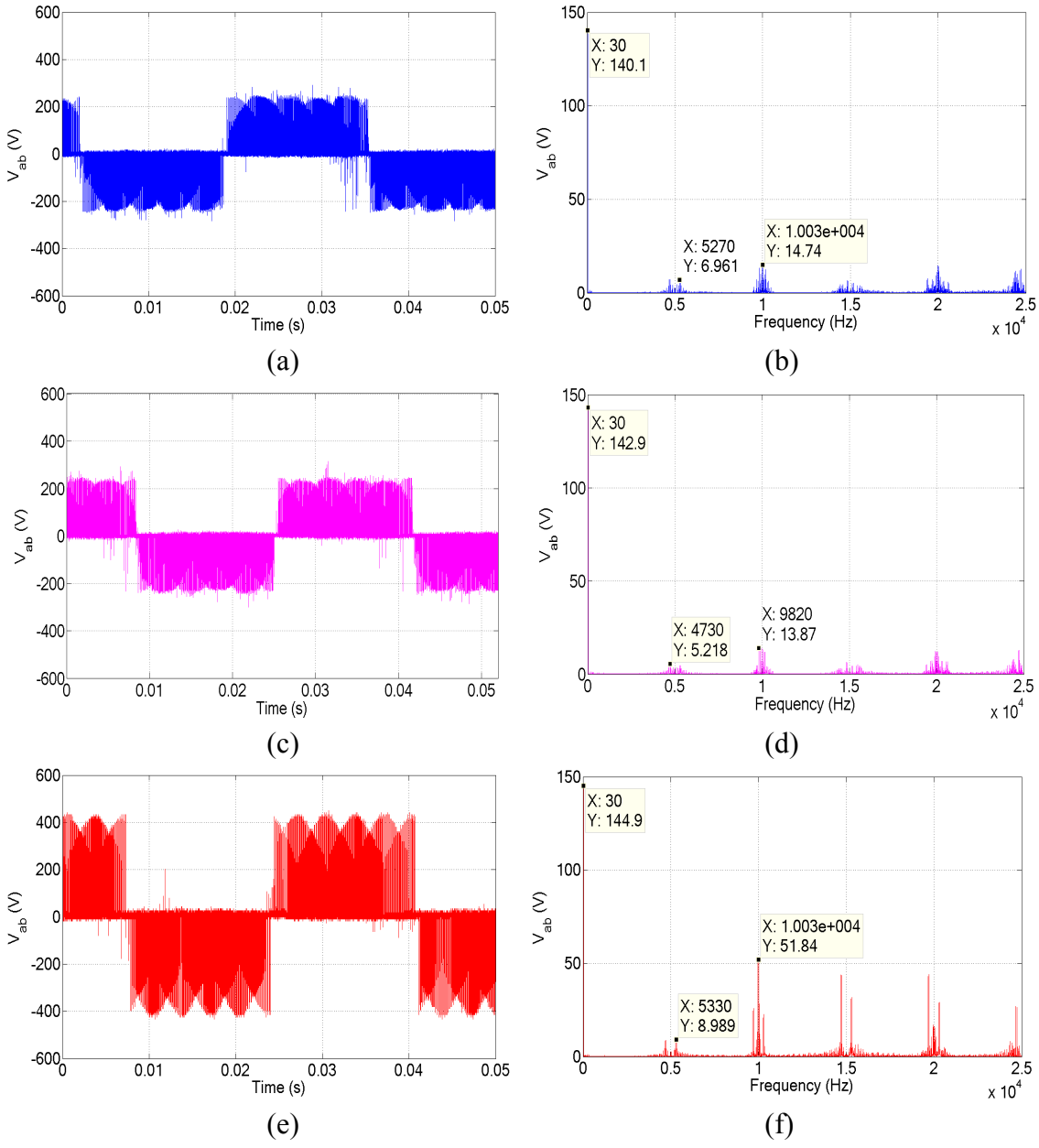


Figure 7.21: The output line-to-line voltages and output voltage spectra (a)(b) the three-level-output-stage matrix converter (c)(d) the indirect three-level sparse matrix converter and (e)(f) the indirect matrix converter at a low modulation index (V_{out_rms} = 62V).

Besides analyzing the output voltage spectra, the total harmonic distortions (THD) of the output line-to-line voltage for these topologies are calculated and presented in Figure 7.22. Similar to Figure 6.17, the three-level matrix converter topologies have lower harmonic distortion than the indirect matrix converter, especially at low voltage transfer ratios, due to their ability to construct the output voltage waveforms with smaller voltages. The THD for both multilevel matrix converters are similar at low voltage transfer ratios (< 0.5). At high output voltage transfer ratios (>0.5) the THD for the three-level-output-stage matrix converter is clearly lower than the indirect three-level sparse matrix converter. The ability of the three-level-output-stage matrix converter to achieve the medium voltage vectors enables the converter to synthesize the reference output vector with a better selection of the nearest three space vectors, compared to the indirect three-level sparse matrix converter. As a result, the harmonic content in the output waveforms for the three-level-output-stage matrix converter is lower. However, the difference in THD between the multilevel matrix converters decreases when the voltage transfer ratio approaches 0.8. This decrease is because the large voltage vectors of both multilevel matrix converters become more dominant in synthesizing the reference output vector.

The THD for the load current of the three-level matrix converters, shown in Figure 7.23, reveals another advantage of constructing the output waveforms with multiple smaller voltages. Compared to the indirect matrix converter the lower distortion in the load current, especially at low voltage transfer ratios, for the three-level matrix converters makes the multilevel matrix converter concept attractive in applications that have loads providing low filtering inductances. At low voltage transfer ratios (< 0.5), due to the uses of input line-to-neutral point voltages to generate the lower output voltage waveforms, the distortion in the load current for the three-level matrix converters is obviously lower than those for the indirect matrix converter that uses the full input line-to-line voltages, as shown in Figure 7.21. However, when the voltage transfer ratio approaches 0.8, the difference in THD between the three-level matrix converters and the indirect matrix converter decreases. This is because the three-level matrix converters use the input line-to-line voltages more frequently to generate the output voltage waveforms, resembling the indirect matrix converter. As a result, the THDs for these topologies converge as the voltage transfer ratio approaches 0.8.

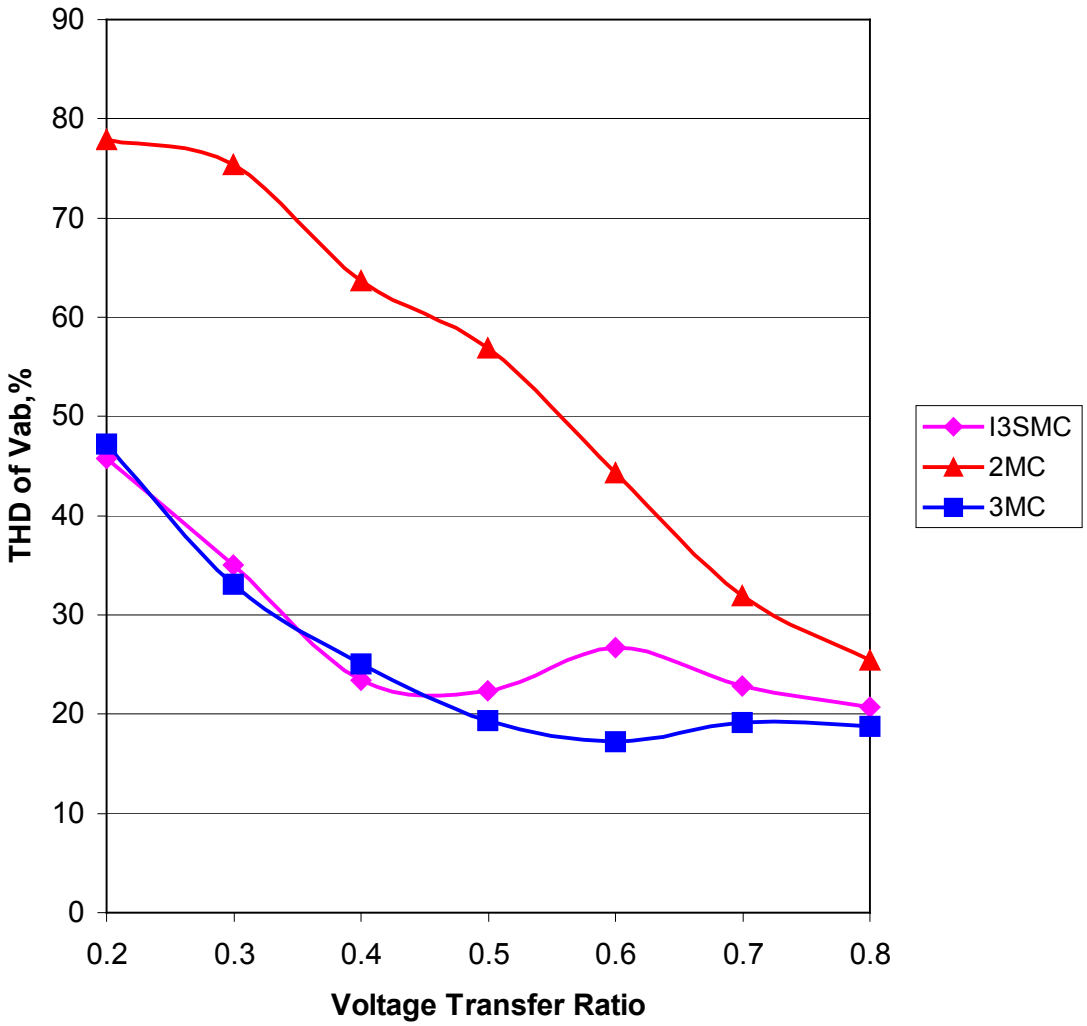


Figure 7.22: The THD for the output line-to-line voltage, V_{ab}, of the indirect three-level sparse matrix converter (pink), the three-level-output-stage matrix converter (blue) and the indirect matrix converter (red).

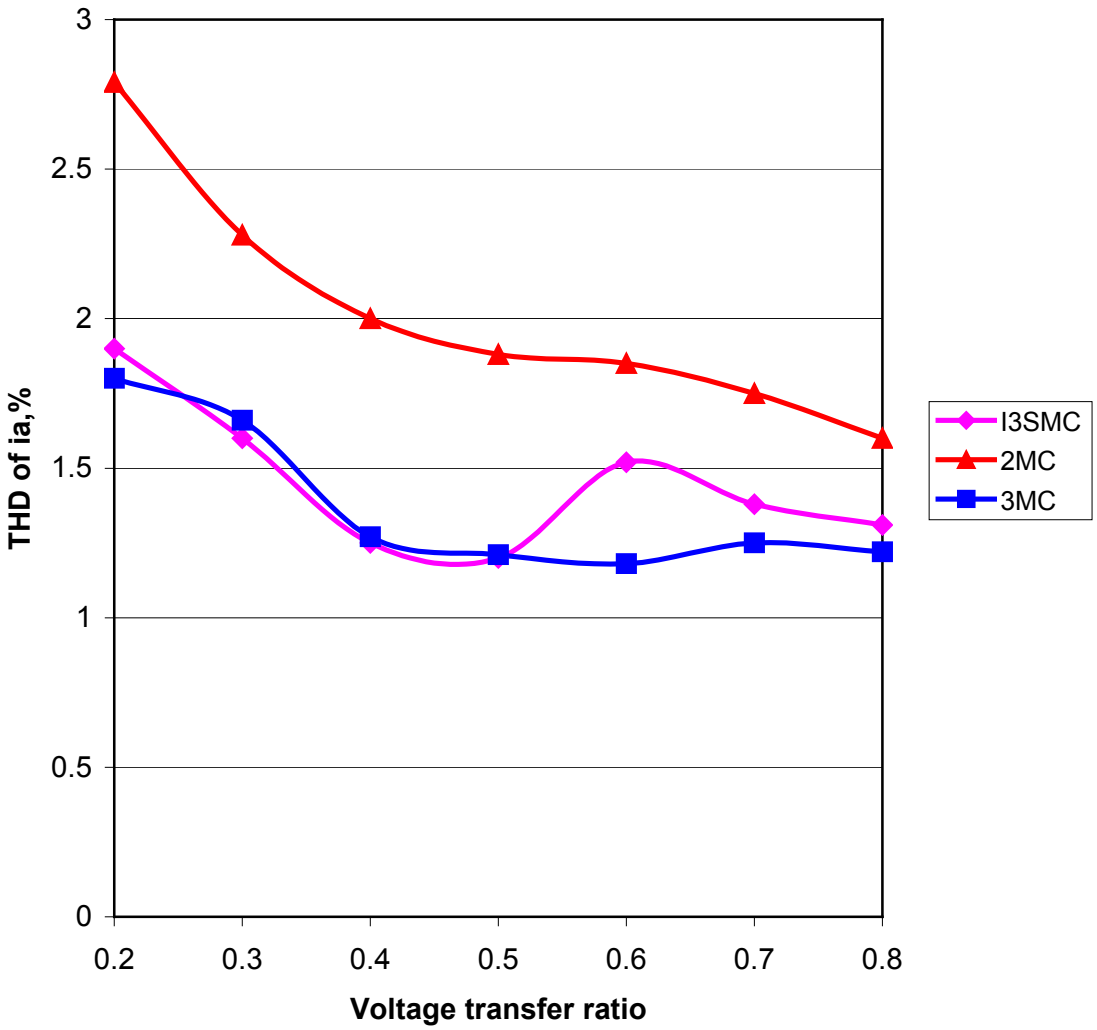


Figure 7.23: The THD for the output current, i_a, of the indirect three-level sparse matrix converter (pink), the three-level-output-stage matrix converter (blue) and the indirect matrix converter (red).

Based on the experimental results presented in Figures 7.20 – 7.23, the three-level matrix converter topologies have been shown to have better output performance than the indirect matrix converter in terms of the harmonic content of the output waveforms. Referring to Figures 7.22 and 7.23, the indirect three-level sparse matrix converter is obviously able to generate comparable quality outputs to the three-level-output-stage matrix converter, giving the indirect three-level sparse matrix converter an advantage since the circuit configuration of this converter is simpler than the three-level-output-stage matrix converter.

7.3.2 Input performance evaluation

In order to operate the three-level matrix converters, the stability of the input capacitor voltages is an important factor. As discussed in Chapters 5 and 6, the ability of the three-level matrix converters to connect the output terminal(s) to the neutral-point of the star-connected input filter capacitors can cause uneven charging/discharging of the input filter capacitors. Without proper control, the uneven changing voltage levels of the input capacitors would affect the DC-link voltages generated by the rectification stage, which has an impact on the ability of the inversion stage to generate proper multilevel outputs, causing output voltage distortion. To show the effectiveness of the modulation strategy in maintaining the input capacitor voltages Figure 7.24 shows the voltage levels of the input capacitors for the three-level matrix converters at a high modulation index (V_{out_rms} = 125V) and a low modulation index (V_{out_rms} = 62V). For comparison, the input capacitor voltages for the indirect matrix converter are also presented, shown in Figures 7.24(e) and 7.24(f).

Referring to Figure 7.24, the unbalance in the input capacitor voltages is noticeable. This unbalance is not due to the neutral-point current since the indirect matrix converter also exhibits the same condition. This unbalance is due to the voltage measurements referenced to a virtual neutral-point of the star-connected input filter capacitors. To check on the effectiveness of the modulation strategy in maintaining the voltage levels, the input capacitor voltages for three-level matrix converters are compared to those for the indirect matrix converters.

As shown in Figure 7.24 there is more distortion in the input capacitor voltages for the three-level matrix converters when compared the waveforms to those for the indirect matrix converter. The non-ideal switching characteristics (turn – on and turn – off time) of the switching devices and the use of time gap in the commutation strategy inevitably limits the ability of the modulation strategy to fully balance the neutral-point current. The distortion in the input capacitor voltages is larger at higher modulation indexes. This is due to the higher load currents that cause more significant charging/discharging of the input filter capacitors. Nevertheless, the stability of the input capacitor voltages is still maintained, proving that the modulation strategy is able to maintain the voltage levels of the input filter capacitors.

Referring to Figure 7.25, the input current waveforms of the three-level matrix converters are balanced and sinusoidal. This result evidently shows that the modulation strategy is able to modulate the three-level matrix converters to generate a set of sinusoidal, balanced input currents despite the presence of the neutral-point current.

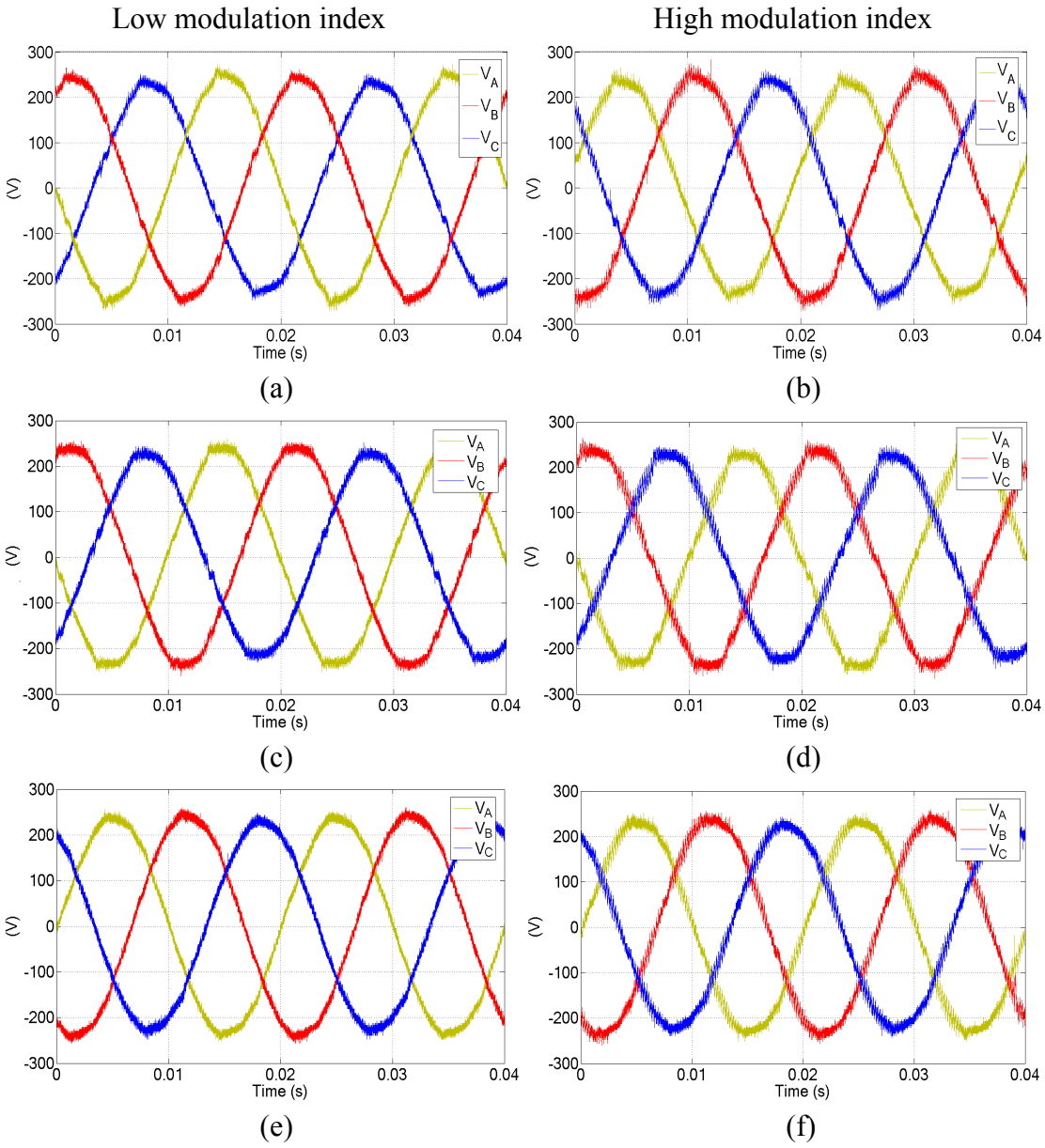


Figure 7.24: The input filter capacitor voltages (a)(b) the three-level-output-stage matrix converter, (c)(d) the indirect three-level sparse matrix converter and (e)(f) indirect matrix converter.

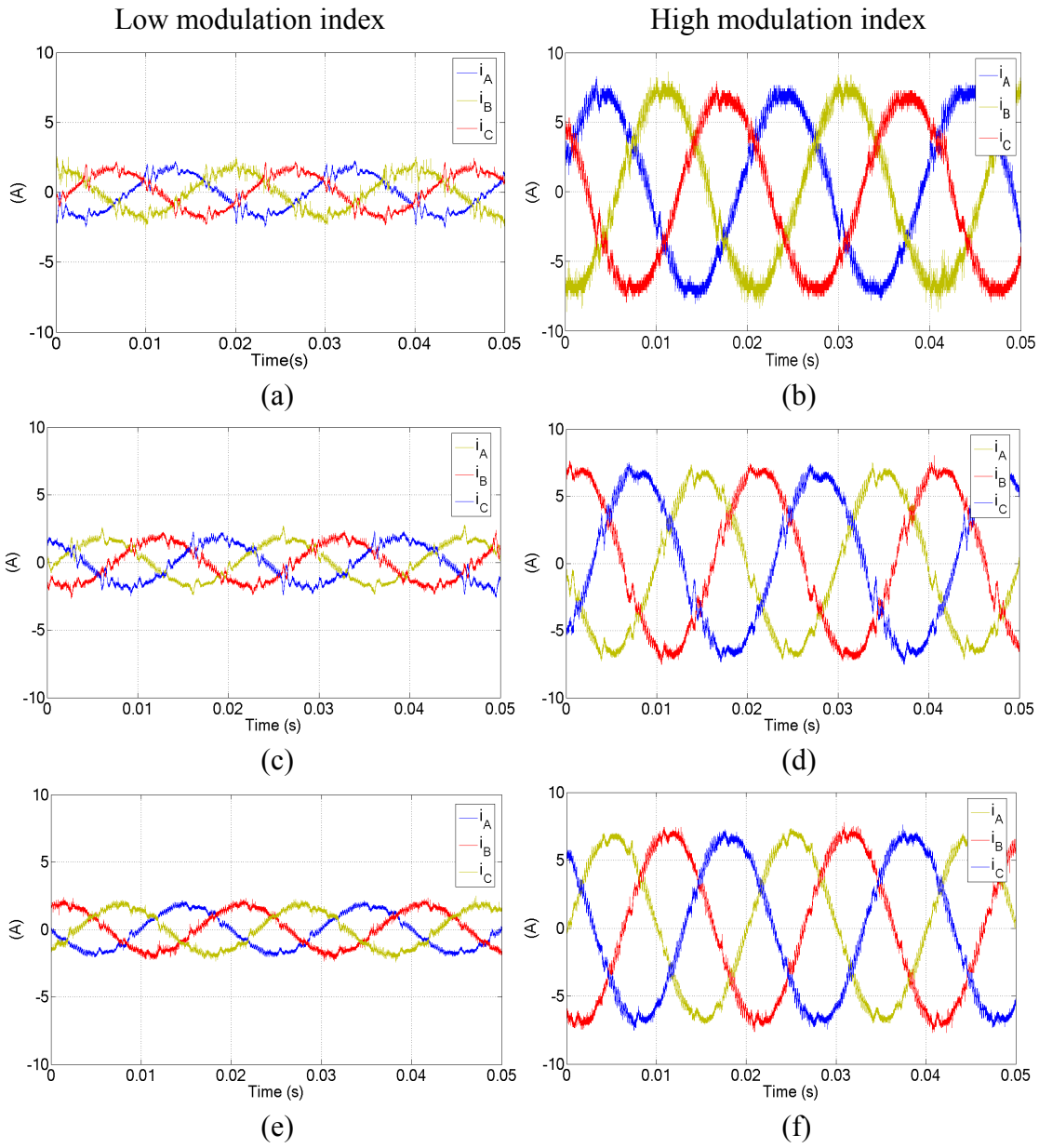


Figure 7.25: The input current waveforms (a)(b) the three-level-output-stage matrix converter, (c)(d) the indirect three-level sparse matrix converter and (e)(f) indirect matrix converter.

7.4 Conclusions

In this chapter, an explanation of the hardware implementation and experimental results from the three-level matrix converter topologies has been given. The design of each circuit for the converter prototypes has been described. In the experimental testing the results from the three-level matrix converter prototypes clearly correspond well to the simulation results. This outcome validates the abilities of the three-level matrix converters to generate multilevel output voltages and the effectiveness of the modulation strategy in maintaining the input filter capacitor voltages as well as generating a set of sinusoidal, balanced input currents, despite the presence of the neutral point current. Compared to the indirect matrix converter, the three-level matrix converters are also shown to able to generate higher quality output waveforms in terms of harmonic content.

Chapter 8

Semiconductor losses in the three-level matrix converters

8.1 Introduction

Even though the output performances of the three-level matrix converters are superior to the indirect matrix converter, a higher number of power semiconductor devices and additional switching in the modulation patterns are required to achieve the desired results. Therefore, this chapter investigates the semiconductor losses in these converter topologies in order to identify any disadvantage.

In general, there are two types of semiconductor losses in a power converter topology: conduction loss and switching loss. The conduction loss is due to the voltage drop across the active semiconductor device when conducting current while the switching loss occurs at each current commutation of the device. In this work, a model based simplified semiconductor losses estimation approach is used to determine the semiconductor losses in the three-level matrix converter topologies.

Since the three-level matrix converter topologies were constructed using IGBTs and diodes, a model for calculating the conduction and switching losses for these devices is described first. Then, the procedures for calculating the semiconductor losses in each three-level matrix converter topology are discussed. Finally, the total semiconductor losses in the three-level matrix converters are compared with the indirect matrix converter topology in order to determine the relative efficiencies of the three-level matrix converter topologies.

8.2 Modeling of conduction losses

For an IGBT, the conduction loss can be modeled by the power dissipation caused by the voltage drop across the device and the current through the device, which can be expressed as below:

$$P_{cond-igbt}(t) = i_{C\_igbt}(t) * v_{CE}(t) \tag{8.1}$$

where i_{C_igbt} is the instantaneous collector current and v_{CE} is the instantaneous collector to emitter saturation voltage of the device. The relationship between v_{CE} and i_{C_igbt} is the forward characteristic of the IGBT and is normally given in the device datasheet. To simplify the modeling process, the forward characteristic can be linearised into the form:

$$v_{CE}(t) = V_{CE\_sat} + R_{CE} \cdot i_{C\_igbt}(t) \tag{8.2}$$

where V_{CE_sat} is the forward voltage drop across the device when the collector current is small and R_{CE} is the approximate on-state resistance slope. In the device datasheet, two forward characteristic curves for device junction temperatures of 25^{o}C and 125^{o}C are provided. This is because the forward characteristic of the device varies with the junction temperature. In order to obtain a reasonable approximation, the forward characteristic is linearised based on the assumption that the device is operated at the intermediate operating temperature, as shown in Figure 8.1(a). The linearised characteristic will generally be valid for currents above 20% of the device rating [73]. Below this threshold the error will not be significant in comparison with the total conduction loss due to the low level of current. Substituting (8.2) into (8.1) gives:

$$P_{cond-igbt}(t) = i_{C\_igbt}(t) * \left(V_{CE\_sat} + R_{CE} \cdot i_{C\_igbt}(t)\right) \tag{8.3}$$

The average conduction power loss in an IGBT over a time interval, T, can then be estimated:

$$\overline{P}_{cond-igbt} = \frac{1}{T} \cdot \int_0^T P_{cond-igbt}(t) \cdot dt \tag{8.4}$$

The time interval, T, must includes an integer number of the supply and load frequency cycles in order to provide a reasonable estimation of the average conduction loss in the IGBT. In the same way, the conduction loss in a diode can be modeled:

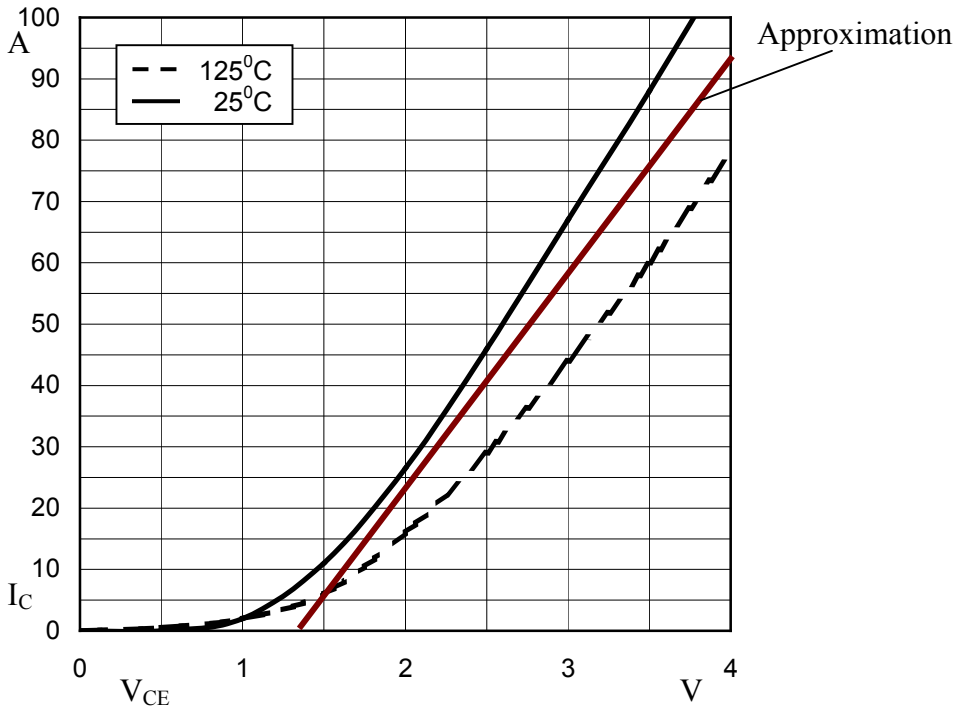
$$P_{cond-d}(t) = i_F(t) * (V_{F0} + R_F \cdot i_F(t)) \tag{8.5}$$

where V_{F0} is the forward voltage drop across the diode when the forward current of the device (i_F) approaches zero and R_F is the approximate on-state resistance slope of the device, as shown in Figure 8.1(b). Since the three-level matrix converter topologies will not be operated above 80A, a linearised characteristic below 80A is shown in the figure. Over a time interval, T, the average conduction power loss in a diode can be estimated:

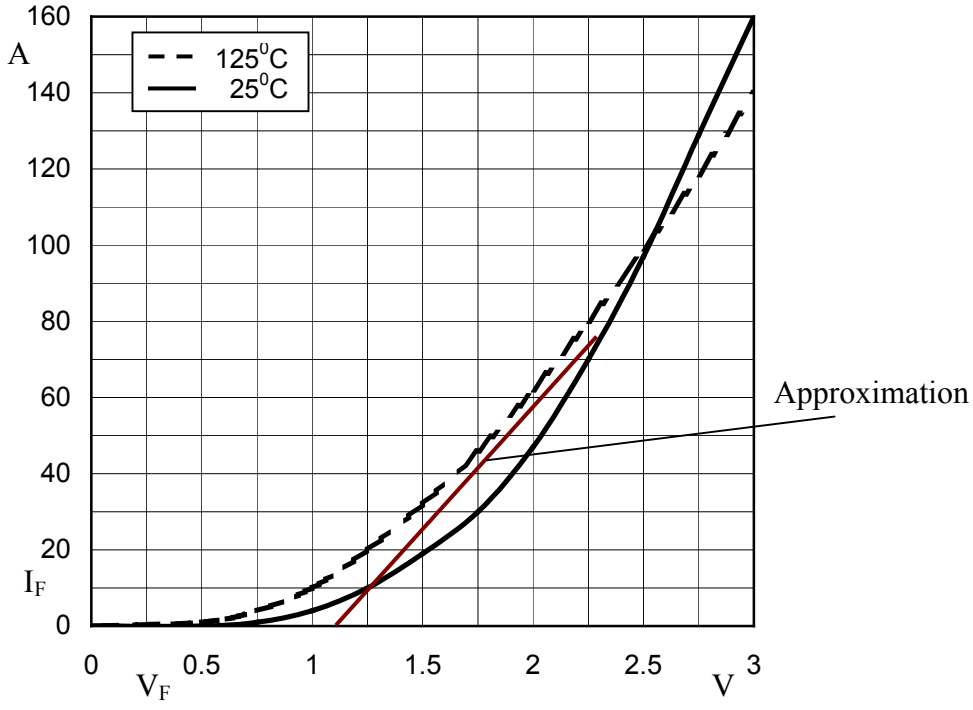
$$\overline{P}_{cond-d} = \frac{1}{T} \cdot \int_0^T P_{cond-d}(t) \cdot dt \tag{8.6}$$

8.3 Modeling of switching losses

Due to the non-ideal switching characteristic of the power semiconductor device, there is always a finite time taken for the device to change state. If the commutation occurs when the current through the device or the voltage across the device is nearly zero, the power loss is negligible and the commutation is referred to as 'soft switching'. However, in most situations, the current and voltage during the commutation are non-zero. Such commutation causes considerable power loss and is referred to as 'hard switching'. Since the energy loss involved in the soft switching is far less than the hard switching, only the losses associated with the hard switching are analyzed in this chapter.



(a) IGBT (V_{CE_sat} = 1.4V, R_{CE} = 26.6mΩ @ V_{GE} = 15V)



(b) Diode (V_{F0} = 1.1V, R_F = 15.11mΩ)

Figure 8.1: The forward characteristic curves from the datasheet of the SEMIKRON IGBT module, SK60GM123.

Figures 8.2 and 8.3 show an approximated behavior of the current and voltage for an IGBT module (constructed with an anti-parallel freewheeling diode) during the hard turned-on and hard turned-off situations, respectively. As shown in Figure 8.2, when the IGBT is turned on at t_0, the collector current (I_C) starts to rise at a fairly constant *di/dt* and the load current (I_L) in the freewheeling diode (of the opposite leg) gradually transfers to the IGBT. Due to the parasitic inductance in the IGBT module, the device (collector – emitter) voltage, V_{CE}, experience a voltage drop (V_{plat}) during this current rise, resulting a plateau in the voltage waveform. When the load current is fully transferred to the IGBT, the outgoing freewheeling diode starts to turn off and force its reverse recovery current (I_{rr}) flowing through the IGBT, causing an overshoot in the collector current. After the collector current reaches the peak value ($I_L + I_{rr}$) at t_1, the collector-emitter voltage begins to fall while the freewheeling diode starts to gain its reverse voltage. The switching process is completed at t_2 with $I_C = I_L$ and $V_{CE} = 0$. As shown in Figure 8.2, a triangle is used to approximate the power loss across the switching time, t_{on}. The area under the triangle represents the amount of energy loss, E_{on}, during the hard turned-on situation of the IGBT.

On the other hand, during the hard turned-off situation, the power loss in the IGBT module consists of the main switching loss and the loss due to the 'tail' current, as shown in Figure 8.3. When the IGBT is turned-off at t_0, the collector-emitter voltage (V_{CE}) starts to rise at a rate dV_{CE}/dt. Due to the parasitic capacitance, there is a current drop (I_{plat}) during this voltage rise, causing a plateau in the collector current waveform. When V_{CE} reaches the forward blocking voltage, V_{CEF}, the freewheeling diode (of the opposite leg) is forward-biased and starts to take over the load current (I_L). As a result, the collector current of the IGBT experiences a rapid fall, followed by a gentle drop to zero at t_2. The approximated distribution of the power loss during this hard turned-off is shown in Figure 8.3. Due to the comparatively small value of the tail current, the switching loss energy, E_{off}, is mostly contributed by the main switching loss during t_{off}.

For an IGBT with an anti-parallel freewheeling diode, the switching loss can be modelled by the switching loss energy associated with each switching event. In the device datasheet, the switching loss energies, E_{on} and E_{off}, were established by integrating the product of the collector current characteristic and the collector-emitter voltage characteristic across the total switching time, as shown below:

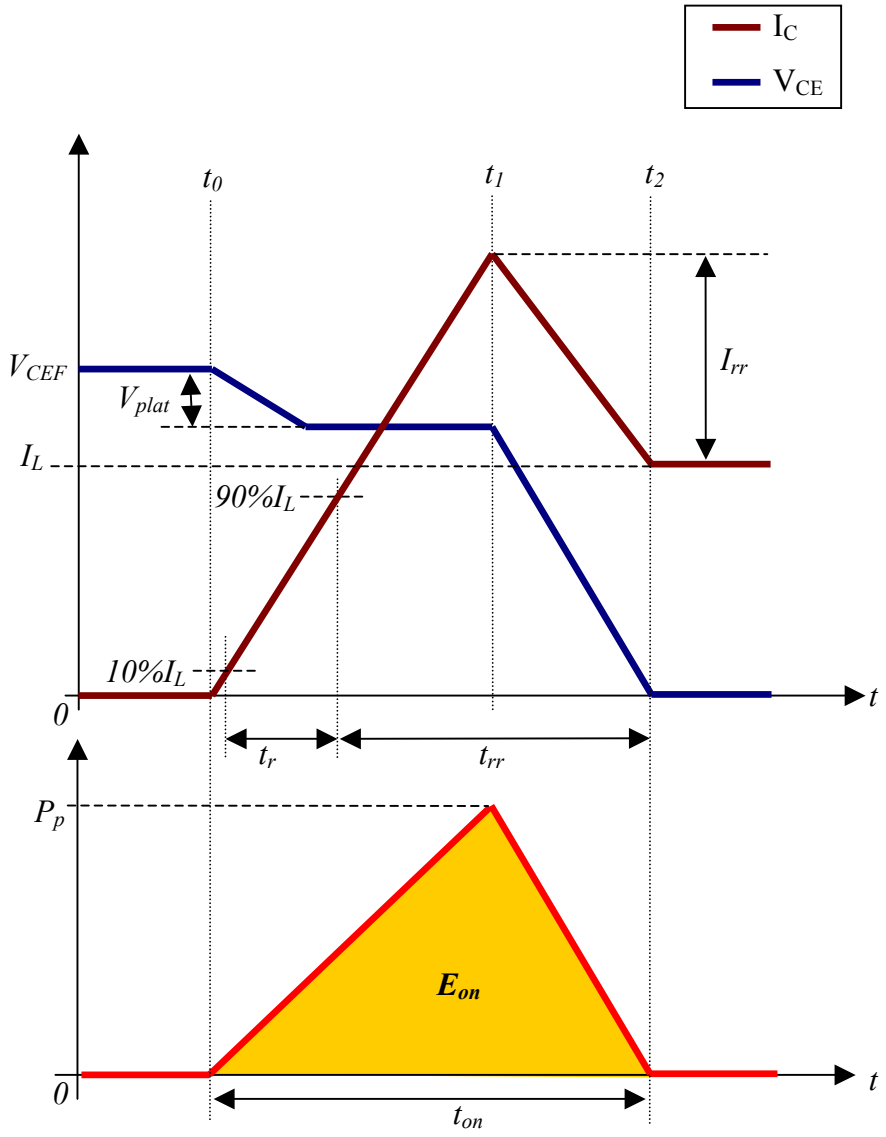


Figure 8.2: Approximation of the voltage and current waveforms at the hard turn-on situation of the IGBT and the contribution to power loss [73]

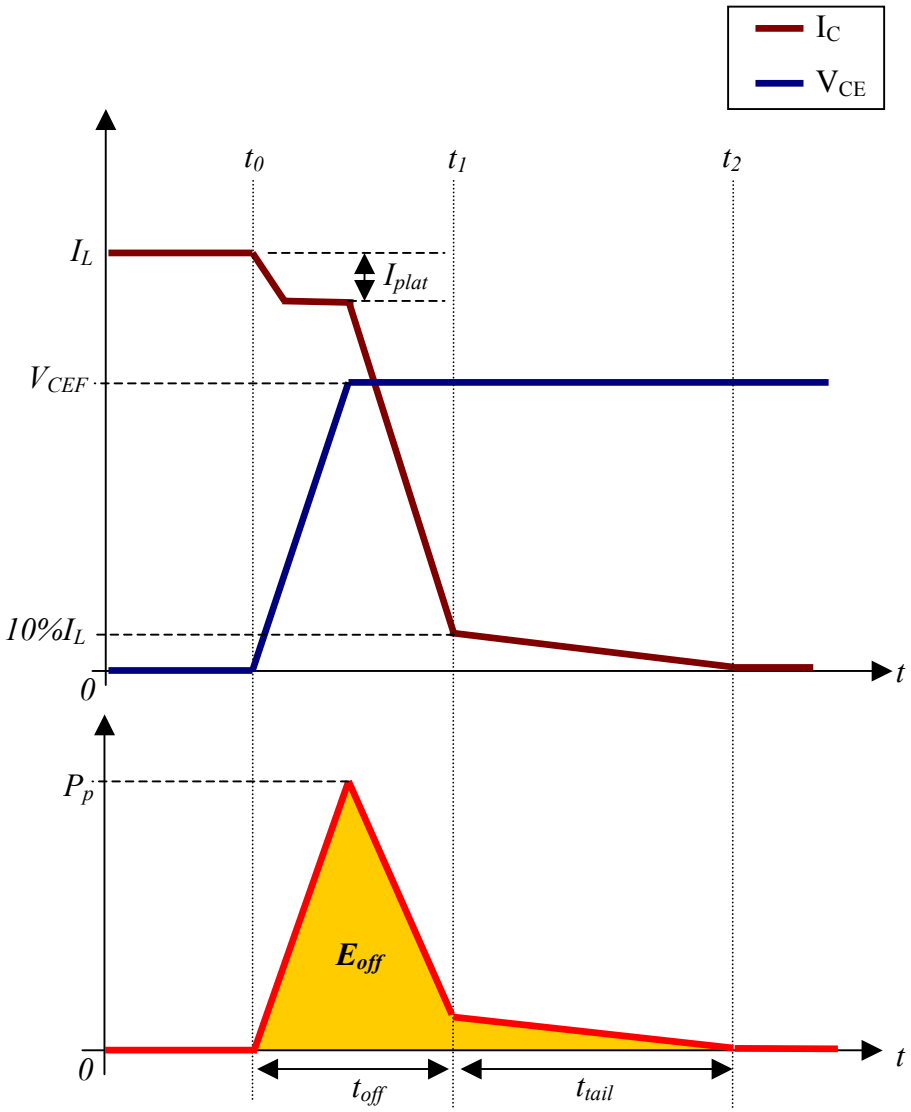


Figure 8.3: Approximation of the voltage and current waveforms at the hard turn-off situation of the IGBT and the contribution to power loss [73]

$$E_{on} = \int_0^{t\_on} V_{CE} \cdot I_C \cdot dt \ , \qquad E_{off} = \int_0^{t\_off+t\_tail} V_{CE} \cdot I_C \cdot dt \tag{8.7}$$

To simplify the modelling process, the switching loss energy is linearised into a form that is proportional to the blocking voltage and the conducting current during the switching event [74,75]:

$$E_{SW} = E_{SWR} \cdot \frac{|v|}{V_{\mathrm{Re}f}} \cdot \frac{|i|}{I_{\mathrm{Re}f}} \tag{8.8}$$

where E_{SWR} is the rated switching loss energy at the reference voltage V_{Ref} and reference current I_{Ref}. V_{Ref} and I_{Ref} are the test parameters given in the device datasheets, while v and i are the actual commutation voltage and current during the switching event.

During a hard turned-on, E_{SWR} is E_{ON} while v is the voltage across the switch just before the commutation and i is the current through the switch just after the commutation. E_{SWR} is E_{off} for a hard turned-off of the IGBT where v is the collector – emitter voltage just after the commutation and i is the collector current just before the commutation. Over a time interval, T, the average switching power losses in an IGBT module can be estimated:

$$\overline{P}_{on} = \frac{1}{T} \cdot \int_0^T E_{on}(t) \cdot dt \tag{8.9}$$

$$\overline{P}_{off} = \frac{1}{T} \cdot \int_0^T E_{off}(t) \cdot dt \tag{8.10}$$

8.4 Semiconductor loss calculations for the three-level matrix converter topologies

The semiconductor loss models described in the previous sections were implemented using SABER to estimate the conduction and switching losses in the three-level matrix converter topologies. Since the semiconductor loss calculations were based on separate models, ideal switching devices were used in the simulation models. In this section, the semiconductor losses in each three-level matrix converter topology were calculated first. Then, the total semiconductor losses in the three-level matrix converter topologies are compared with the indirect matrix converter topology.

To determine the effects of having a higher number of power semiconductor devices and additional switching transitions in the modulation patterns on the semiconductor losses, external factors (e.g. load currents and supply voltages) that contribute to the semiconductor losses in the three-level matrix converter topologies were kept constant. During the simulation, the supply voltage was fixed at 240V. Then, based on (8.3) and (8.5), the conduction losses in a converter topology increase proportionally to the load current. Therefore, a constant torque load was considered in the loss calculations, where the load current (I_{load}) and load power factor were kept constant, 20A and 0.94 respectively. The switching frequency of the converter was fixed at 5kHz, because the switching losses are proportionate to the switching frequency. In the following loss calculations, a 200ms simulation time was chosen to accommodate sufficient number of supply and load frequency cycles in order to provide reasonable estimation of the average semiconductor losses in the three-level matrix converter topologies.

8.4.1 The three-level-output-stage matrix converter

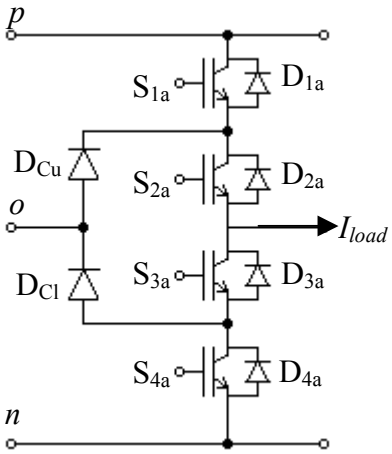
For the three-level-output-stage matrix converter, the semiconductor loss calculations for the rectification stage and the inversion stage were performed separately so that, for each stage, the redundant calculations can be minimized according to respective functionality. For example, by applying space vector modulation, the switching behaviour for each bi-directional switch in the rectification stage is the same for a set of

balanced three-phase supply voltages. This similarity enables the total semiconductor losses in the rectification stage to be estimated based on the semiconductor losses in one bi-directional switch. In the same way, the semiconductor losses in the inversion stage can be estimated based on the losses in one output phase leg since each output phase leg of the inversion stage is operated identically for a set of balanced three-phase output currents. Table 8.1 presents the data that is used in the semiconductor loss calculations for the three-level-output-stage matrix converter.

	Rectification stage	Inversion stage
Device	SK60GM123	SK40GB123
Manufacturer	SEMIKRON	SEMIKRON
V_{CE_sat}/(V)	1.4	1.2
R_{CE}/(mΩ)	26.6	53
V_{F0}/(V)	1.1	1
R_F/(mΩ)	15.11	53
E_{on}/(mWs)	6.5	4.4
E_{off}/(mWs)	5.25	3.6
V_{Ref}/(V)	600	600
I_{Ref}/(A)	50	30

Table 8.1: Data from the device datasheet

The conduction losses in the three-level-output-stage matrix converter was determined by substituting the sampled instantaneous currents of the conducting devices into the models using (8.3) and (8.5). For the rectification stage, the current always flows through two IGBTs and two diodes. The conducting devices in the inversion stage can be determined according to the on-state switching devices and the direction of the load current (I_{load}), as shown in Figure 8.4.



Switches on	Device conduct	
	$I_{load} > 0$	$I_{load} < 0$
S_{1a}, S_{2a}	S_{1a}, S_{2a}	D_{1a}, D_{2a}
S_{2a}, S_{3a}	D_{Cu}, S_{2a}	D_{Cl}, S_{3a}
S_{3a}, S_{4a}	D_{3a}, D_{4a}	S_{3a}, S_{4a}

Figure 8.4: The conducting devices in the inversion stage according to the on-state switching devices and the direction of the load current.

To determine the switching losses in each stage of the three-level-output-stage matrix converter, it is important to understand the commutation mechanism between the switches. For the rectification stage, the relative input voltage magnitude based four-step commutation strategy is applied to commutate current between the bi-directional switches. As discussed in Section 2.4.2.2, this commutation strategy relies on the knowledge of the relative magnitudes of the input voltages to determine the commutation sequence. Figure 8.5(a) shows the device gate timings for this four-step commutation strategy when commutating from S_{Aa} to S_{Ba} with $V_A > V_B$. This commutation sequence is based on the schematic diagram given in Figure 2.14, where I_L is the link current (I_{link}) of the three-level-output-stage matrix converter. If I_{link} is positive, the commutation will occur at t_1, resulting a hard turn-off in S_{Aa1} and a soft turn-on in S_{Ba1}. Conversely, if I_{link} is negative, commutation will happen at t_2, resulting a hard turn-on in S_{Ba2} and soft turn-off in S_{Aa2}. Table 8.2 summarizes the switching energy losses involved in the commutations between S_{Aa} and S_{Ba} for different link current polarities and the relative magnitudes of V_A and V_B. For the inversion stage, the commutation occurs based on the direction of I_{load}, as shown in Figure 8.6. As shown in Table 3.1, the switching states for S_{1a} and S_{2a} are always opposite to those for S_{3a} and S_{4a} respectively. As a result, if S_{1a} is the incoming switch, S_{3a} must be the outgoing switch.

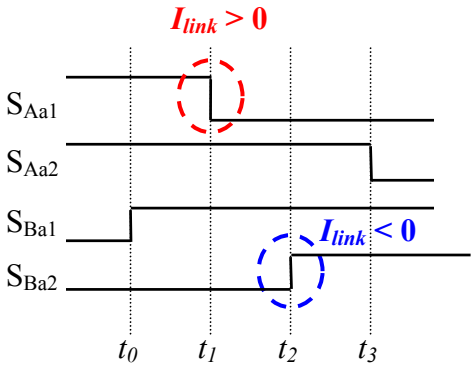
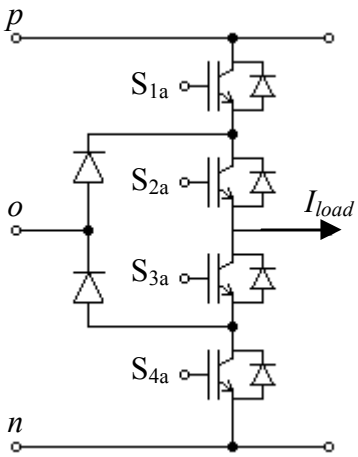


Figure 8.5: Timing diagram showing the commutation sequence of the bi-directional switches based on the four-step commutation strategy for the case where $V_A > V_B$

	$I_{link} > 0$		$I_{link} < 0$	
	$S_{Aa} \rightarrow S_{Ba}$	$S_{Ba} \rightarrow S_{Aa}$	$S_{Aa} \rightarrow S_{Ba}$	$S_{Ba} \rightarrow S_{Aa}$
$V_A > V_B$	$S_{Aa1} \Rightarrow E_{off}$ $S_{Ba1} \Rightarrow 0$	$S_{Aa1} \Rightarrow E_{on}$ $S_{Ba1} \Rightarrow 0$	$S_{Aa2} \Rightarrow 0$ $S_{Ba2} \Rightarrow E_{on}$	$S_{Aa2} \Rightarrow 0$ $S_{Ba2} \Rightarrow E_{off}$
$V_A < V_B$	$S_{Aa1} \Rightarrow 0$ $S_{Ba1} \Rightarrow E_{on}$	$S_{Aa1} \Rightarrow 0$ $S_{Ba1} \Rightarrow E_{off}$	$S_{Aa2} \Rightarrow E_{off}$ $S_{Ba2} \Rightarrow 0$	$S_{Aa2} \Rightarrow E_{on}$ $S_{Ba2} \Rightarrow 0$

Table 8.2: The switching energy losses for the commutations between S_{Aa} and S_{Ba}



	Switching loss energy	
	$I_{load} > 0$	$I_{load} < 0$
S_{1a} ↑	$S_{1a} \Rightarrow E_{on}$ $S_{3a} \Rightarrow 0$	$S_{1a} \Rightarrow 0$ $S_{3a} \Rightarrow E_{off}$
S_{1a} ↓	$S_{1a} \Rightarrow E_{off}$ $S_{3a} \Rightarrow 0$	$S_{1a} \Rightarrow 0$ $S_{3a} \Rightarrow E_{on}$
S_{2a} ↑	$S_{2a} \Rightarrow E_{on}$ $S_{4a} \Rightarrow 0$	$S_{2a} \Rightarrow 0$ $S_{4a} \Rightarrow E_{off}$
S_{2a} ↓	$S_{2a} \Rightarrow E_{off}$ $S_{4a} \Rightarrow 0$	$S_{2a} \Rightarrow 0$ $S_{4a} \Rightarrow E_{on}$

Figure 8.6: The switching losses in the inversion stage

Since the energy loss involved in soft switching is at least an order of magnitude less than for the hard switching [73], only the energy losses due to hard switching in the three-level-output-stage matrix converter topology were determined using the model given in equation (8.8). The semiconductor losses in the three-level-output-stage matrix converter are shown in Figures 8.7. Compared to the conduction losses in the rectification stage (*P_cond_rec*), the conduction losses in the inversion stage (*P_cond_inv*) are obviously higher, because:

- The inversion stage has more conducting devices (= 6) than the rectification stage (= 4) at any instant of time
- The on-state resistances, R_{CE} and R_F, for the IGBT modules in the inversion stage are higher than those for the rectification stage, as shown in Table 8.1. If the IGBT modules with smaller on-state resistances (e.g. $R_{CE} \approx 26\text{m}\Omega$ and $R_F \approx 15\text{m}\Omega$) are used in the inversion stage, the conduction loss can be reduced (e.g. *P_cond_inv* ≈ 160W at a voltage transfer ratio of 0.8).
- The load current (I_{load}) of the three-level-output-stage matrix converter is constant and continuous. Hence, the conducting devices in the inversion stage always experience conduction losses. Conversely, for the rectification stage, the link current (I_{link}) is discontinuous, as shown in Figure 8.8. This discontinuity is due to the use of small voltage vectors and zero voltage vectors. For example, when the switching state *ONN* (V_1) is applied, there is no current flowing through the DC-link '*p*'. As a result, the conducting devices in the upper DC-link of the rectification stage will not experience any conduction loss, as shown in Figure 8.8.

As shown in Figure 8.7, the conduction losses in the rectification stage decreases linearly as the voltage transfer ratio reduces. This decrease is because the small voltage vectors and zero voltage vectors become more dominant in synthesizing the reference output vector. Therefore, there are more discontinuities in the DC-link current, resulting lower average link current as well as lower conduction losses in the rectification stage.

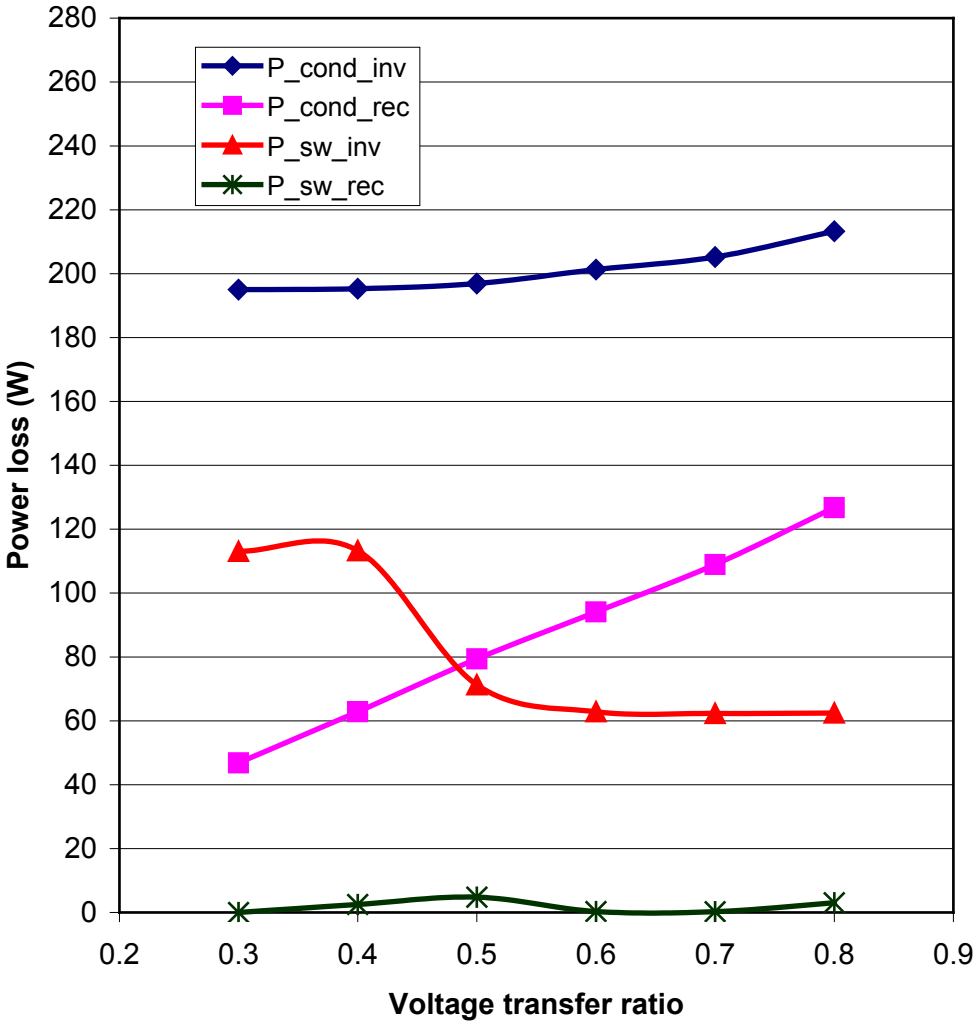


Figure 8.7: The semiconductor losses in the three-level-output-stage matrix converter

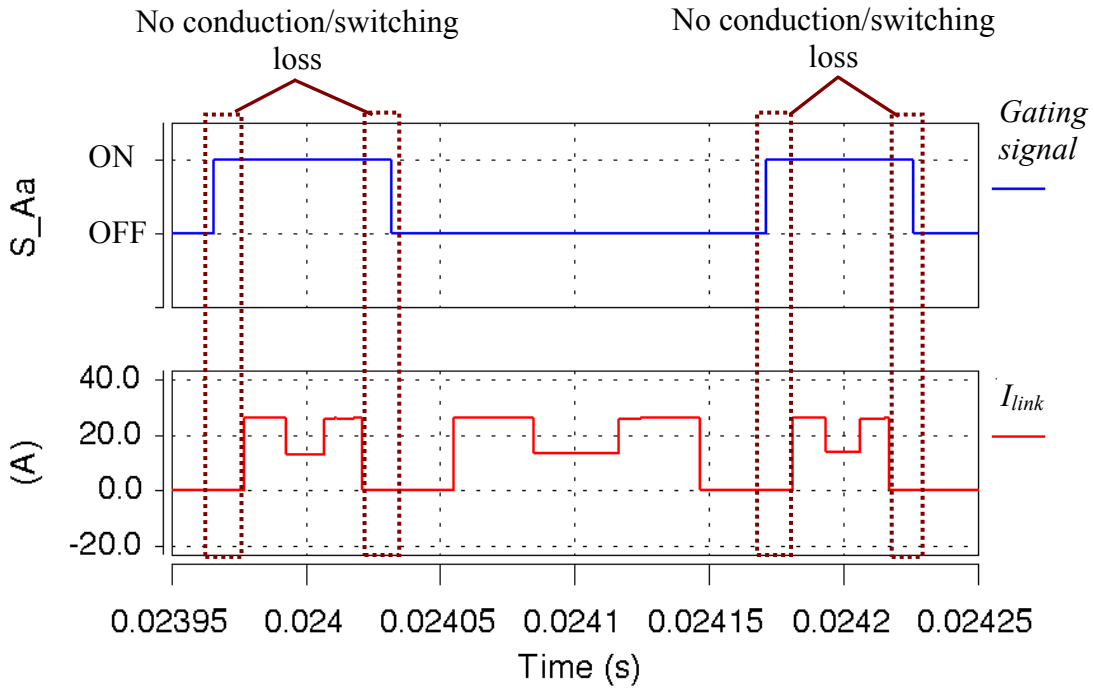


Figure 8.8: The lossless regions for the conducting devices in the rectification stage

Referring to Figure 8.7, the switching losses in the inversion stage (*P_sw_inv*) are much higher than that for the rectification stage (*P_sw_rec*). As discussed earlier, the load currents of the three-level-output-stage matrix converter are continuous. Hence, the switching devices in the inversion stage always commutate when the voltage and current are nonzero. The increase of switching losses in the inversion stage, when the voltage transfer ratio is lower than 0.5, is due to the increased number of switching transitions in the modulation pattern for the inversion stage at low modulation indexes (Triangle T1), as shown in Table 5.4. Conversely, due to the discontinuities in the link current, the bi-directional switches in the rectification stage often commutate when the link current is zero (soft commutation), as shown in Figure 8.8. As a result, the switching losses in the rectification stage are comparatively low. For the three-level-output-stage matrix converter, the conduction losses in the inversion stage are obviously the main losses. In order to reduce the total semiconductor losses in this topology, the IGBT modules with lower on-state resistances (R_{CE} and R_F) should be used to construct the inversion stage.

8.4.2 The indirect three-level sparse matrix converter

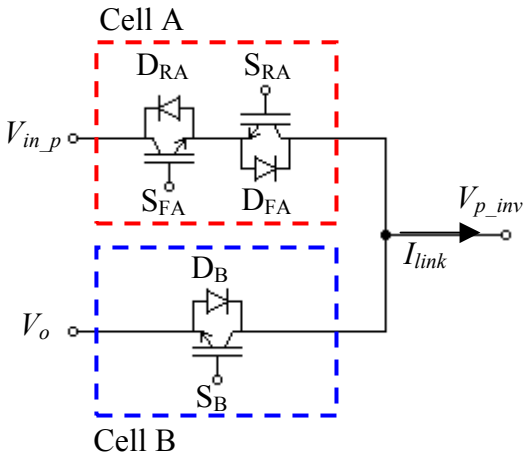
For the indirect three-level sparse matrix converter, the semiconductor loss calculations for the rectification stage and neutral-point commutator were performed together while the semiconductor losses in the inversion stage were estimated separately. Table 8.3 presents the relevant data extracted from the device datasheet for this process.

	Rectification stage	Neutral – point commutator	Inversion stage
Device	SK60GM123	SK40GB123	SK35GB126T
Manufacturer	SEMIKRON	SEMIKRON	SEMIKRON
V_{CE_sat}/(V)	1.4	1.2	0.8
R_{CE}/(mΩ)	26.6	53	25.6
V_{F0}/(V)	1.1	1	1.15
R_F/(mΩ)	15.11	53	15.4
E_{on}/(mWs)	6.5	4.4	7.75
E_{off}/(mWs)	5.25	3.6	4
V_{Ref}/(V)	600	600	600
I_{Ref}/(A)	50	30	35

Table 8.3: Relevant data from the device datasheet.

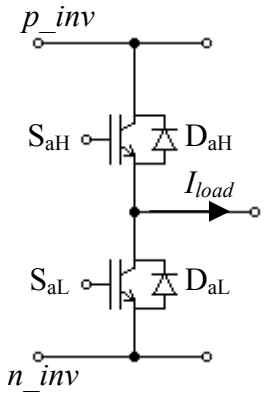
As discussed in Section 6.3, the rectification stage and neutral-point commutator are always switched to supply the required voltage levels to the inversion stage's input terminals (*p_inv* and *n_inv*). Hence, the conduction and switching losses in the rectification stage and neutral-point commutator are affected by the modulation of the inversion stage. Figure 8.9 can be used to explain the conduction losses in the upper DC-link of the rectification stage and neutral-point commutator. V_{in_p} is the input phase voltage (V_{Ao}, V_{Bo} or V_{Co}) applied to the DC-link point '*p*'; V_o is the neutral-point voltage at the DC-link middle point '*o*' and V_{p_inv} is the voltage applied to the inversion stage's terminal '*p_inv*'. If V_{in_p} is required by the inversion stage, the bi-directional switch of

the rectification stage (Cell A) is turned on, giving $V_{p\_inv} = V_{in\_p}$. Based on the direction of the DC-link current (I_{link}), the conducting devices are determined and the conduction losses in the rectification stage and neutral-point commutator can be estimated. For the inversion stage, the conducting devices can be determined according to the on-state switching devices and the direction of the load current (I_{load}), as shown in Figure 8.10.



Switches On	V_{p_inv}	Device conduct	
		$I_{link} > 0$	$I_{link} < 0$
S_{FA}, S_{RA}	$= V_{in\_p}$	S_{FA}, D_{FA}	S_{RA}, D_{RA}
S_B	$= V_o$	D_B	S_B

Figure 8.9: The conducting devices in the upper DC-link of the rectification stage (Cell A) and the neutral-point commutator (Cell B).



Switches on	Device conduct	
	$I_{load} > 0$	$I_{load} < 0$
S_{aH}	S_{aH}	D_{aH}
S_{aL}	D_{aL}	S_{aL}

Figure 8.10: The conducting devices in the inversion stage.

For the indirect three-level sparse matrix converter, the switching losses in the rectification stage and neutral-point commutator can be estimated based on the device current commutation. The current commutation between the bi-directional switches in the rectification stage is identical to the three-level-output-stage matrix converter topology, as discussed in the Section 8.4.1. However, to commutate current between the bi-directional switches in the rectification stage and the unidirectional switches in the neutral-point commutator, a three-step relative voltage magnitude based commutation strategy, discussed in Section 7.2.2.1, is applied. Figure 8.11 shows the device gate timings for this three-step commutation strategy when commutating from the rectification stage (Cell A) to the neutral-point commutator (Cell B). The commutation sequence is derived based on the upper DC-link voltage (V_{in_p}) of the rectification stage and the neutral-commutator voltage (V_o) shown in Figure 8.9, where V_{in_p} is larger than V_o because the rectification stage is always modulated to supply positive voltage level to the DC-link point '*p*'. If the DC-link current (I_{link}) is positive, the commutation will occur at t_0, resulting a hard turn-off in S_{FA}. Conversely, if I_{link} is negative, commutation will happen at t_1, resulting a hard turn-on in S_B and soft turn-off in S_{RA}. Table 8.4 summarizes the switching energy losses involved in the commutations between the switches for the upper DC-link of the rectification stage and the neutral-point commutator for different link current polarities. For the inversion stage, the hard and soft switching of the devices can be determined according to the direction of the load current, as shown in Figure 8.12.

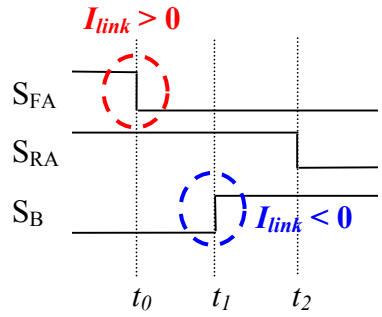
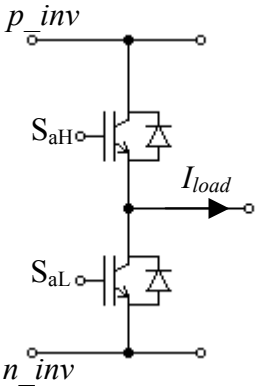


Figure 8.11: Timing diagram showing the commutation sequence for the upper DC-link of the rectification stage and neutral-point commutator based on the three-step current commutation strategy.

	$I_{link} > 0$		$I_{link} < 0$	
	Cell A → Cell B	Cell B → Cell A	Cell A → Cell B	Cell B → Cell A
$V_{in\_p} > V_o$	$S_{FA} \Rightarrow E_{off}$	$S_{FA} \Rightarrow E_{on}$	$S_{RA} \Rightarrow 0$ $S_B \Rightarrow E_{on}$	$S_{RA} \Rightarrow 0$ $S_B \Rightarrow E_{off}$

Table 8.4: The switching losses in the rectification stage and neutral-point commutator



	Switching loss energy	
	$I_{load} > 0$	$I_{load} < 0$
S_{aH} ↑	$S_{aH} \Rightarrow E_{on}$ $S_{aL} \Rightarrow 0$	$S_{aH} \Rightarrow 0$ $S_{aL} \Rightarrow E_{off}$
S_{aH} ↓	$S_{aH} \Rightarrow E_{off}$ $S_{aL} \Rightarrow 0$	$S_{aH} \Rightarrow 0$ $S_{aL} \Rightarrow E_{on}$

Figure 8.12: The switching losses in the inversion stage

The conduction and switching losses in the indirect three-level sparse matrix converter are shown in Figures 8.13. With constant and continuous load current, the conduction losses in the inversion stage remain constant for different voltage transfer ratios because, at any instant, there is always one switch or one diode conducting for each output phase leg. In contrast, the conduction losses in the rectification stage decrease linearly as the voltage transfer ratio reduces. This loss profile is because the neutral-point commutator is connected to the inversion stage more frequently in order to generate the small voltage vectors, which become dominant in synthesizing the reference output voltage vector. Therefore, the conduction losses in the neutral-point commutator increase while the conduction losses in the rectification stage decrease. However, when the voltage transfer ratio is less than 0.5, the use of zero voltage vectors causes discontinuities in the link current, resulting lower average link current as well as lower conduction loss in the neutral-point commutator and rectification stage.

The switching losses in the indirect three-level sparse matrix converter are also shown in Figure 8.13. When the indirect three-level sparse matrix converter generates the small voltage vectors, the input line-to-neutral point voltages are connected to the inversion stage input terminals, reducing the voltage stresses across the switch devices. As a result, the switching losses in the inversion stage decrease when the voltage transfer ratio gets smaller. However, due to the increased number of switching transitions in the modulation patterns at low modulation indexes (Table 6.7), the switching losses in the inversion stage increase significantly when the voltage transfer ratio is less than 0.5. Unlike the three-level-output-stage matrix converter, the use of small voltage vectors in the indirect three-level sparse matrix converter does not cause the link current to be discontinuous. Therefore, there are switching losses in the rectification stage of the indirect three-level sparse matrix converter. Nevertheless, at low modulation indexes, the use of zero voltage vectors causes discontinuities in the link current. As a result, the switching losses in the rectification stage are lower when the voltage transfer ratio is less than 0.5. For the indirect three-level sparse matrix converter, there is no switching loss in the neutral-point commutator because the link current always flows in the positive direction. As shown in Table 8.4, only the bi-directional switches experience switching losses for the positive DC-link current.

8.4.3 Comparison of semiconductor losses between the three-level matrix converters and the indirect matrix converter

To determine the topology that experiences the most semiconductor losses, Figure 8.14 shows the total semiconductor losses comparison between the three-level matrix converter topologies and the indirect matrix converter topology for different voltage transfer ratios. Among these topologies, the three-level-output-stage matrix converter obviously suffers the highest semiconductor losses due to high conduction losses in the inversion stage. The conduction losses can be reduced using the IGBT modules with lower on-state resistances, as discussed in section 8.4.1.

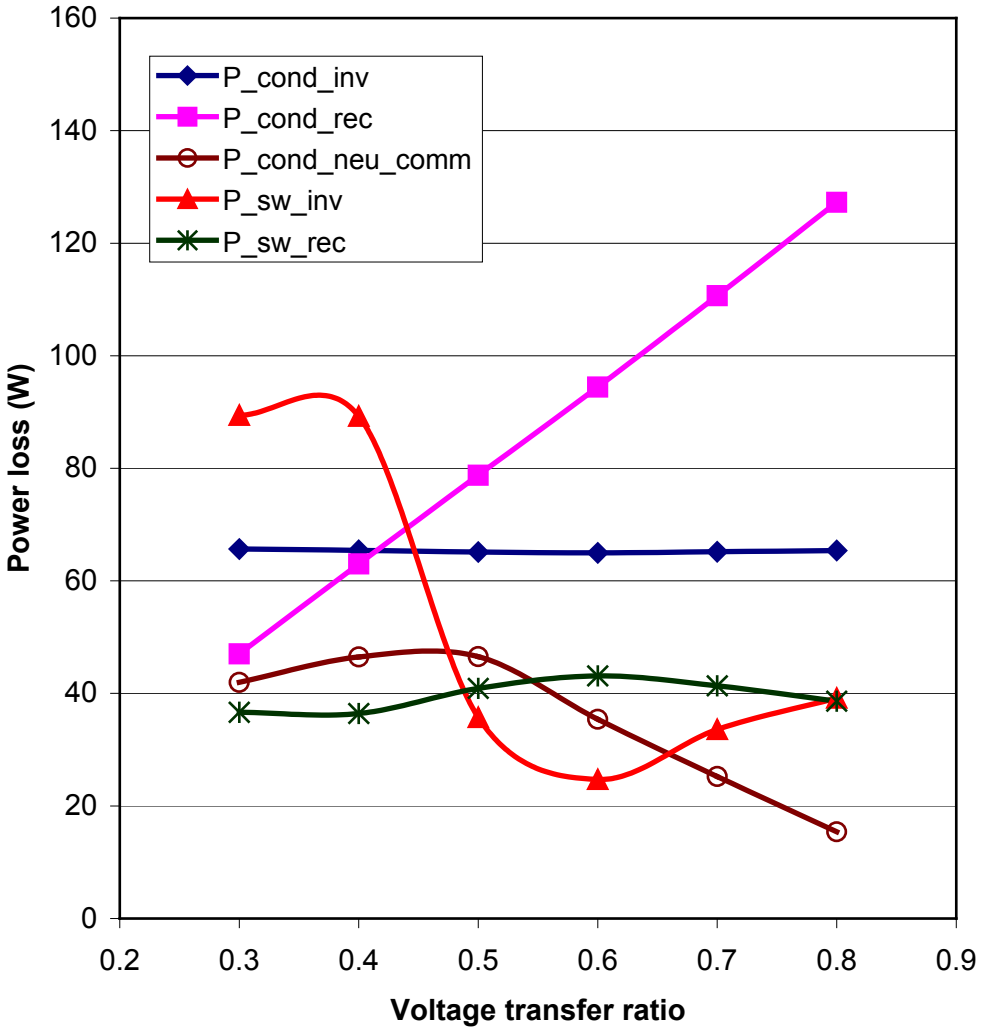


Figure 8.13: The semiconductor losses in the indirect three-level sparse matrix converter

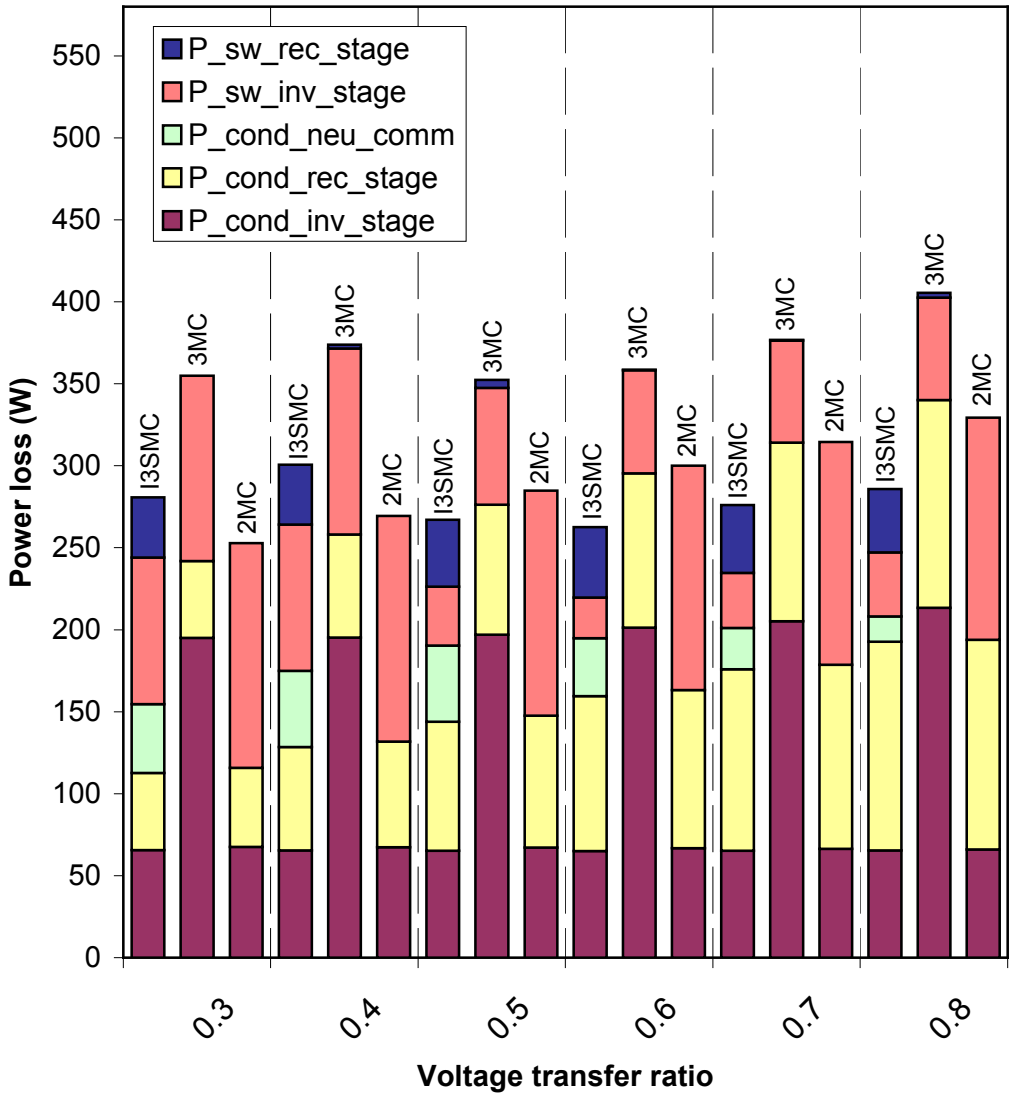


Figure 8.14: The semiconductor losses comparison at different voltage transfer ratios between the indirect three-level sparse matrix converter (I3SMC), the three-level-output-stage matrix converter (3MC) and indirect matrix converter (2MC)

Despite having a higher number of power semiconductor devices and additional switching transitions in the modulation patterns, the semiconductor losses in the indirect three-level sparse matrix converter are lower than those for the indirect matrix converter at high voltage transfer ratios (> 0.5). This is due to the lower switching losses in the indirect three-level sparse matrix converter. Using the input line-to-neutral point voltages to generate the small voltage vectors, the voltage stresses across the switching devices in the inversion stage of the indirect three-level sparse matrix converter are reduced. Besides that, referring to the switching patterns shown in Tables 6.8 and 6.9, there is no switching in the inversion stage for certain change of switching states in the switching pattern. For example, referring to T3 of S1 shown in Table 6.8, *PPO*, *PPN* and *OON* actually represent the same switching state (*PNN*) in the inversion stage. As a result, the switching losses in the inversion stage of the indirect three-level sparse matrix converter are lower than those for the indirect matrix converter that uses the full input line-to-line voltages. However, due to the increased number of switching transitions in the modulation patterns at low modulation indexes, the switching losses in the indirect three-level sparse matrix converter increase significantly, resulting higher semiconductor losses than the indirect matrix converter at low voltage transfer ratios.

Due to low semiconductor losses in the indirect three-level sparse matrix converter, the efficiency of this converter is the highest at high voltage transfer ratios (>0.5), as shown in Figure 8.15. However, at low voltage transfer ratios (< 0.5), the increase of semiconductor losses in the indirect three-level sparse matrix converter inevitably lowers the efficiency, causing this converter trailing behind the indirect matrix converter. The high semiconductor losses in the three-level-output-stage matrix converter make the efficiency of this converter the lowest among three converter topologies. In order to improve the efficiency, the semiconductor losses in the three-level-output-stage matrix converter must be reduced particularly the conduction losses in the inversion stage.

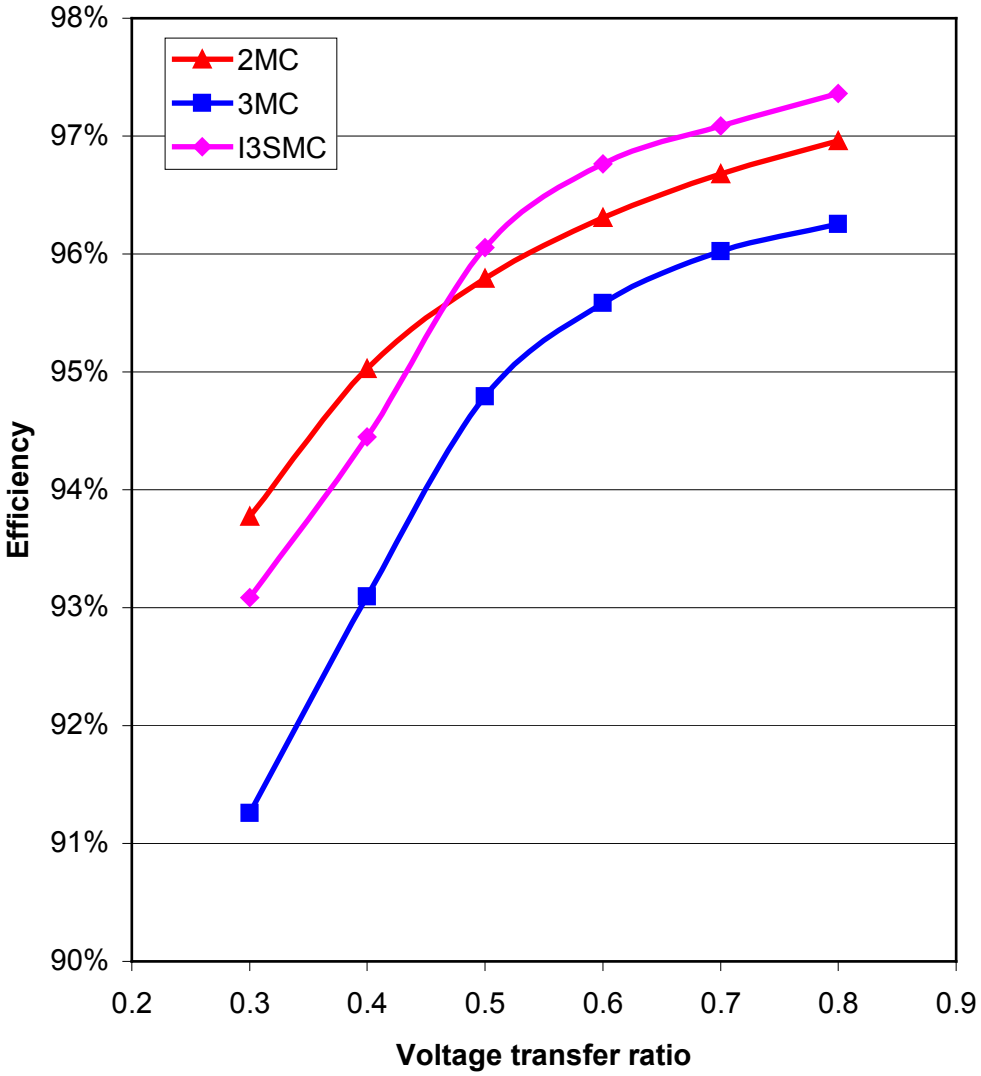


Figure 8.15: Efficiency comparison of the converters against the voltage transfer ratio at a load current of 20A.

8.5 Conclusions

In this chapter an explanation of the conduction and switching losses in a power converter has been given. Simulation models have been developed to estimate the semiconductor losses in each three-level matrix converter topology. To effectively determine the losses the semiconductor device data of the devices used in the prototypes were incorporated into the loss models.

The distributions of the semiconductor losses in the three-level matrix converter topologies were analyzed for different voltage transfer ratios under constant load current conditions. The high number of power semiconductor devices in the three-level matrix converter topologies and the additional switching transitions in the modulation patterns have been shown to have an impact on the semiconductor losses.

In the semiconductor losses comparison, the three-level-output-stage matrix converter has the highest semiconductor losses, resulting lower efficiency when compared to the indirect matrix converter. In contrast, the indirect three-level sparse matrix converter has been shown to have higher efficiency than the indirect matrix converter at high voltage transfer ratios, giving the converter an advantage since the indirect three-level sparse matrix converter has a better output performance than the indirect matrix converter.

Chapter 9

9.1 Conclusions

With ongoing research efforts, the matrix converter technology is developing as a promising technique for direct AC – AC power conversion. As discussed in Chapter 2, the matrix converter topology has the following features that are desirable in a range of applications:

- adjustable input displacement factor, irrespective of the load
- the capability of regeneration (Four-quadrant operation)
- high quality input and output waveforms
- the lack of bulky and limited lifetime energy storage components

In order to further increase the attractiveness of matrix converters, the multilevel concept has been integrated into the matrix converter topology to improve the output waveform quality. Having the ability to generate multilevel output voltages, the multilevel matrix converter topology is able to generate better quality output waveforms than the conventional matrix converter topology in terms of harmonic content, but at the cost of higher number of power semiconductor devices and a more complicated modulation strategy.

In this work a simpler multilevel matrix converter topology, the indirect three-level sparse matrix converter, has been proposed. This multilevel matrix converter topology is the hybrid combination between a simplified three-level neutral point clamped voltage source inverter and an indirect matrix converter topology. Despite having a simpler circuit configuration, the indirect three-level sparse matrix converter is able to generate multilevel output voltages.

In order to assess the performance of the indirect three-level sparse matrix converter, the converter was compared with the indirect matrix converter and the three-level-output-

stage matrix converter. The three-level-output-stage matrix converter is a multilevel matrix converter topology that applies a conventional three-level neutral point clamped voltage source inverter concept to the inversion stage of an indirect matrix converter topology. This converter has a complicated circuit configuration but is able to generate switching states that are not achievable with the indirect three-level sparse matrix converter. The performance comparison between the indirect three-level sparse matrix converter and the three-level-output-stage matrix converter showed the superior waveform quality achievable by the indirect three-level sparse matrix converter.

In Chapters 5 and 6, space vector modulation strategies have been derived for each three-level matrix converter topology. The simulation results clearly show the effectiveness of the modulation strategy in controlling the three-level matrix converters in order to generate multilevel output voltages as well as maintain the input capacitor voltages and generate a set of balanced, sinusoidal input currents despite the presence of neutral-point current. Compared to the indirect matrix converter, the three-level matrix converter topologies obviously generate better quality output waveforms in term of harmonic content. In addition, due to the use of multiple smaller voltages, the distortion in the load currents for the three-level matrix converters is lower than those for the indirect matrix converter, giving an advantage to the three-level matrix converter when the load provides very low inductance.

Even though the three-level-output-stage matrix converter is able to achieve additional switching states, compared to the indirect three-level sparse matrix converter, the output performances for both multilevel topologies are comparable, giving the indirect three-level sparse matrix converter an advantage because of the simpler circuit configuration. The higher switching frequency harmonics in the unfiltered input currents for the indirect three-level sparse matrix converter at low voltage transfer ratios is probably a disadvantage but the application of a low-pass filter is sufficient to filter out these undesirable switching frequency harmonics.

In order to validate the simulation results, the three-level matrix converter prototypes were constructed and tested at realistic power levels. The experimental results in Chapter 7 clearly correspond well to the simulation results shown in Chapters 5 and 6, proving the abilities of the three-level matrix converters to generate better quality output waveforms than the indirect matrix converter as well as the ability of the indirect three-

level sparse matrix converter to generate comparable quality output waveform to the three-level-output-stage matrix converter

After analysing the performance, it is important to investigate the efficiency of the indirect three-level sparse matrix converter in order to evaluate the industrial potential of this topology. In Chapter 8, the semiconductor losses in the converter were calculated using simulation models and then compared to both the conventional indirect matrix converter and the three-level-output-stage matrix converter. Due to high number of power semiconductor devices and additional switching transitions in the modulation patterns, the semiconductor losses in the three-level-output-stage matrix converter are the highest, leading to the lowest efficiency among the three topologies. In contrast, the indirect three-level sparse matrix converter has comparable losses to the indirect matrix converter. Therefore, the indirect three-level sparse matrix converter has efficiency similar to the indirect matrix converter, giving the converter good potential in industrial and aerospace applications.

9.2 Future work

The following are some of the interesting topics in which further research can be undertaken in order to develop the indirect three-level sparse matrix converter topology:

- Implementation of the indirect three-level sparse matrix converter as a motor drive
- Derivation of alternative modulation strategies that can further exploit the potential of the converter
- Implementation of the indirect three-level sparse matrix converter with unbalanced voltage supply to check on the performance and reliability

The work carried out in this project has resulted in several conference papers, which are listed in appendix C.

Appendix A

Parameters Used

Simulation analysis

The Indirect Matrix Converter (Chapter 2):

- Input:
  - Input voltages, V_{in_rms} = 240V
  - Input frequency, f_i = 50Hz
- Input filter:
  - Inductor, L_f = 0.633mH
  - Capacitor, C_f = 10μF
- Load:
  - Resistor, R_L = 20Ω
  - Inductor, L_L = 10mH
- Output:
  - Output voltage, V_{out_peak} = 270V
  - Output frequency, f_{out} = 30Hz
- Switching frequency, f_{sw} = 5kHz

The three-level neutral-point-clamped voltage source inverters (Chapters 3 and 4):

- Voltage source, V_{DC} = 250V
- Load:
  - Resistor, R_L = 20Ω
  - Inductor, L_L = 10mH
- Output voltages:
  - At $m_u = 0.9$, V_{out_peak} = 259V
  - At $m_u = 0.4$, V_{out_peak} = 115V
- Output frequency, f_{out} = 30Hz
- Switching frequency, f_{sw} = 5kHz

The three-level matrix converter topologies (Chapters 5 and 6):

- Input:
  - Input voltages, V_{in_rms} = 240V
  - Input frequency, f_i = 50Hz
- Input filter:
  - Inductor, L_f = 0.633mH
  - Capacitor, C_f = 10μF
- Load:
  - Resistor, R_L = 20Ω
  - Inductor, L_L = 10mH
- Output:
  - At a high modulation index, V_{out_peak} = 270V
  - At a low modulation index, V_{out_peak} = 135V

  - Output frequency, f_{out} = 30Hz
- Switching frequency, f_{sw} = 5kHz

Experimental Validation

- Input:
  - Supply voltage, V_{in_rms} = 156V
  - Supply frequency, f_i = 50Hz
- Input filter:
  - Inductor, L_f = 0.633mH
  - Capacitor, C_f = 10μF
- Load:
  - Resistor, R_L = 20Ω
  - Inductor, L_L = 10mH
- Output:
  - At a high modulation index, V_{out_rms} = 125V
  - At a low modulation index, V_{out_rms} = 62V
  - Output frequency, f_{out} = 30Hz
- Switching frequency, f_{sw} = 5kHz

Appendix B

List of Symbols

Notation	Meaning
V	Volt
A	Ampere
Ω	Ohm
H	Henry
F	Farad
Hz	Hertz
^{o}C	Degree Celsius
ϕ	Phase
AC	Alternating current
DC	Direct current
IM	Induction motor
LC	Inductor plus capacitor
RL	Resistor plus inductor
GTO	Gate turn off thyristor
IGBT	Insulated gate bipolar transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
IGCT	Integrated gate commutated thyristor
MCT	MOS controlled thyristor
INV	Inversion stage
REC	Rectification stage
NC	Neutral-point commutator
RMS	Root mean square

NPC VSI	Neutral-point-clamped voltage source inverter
SNPC VSI	Simplified neutral-point-clamped voltage source inverter
I3SMC	Indirect three-level sparse matrix converter
3MC	Three-level-output-stage matrix converter
2MC	Indirect matrix converter
THD	Total harmonic distortion
V_{DC}	DC voltage supply
s	Load neutral-point
z	Supply voltage neutral-point
p, n	DC-link terminals
p_inv, n_inv	Inverter input terminals
o	DC-link middle point
ω_o	Frequency of the output voltage
ω_i	Frequency of the input voltage
f_{sw}	Switching frequency
f_i	Frequency of the input voltage
f_{out}	Frequency of the output voltage
f_{cutoff}	Cutoff frequency of the input filter
ΔV	Voltage difference
ΔV_L	Maximum voltage drop across the filter inductor
V_A, V_B, V_C	Three phase input voltages
V_{AB}, V_{BC}, V_{CA}	Three line-to-line input voltages
V_a, V_b, V_c	Three output line-to-supply neutral voltages
V_{ab}, V_{bc}, V_{ca}	Three output line-to-line voltages
V_{as}, V_{bs}, V_{cs}	Three output line-to-load neutral voltages
V_{ao}, V_{bo}, V_{co}	Three output line-to-DC-link midpoint voltages
V_{pz}, V_{nz}	The potentials at the DC-link terminals referenced to the supply neutral

V_{po}, V_{no}	The potentials at the DC-link terminals referenced to the DC-link midpoint
V_{po_avg}, V_{no_avg}	Averages of V_{po} and V_{no}
V_{pn}	DC-link voltage
V_{pn_avg}	Average DC-link voltage
V_{in_p}, V_{in_n}	Input phase voltage applied to the DC-link terminals, *p* and *n*
V_{p_inv}, V_{n_inv}	Potentials applied to the inverter input terminals, *p_inv* and *n_inv*
V_{in_rms}	RMS amplitude of the input voltage
V_{out_peak}	Peak amplitude of the output voltage
V_{out_rms}	RMS amplitude of the output voltage
V_o	Neutral-point voltage at the DC-link middle point '*o*'
V_i	Input voltages
V_R	Rated voltage supply
v_{CE}	Instantaneous collector-to-emitter saturation voltage of the IGBT
V_{CE_sat}	Forward voltage drop across the IGBT when the collector current, i_{C_igbt}, is small
V_{CE}	Collector-to-emitter voltage of the IGBT
V_{CEF}	Forward blocking voltage of the IGBT
$\overline{V}_{out}$	Reference output voltage vector
V_{om}	The magnitude of the reference output voltage vector
V_{F0}	Forward voltage drop across the diode
i_A, i_B, i_C	Three phase input currents
i_a, i_b, i_c	Three phase output currents
i_{ab}, i_{bc}, i_{ca}	Three output line-to-line currents
I_R	Rated input current
I_L	Load current
i_o	Neutral-point current
i_{C_igbt}	Instantaneous collector current of the IGBT

I_C	Collector current of the IGBT
I_{rr}	Reverse recovery current
I_{load}	Load current
I_{link}	DC-link current
$\bar{I}_{in}$	Reference input current vector
I_{im}	The magnitude of the reference input current vector
I_s	Secondary current of the voltage and current transducers
i_F	Forward current of the diode
φ_i	The displacement angle of the input currents with respect to the input voltages
θ_o	The direction of the reference output voltage vector
θ_{out}	The angle of the reference output vector within the sector
θ_i	The direction of the reference input current vector
θ_{in}	The angle of the reference input vector within the sector
m_R	Modulation index of the rectification stage
m_I	Modulation index of the inversion stage
m_u	Modulation index of the three-level voltage source inverter
C_f	Input filter capacitor
C_C	Clamp capacitor
L_f	Input filter inductor
L_L	Inductor load
R_C	Clamp resistor
R_d	Damping resistor
R_L	Resistor load
R_p	Primary resistor for the voltage transducer
R_m	Measurement resistor for the voltage and current transducers
R_{CE}	On-state resistance of the IGBT
R_F	On-state resistance of the diode
d_γ, d_δ, d_0	Duty cycles for the current vectors I_γ, I_δ, I_0

d_α, d_β, d_0	Duty cycles for the voltage vectors V_α, V_β, V_0
d_x, d_y, d_z	Duty cycles for the selected active vectors V_x, V_y, V_z
$P_{cond\text{-}igbt}$	Conduction loss of the IGBT
$P_{cond\text{-}d}$	Conduction loss of the diode
P_p	Peak amplitude of the switching power loss
E_{on}	Turned-on switching loss energy of the IGBT
E_{off}	Turned-off switching loss energy of the IGBT
E_{SWR}	Rated switching loss energy
T_{SW}	Switching period
t_{on}	Turned-on switching time for the IGBT
t_{off}	Turned-off switching time for the IGBT
t_{rr}	Reverse recovery period for the diode

Appendix C

Published Papers

The work has resulted in the following papers having been published:

I. C. Klumpner, M. Lee and P. Wheeler, "A new three-level sparse indirect matrix converter", *Proceedings of IEEE Industrial Electronics Conference*, pp.1902 – 1907, Nov. 2006.

II. M. Y. Lee, P. W. Wheeler and C. Klumpner, "A new modulation method for the three-level-output-stage matrix converter," *Proceedings of Power Conversion Conference*, pp. 776 – 783, April 2007.

III. M. Y. Lee, P. Wheeler and C. Klumpner, " Modulation method for the three-level-output-stage matrix converter under balanced and unbalanced supply condition," *Proceedings of European Power Electronics and Applications Conference*, pp. 1 – 10, Sept. 2007.

IV. M. Y. Lee, C. Klumpner and P. Wheeler, " Experimental evaluation of the indirect three-level sparse matrix converter," *Proceedings of Power Electronics, Machines and Drives*, pp. 50 – 54, April 2008.

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