Direct Energy Converter Controllers for Switched Reluctance Motor Operation

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Abstract

There is increasing demand for simple motor drives offering high reliability and fault tolerance in applications such as the aerospace actuator industry, with the development of 'more electric aircraft'.

This thesis presents a motor drive employing a switched reluctance motor, the novel single sided matrix converter, and a novel double band hysteresis based control scheme for control of the converter, implemented using a field programmable gate array (FPGA).

The single sided matrix converter is a direct energy converter, capable of supplying unidirectional currents from a multiphase AC voltage source. It is suitable for driving motors such as the switched reluctance motor and trapezoidal permanent magnet direct current (PMDC) machine. The use of a direct energy converter removes the DC link energy storage element usually found in switched reluctance motor drives, making practical implementation possible without the use of electrolytic capacitors. This is a requirement for applications in the aerospace industry. Controller implementation without the use of a digital signal processor (DSP) makes application of the converter in the aerospace industry easy as specific DSP approval is not required.

Simulations of the converter operation are presented, followed by a description of the practical implementation of the novel converter and control schemes. Practical results demonstrate the reliable operation of the converter, driving both switched reluctance and trapezoidal PMDC machines.

The work has been published in three conference papers, presenting both the topology of the drive and the applied control schemes, as well as analysing the fault tolerant capabilities of the drive.

Acknowledgements

I would like to thank Dr Keith Bradley for his wide ranging expertise, encouragement and trusting belief in me throughout this PhD. I would also like to thank Dr Pat Wheeler for his assistance with the hardware design, Xiaoyan Huang for her help with the PMDC machine, and Kevin Last, Colin Blackburn, Matt Cooper and the other workshop staff for the mechanical and electrical help needed in producing and testing the single sided matrix converter and setting up the motor loading system.

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Key to Acronyms, Abbreviations & Terminology

Notation	Meaning
ω	Rotational Speed
θ	Angular position
(V,I)A,B,C	Input Phase (Voltages, Currents)
(V,I)u,v,w,x,y	Output Phase (Voltages, Currents)
A, B, C, U	Required Input Phase Connections
	(A,B,C) with polarity (U)
A/D	Analogue to digital Converter
AC	Alternating Current
CARAD	Civil Aircraft and Technology Demonstration
D	Current Direction of Change
DB	Double Band
DC	Direct Current
DSP	Digital Signal Processor
DTI	Department of Trade and Industry
EHA	Electro hydraulic Actuator
EMA	Electro Mechanical Actuator
EMF	Electro Motive Force
EPSRC	Engineering and Physical Sciences Research Council
FPGA	Field Programmable Gate Array
I,i	Current
IC	Integrated circuit
IGBT	Insulated Gate Bipolar Transistor
IPC	Association Connecting Electronics Industries
L	Inductance
Linear SRM	Magnetically Linear, Non Saturating,
	Rotating Switched Reluctance Motor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board

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Notation	Meaning
PMDC	Permanent Magnet Direct Current
PWM	Pulse Width Modulation
R	Resistance
RL	Resistive and Inductive
rms	Root Mean Square
rpm	Revolutions per Minute
SAa, SBa, SCa	SSMC Output Current High Side Switches connecting to input phase A, B, C respectively
SAb, SBb, SCb	SSMC Output Current Low Side Switches connecting to input phase A, B, C respectively
SATOW	Surface Actuation of Thin and Optimised Wings
SB	Single Band
sec	Seconds
Scope	Oscilloscope
SR	Switched Reluctance (Motor)
SSMC	Single Sided Matrix Converter
SVM	Space Vector Modulation
t	Time
U1,U2,U3,U4	Output Current with respect to Hysteresis Band Logic Signals
V	Voltage
V+3, V+2, V+1	Positive Input Voltage Level Bands
V0	Voltage Level zero
V-1, V-2, V-3	Negative Input Voltage Level Bands
V1,V2,V3	Required Voltage Level (without polarity)
VHDL	Very-High-Speed Integrated Circuit Hardware Description Language
X, Y, Z, A, B, C	Input Voltage State Logic Signals
x-x	Switched Reluctance Motor Pole Numbers

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Chapter 1

Introduction

In many applications today simple, reliable, high performance motor drives are desired. This need is clear in the safety critical aerospace actuator industry more than any other, where there is considerable interest in replacing the conventional centralised hydraulic flight control system with electrically powered actuators located near to the control surface being moved [1] [2] [3]. Whilst simple systems may be the aim, simplicity rarely allows high performance, or optimisation of efficiency. The approach is therefore to design a system which uses simple elements where possible, and highly reliable elements where it is not possible. Unfortunately however, it is common that the more complicated a system is, the less reliable it becomes, as it has more potential failure modes. A third level to the systems design approach is therefore adopted, which encompasses fault tolerance and redundancy [4]. An analysis is performed to evaluate the local systems ability to continue functioning after the failure of an element within it, albeit in a non-ideal or lesser efficient way, in order that the larger system can continue to function until repairs can be made [5].

In the work of this thesis, the above design approach has been implemented in specifying a motor drive suitable for use in operability critical applications, such as the aerospace actuator industry.

One of the simplest and most reliable forms of motor is the switched reluctance (SR) motor

[6], which makes it highly suitable for use in aircraft actuators [7]. This motor has a simple construction, with a laminated rotor free of both windings and magnets. The stator is also a simple design, constructed again of steel laminations, and with a small number of poles carrying isolated phase windings. This simple construction makes the motor cheap to produce, and the simple laminated rotor makes it highly mechanically robust and suitable for operation over a very wide speed range. The isolated phase windings make this motor highly fault tolerant, as with the right numbers of poles and phases, it can continue to spin with a fault on one phase, without a danger of the fault affecting other phases. The switched reluctance motor has been acknowledged by Boeing as being the preferred motor for many aerospace applications, due to the built in redundancy, and the fundamental magnetic and electrical isolation of the design [8]. The absence of permanent magnets from the motor is also seen as an advantage, as there are no demagnetisation concerns at higher temperatures. A 25kW 16,000rpm switched reluctance motor was developed for an aerospace actuator by Glasgow University, with the design being favoured due to the inherent fault tolerant advantages [9] .

The conventional way to drive a switched reluctance motor is using a simple asymmetric half-bridge switching converter, as was used in the Glasgow project [9]. This connects a DC voltage source in the required direction across the motor phases in alternate directions at high frequency, in order to produce the required change in current level. The switching is done using solid state power electronic switches such as MOSFET's or IGBT's. Other converter topologies have been proposed and are used where only low power or low speed operation is required, or where larger phase numbers are present [10]. Circuit topologies have also been developed that are better suited to high speed operation [11] [12]. The common feature of all of these circuits is that they are supplied from a DC voltage source, which is commonly a large capacitor, supplied from a rectified sinusoidal voltage source. This implies a multi-stage energy conversion process and has the disadvantage of the requirement for a large DC link capacitor between the input and output stages, such that a smooth DC link voltage is maintained despite the large power pulsations drawn by the switched reluctance motor. In order to achieve a large capacitance in a suitable volume, electrolytic capacitors are normally necessary. These still generally occupy a significant volume of the drive, and are unsuitable for aerospace applications due to the vulnerability of

the fluid within them to large variations in pressure and temperature. The rectification stage normally also implies uni-directional power flow, making regenerative braking impossible. An active front end PWM voltage source rectifier can be used but adds a further level of complexity to the drive, and potential for reliability problems.

Presented in this thesis is a novel form of power electronic converter, termed the single sided matrix converter (SSMC). This is a direct energy converter, and switches input phases directly to output phases, without the use of an intermediary energy storage device. It is based on a standard matrix converter topology, but uses only unidirectional switch cells (implemented using an IGBT), as opposed to the conventional bidirectional switch cells. This means that only unidirectional currents can be supplied by the SSMC, as are required by the switched reluctance motor. The complex commutation problem seen in conventional matrix converters [13] remains a vulnerability of the drive, even though reliable commutation schemes have been tested at significant power levels [14] [15]. The use of unidirectional switch cells means that the commutation problem is greatly simplified, as the reduced number of power electronic switches and arrangement of diodes makes a short circuit between input phases impossible. Care must only be taken to ensure that an open circuit on the output side does not occur.

Control of the drive was to be achieved without the use of a digital signal processor (DSP), making it easily usable in the aerospace industry, without the need for approval of the specific DSP. Two simple hysteresis based control schemes were therefore proposed which would be suitable for implementation using a field programmable gate array (FPGA) chip. The first of these uses a single hysteresis band, and applies the most positive and most negative supply voltages available in order to control the motor phase currents. The second scheme uses a novel double hysteresis band configuration and applies different input line to line voltages across the motor phase terminals depending on the current change required.

A motor drive is therefore proposed which uses:

- a simple, inherently fault tolerant motor.
- a direct energy conversion power electronic converter which avoids the need for large

electrolytic capacitors, making it suitable for aerospace applications, and which is inherently simpler than a conventional matrix converter.

- a control scheme fully implemented on an FPGA, making its use in aerospace actuation systems a straightforward process.

Potential for use of the SSMC with a brushless trapezoidal PMDC motor was also recognised early in this PhD, and a second student, Xiaoyan Huang began work on the design of a novel 5-phase PMDC motor as part of her PhD. Two single sided matrix converters were therefore assembled and tested as part of this PhD work, with results presented for both applications.

1.1 Thesis Structure

The remainder of this thesis is divided into chapters, covering different areas of the work carried out.

Chapter 2 provides an overview of some common power electronic converter types, including direct energy converters. A detailed review of the conventional matrix converter and its associated practical implementation problems, solutions and control methods is provided.

In chapter 3, the single sided matrix converter is introduced. Firstly the circuit topology is explained, followed by a look at the methods of control that are proposed. Consideration is also given to the most appropriate form of control platform to be used, bearing in mind the need for high reliability and potential application within the aerospace industry. A review is then provided of the types of motor which may be suitable for use with the SSMC, and the design considerations that should be taken into account to provide reliable, fault tolerant operation.

Presented in chapter 4 are simulations performed to verify the operation of the circuit

topology and the proposed control schemes. Firstly the models used are described, including the simple switched reluctance motor model that was developed. Simulation results are then provided for operation of both control schemes, applied to control of currents in an inductive/resistive load, the switched reluctance motor, and a trapezoidal PMDC motor.

Chapter 5 gives details of the practical implementation of the single sided matrix converter and its control. First the converter hardware is described, including the controller platform, and several PCB's. One of these was used to provide the laminated power planes required for safe operation of the matrix converter. The FPGA controller is then described. A review is provided of the program development suite, followed by a consideration of the procedures required to develop programmes for FPGA's. A description is then given of the FPGA control software developed, as well as the interfacing of a DSP, used to extract controller operation data.

In chapter 6, the practical results taken from the prototype SSMC are presented. Results for two converters were acquired, demonstrating operation of the SSMC with both the switched reluctance and trapezoidal PMDC motors. Results for both proposed control schemes are given.

Chapter 7 presents the conclusions drawn from the work, including advantages and disadvantages of the two proposed control techniques. This is followed by a look at areas recognised as requiring further research.

Chapter 2

Power Electronic Converters including the Matrix Converter

Throughout the majority of this thesis, the SSMC is considered as an electronic drive for an electric motor. In broader terms however, it is a power electronic converter, and fits into a family of power electronic converters, differentiated by their input and output current and voltage types and power flow capabilities. This chapter begins by summarising the general types of power conversion performed using power electronic converters, before a somewhat more detailed explanation of the operation of AC input direct power converters. The intention is to assist the reader in placing the SSMC within this family of power converters, whilst gaining an understanding of the relative advantages and disadvantages of each.

2.1 Power Electronic Converters Overview

Power Electronic Converters are used when there is a need to modify the form of electrical energy. Semiconductor devices are used to switch the electrical supply, using a large number of circuit topologies. The energy conversions that are commonly implemented

using power electronic converters are:

1. DC to DC
2. AC to DC
3. DC to AC
4. AC to AC

Conversions 1 to 3 are commonly performed as direct conversion's, whereas conversion 4 is usually achieved using a two step process. The converters used to perform each of the conversions are mentioned briefly below.

DC to DC conversion is commonly performed by either a chopper for voltage reduction, or a boost converter where a higher output voltage is required.

AC to DC conversion is performed by a rectifier, either uncontrolled, using diodes, or controlled, using thyristors, where the output voltage is controllable. PWM rectifiers are also sometimes used where greater control over input current quality, or regeneration to the supply is required.

DC to AC conversion is performed using an inverter. There are two common forms of inverter. The first, the 'Six Step Square-Wave Inverter', outputs rectangular blocks of voltage at the required output frequency. A positive output voltage would be followed by a period of zero volts, and then a period of negative voltage, again followed by a period of zero volts. When connected across an inductive load this rectangular output voltage induces an approximately sinusoidal flow of current. The second common form of inverter is the 'Pulse Width Modulated (PWM) Inverter'. With this form of inverter, the DC voltage is switched across the output at a high frequency. By varying the on duration with respect to the off duration, and applying this across an inductive load, a sinusoidal current is induced.

AC to AC conversion is most commonly performed as a two step conversion, where the incoming AC is first rectified to produce DC, which is smoothed using a DC link capacitor

and then inverted, commonly using a PWM Inverter, to reproduce AC at a new voltage and frequency. This approach is widely used, and when using a PWM controlled rectifier and PWM inverter, is seen to produce very good results. Sinusoidal input and output currents are produced, assuming that the high frequency switching component of the waveform is filtered out by both the load inductance, and the supply side filter, and unity power factor at the input is possible. This form of AC to AC converter does however rely heavily on the use of a relatively large DC link capacitance in order to smooth the power flow between the input and output.

2.1.1 The PWM Current Source Rectifier

The PWM rectifier may be used as the front end in a back-to-back inverter arrangement, where regeneration to the supply and/or improved input current quality is required. Two topologies exist, the voltage source PWM rectifier and the current source PWM rectifier. A PWM rectifier is shown within the red dashing in figure 2.1, as part of a regenerative AC motor drive. Both the voltage and current source rectifiers output to a DC stage, this being a DC link capacitor in the case of the voltage source PWM rectifier, and a DC link inductor labelled Ld here, for the current source PWM rectifier.

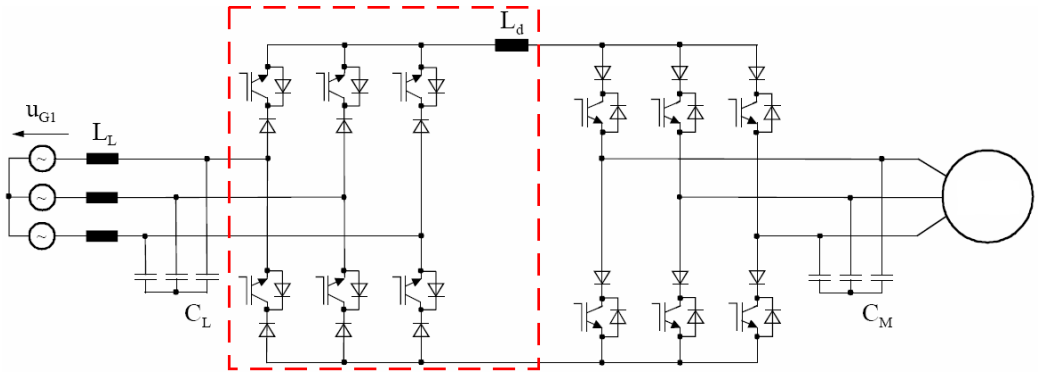

Figure 2.1: PWM Current Source Rectifier

The circuit topology of the PWM current source rectifier is the same as that used in the single sided matrix converter, however its control and use are quite different. In the current

source PWM rectifier a continuous, but variable Ld current is required. This is fed to the output stage, which modulates the constantly flowing current between the AC load phases. In this type of balanced three phase AC application, constant output power will be drawn, implying constant input power. With the correct modulation of the input side switching devices, possibly using the space vector method [16], this constant power flow is inherently translated into sinusoidal input currents [17]. The use of the circuit to supply pulsed DC loads presents a new control problem, which is the focus of this work.

2.2 Direct Power Converters (AC Input)

For the purposes of this thesis, the term 'direct power converter' refers to a power electronic converter which does not include an energy storage element between its input and output side. An example of a converter that does include an energy storage element is the PWM rectifier/inverter combination described in section 2.1. Also, as this research was concerned with drawing power from an AC supply, this chapter considers only direct power converters designed for use with an AC input. Most converters designed to supply power from a DC input are inherently direct power converters.

Referring to table 2.1, one can see how the SSMC compares with the Rectifier, the Cycloconverter and the Matrix Converter. Each is a direct power converter, however the Cycloconverter and Matrix Converter produce an AC output, whilst the Rectifier and Single Sided Matrix Converter produce a DC type output. However, considering the type of commutation, the Rectifier and Cycloconverter are naturally commutated, whilst the two forms of matrix converter are force commutated. An explanation of each converter topology and the way in which it is operated is provided in the remainder of this chapter.

	Commutation	
	Natural	Forced
Non-AC Output	Rectifier	Single Sided Matrix Converter
AC Output	Cycloconverter	Matrix Converter

Table 2.1: AC input Direct Conversion Power Electronic Converters

2.2.1 The Cycloconverter

The Cycloconverter is a direct conversion static frequency changer. Two circuit topologies for a three phase input, three phase output Cycloconverter are shown in figure 2.2. The circuit uses thyristors, and by applying a varying delay to the appropriate thyristor firing signal, an output voltage can be produced which approximates a sine wave.

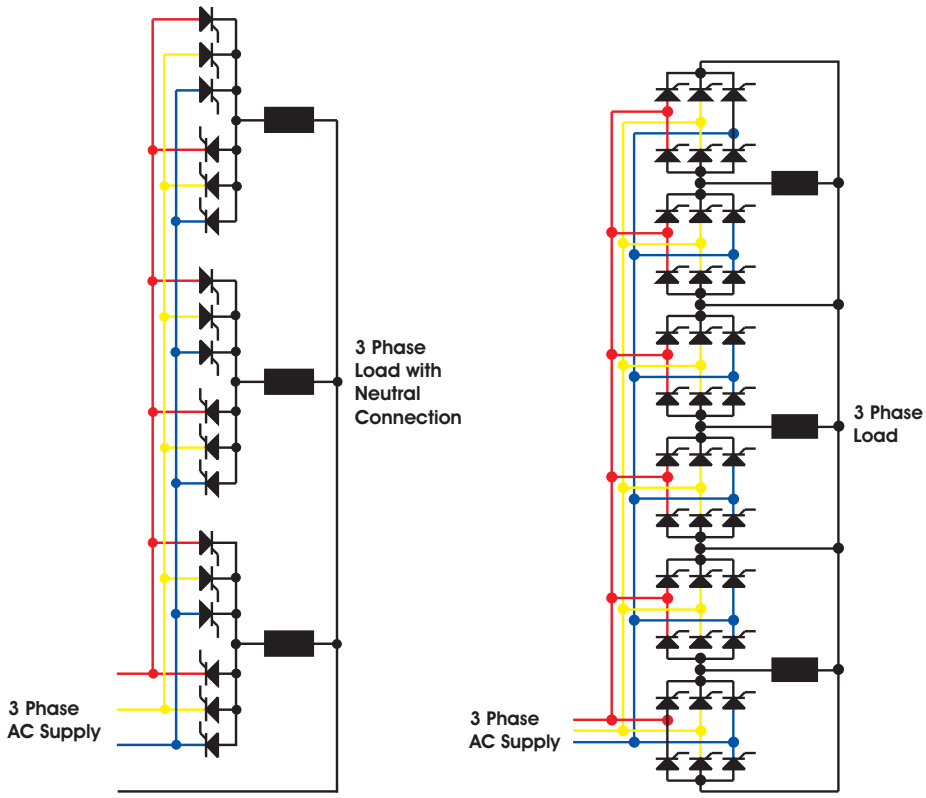

Figure 2.2: Cycloconverter Topology. a,6-Pulse. b,12-Pulse.

Once a thyristor has been fired, it conducts until the potential applied across it is reversed. This implies that high frequency switching of the devices is not possible, and hence only output frequencies lower than that of the input frequency may be reproduced. Figure 2.3 shows the three input phase voltages along with the output phase voltage in solid black, and the output current as the dashed black sine curve. This is for the case of a resistive load, with maximum output voltage at approximately $2/11^{ths}$ supply frequency. More commonly, inductive loads are supplied. When this is the case, the current lags the voltage as shown

in figure 2.4.

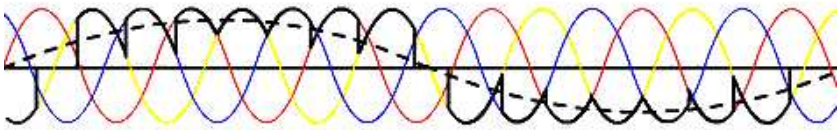

Figure 2.3: Cycloconverter Single Output Phase Voltage - Resistive Load

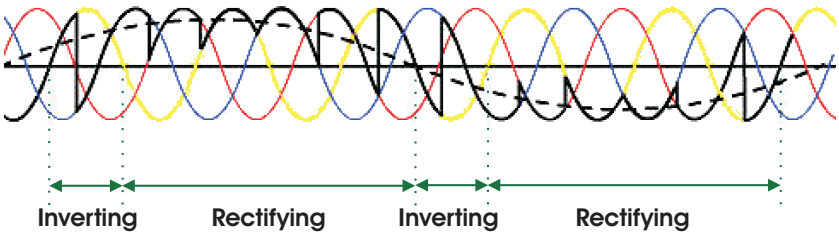

Figure 2.4: Cycloconverter Single Output Phase Voltage - Resistive & Inductive Load

Whilst clearly a direct power converter, the cycloconverter has the significant disadvantage that its switching frequency is tied to that of the voltage supply, and can therefore only supply loads requiring slow changes in average current level, such as low frequency AC drives as can be found in traction applications [18] and large rolling mills [19].

2.2.2 The Matrix Converter

The matrix converter can be considered as a force commutated cycloconverter, implying a direct AC to AC converter capable of high switching frequencies, and therefore output voltage frequencies greater than that of the cycloconverter. The three phase version uses nine bidirectional switches, allowing connection of each output phase to each input phase of the converter. This implies bidirectional power flow, allowing regeneration to the supply if the application is suitable. Precise control of the phase commutations is essential in order to avoid short circuits on the input side of the converter.

Complex switching strategies are employed within the matrix converter control, requiring

the use of a DSP. This however allows sinusoidal input currents to be drawn, when a balanced sinusoidal load is being driven. Power factor correction is inherently possible by advancing or delaying the input current waveform with respect to the input voltage waveforms.

The direct conversion nature of the matrix converter means that no DC link capacitor is used. This is advantageous for aerospace actuators, however, the lack of energy storage within the converter implies filtering of the supply is necessary in order to meet its harmonic requirements. The input filter uses a small amount of energy storage within low value capacitors in order to remove the majority of the switching harmonics induced in the supply currents due to the PWM switching of the matrix converter.

A more in depth description of the topology, control, and commutation problem is provided in section 2.3.

2.3 The Conventional Matrix Converter

The concept of the matrix converter was first seen in the work of L.Gyugyi and B.Pelly, who described 'Static Power Frequency Changers' in their publication of 1976 [20]. At this time the matrix converter was referred to as a Force Commutated Cycloconverter, this being a cycloconverter in which bidirectional static power devices were employed and controlled in such a way as to enable the converter to be used as an unrestricted frequency changer capable of regenerative power recovery. Much research has been carried out since this time in optimising the control of the matrix converter devices in order to produce a safe, reliable and efficient implementation of the topology, suitable for applications in the real world.

The following sections discuss the fundamentals of the matrix converter, including its advantages and disadvantages when compared with alternative drives. Many solutions to the practical implementation problems of the matrix converter have been proposed over the years, and a review of those is given, including descriptions of the mathematical models used to solve the modulation problem.

2.3.1 Circuit Structure

The Matrix converter offers an all silicon solution for AC-AC power conversion. A 3-phase to 3-phase matrix converter consists of an array of nine bi-directional switches, constructed from unidirectional power devices, and arranged such that any of the output lines of the converter can be connected to any of the input lines. A simplified block diagram of the circuit layout is given in figure 2.5. One commonly used form of bidirectional switch is the common emitter configuration, as shown in figure 2.6. The advantage of the common emitter configuration is that only one isolated floating power supply is required per bidirectional switch cell.

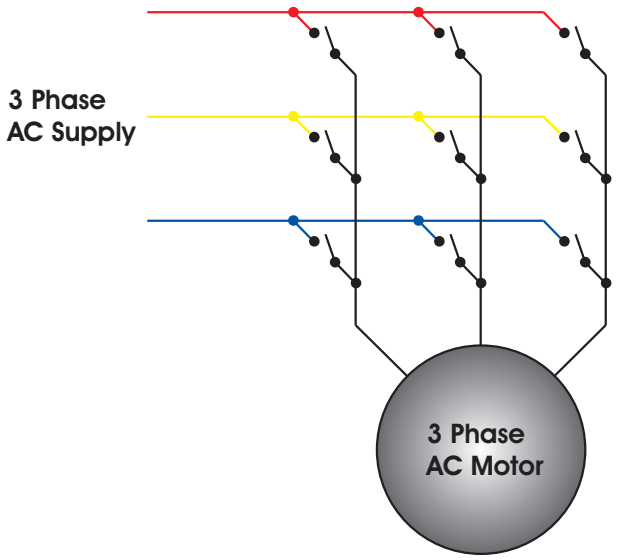

Figure 2.5: Conventional AC Matrix Converter Topology

The required output voltages are generated by the precise, high frequency modulation of the converter switches, based on the supply voltage state. When compared with conventional AC/DC drives as used with switched reluctance motors, or AC/DC/AC drives used with sinusoidal AC machines, the matrix converter topology has several advantages. The first, and major of these is the removal of the DC link and associated bulky electrolytic capacitors, which have a limited lifetime, and are intolerant to high temperatures. This results in a high power density converter being possible. Bidirectional power flow is also

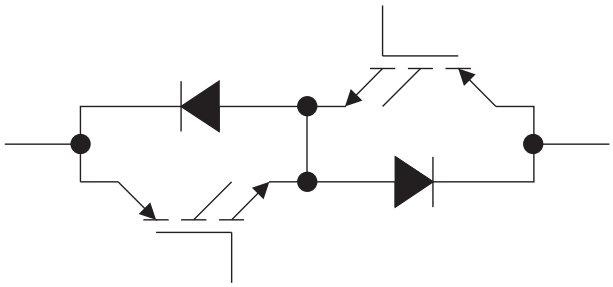

Figure 2.6: Common Emitter Bidirectional Switch Cell used in Conventional AC Matrix Converters

an inherent feature of the matrix converter, and with appropriate control of the switching components, both output voltage and input current are sinusoidal (for a balanced sinusoidal load), with the only harmonics generated being at or above the device switching frequency. Unity displacement factor in the supply is also inherently possible with the use of the appropriate modulation technique.

Research carried out since the 1970's has overcome many of the problems of practical implementation of the matrix converter, and interest from industry is growing [21], with specific matrix converter IGBT packages being developed [22] [23] [24]. As semiconductor prices continue to fall, matrix converters may in the future become attractive alternatives to the back-to-back inverter commonly used in applications where sinusoidal input currents and true bidirectional power flow are required [25]. One of the problems with the matrix converter, where standard supply voltage and standard machines are to be used is the voltage transfer ratio, as is discussed in section 2.3.2.2. This will not however cause a problem when the electrical machine can be designed for use with a matrix converter, as part of an integrated motor drive.

2.3.2 Mathematical Model and Modulation Strategies

The problem of modulating the switches in a matrix converter is a complex one. This section presents the mathematical model of matrix converter operation, and introduces the

modulation problem. The material in this section is based on the mathematical development presented in [26]. Several different matrix converter modulation strategies have been proposed, and this section discusses the two most common. The remaining solutions are mostly similar, and are not discussed here.

The following study is based on a three phase input, three phase output matrix converter, as shown in figure 2.5. The principle will however apply to a converter with any number of input and output phases. The designation of input and output connections in the matrix converter is arbitrary, as the converter switching circuit is symmetrical. However all sensible modes of operation will see one side of the matrix converter having a voltage stiff characteristic, and the other side having a current stiff characteristic. In this discussion, and as with any motor drive application, the input side is voltage stiff (as ensured by lineside phase to phase filter capacitors), and the output is current stiff, due to the inductive nature of the motor load.

If one assumes ideal switching, switching functions can be used to derive a mathematical model for the matrix converter [27]. The switching function, S_{Kj} for the switch connecting input line K to output line j is defined to be 1 when the switch is connecting and 0 when it is not. Using this terminology, the instantaneous current and voltage relationships can be given as in 2.1 and 2.2.

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} S_{Aa}(t) & S_{Ba}(t) & S_{Ca}(t) \\ S_{Ab}(t) & S_{Bb}(t) & S_{Cb}(t) \\ S_{Ac}(t) & S_{Bc}(t) & S_{Cc}(t) \end{bmatrix} \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \tag{2.1}$$

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} S_{Aa}(t) & S_{Ab}(t) & S_{Ac}(t) \\ S_{Ba}(t) & S_{Ba}(t) & S_{Bc}(t) \\ S_{Ca}(t) & S_{Cb}(t) & S_{Cc}(t) \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{2.2}$$

A constraint on possible switching combinations is imposed by the fact that short circuits of the capacitive input side, and open circuits of the inductive output side must be avoided. If this constraint is not adhered to, damage to the converter will occur. The switching function representing this constraint is given in 2.3

$$\sum_{K=A,B,C} S_{Ka}(t) \;=\; \sum_{K=A,B,C} S_{Kb}(t) \;=\; \sum_{K=A,B,C} S_{Kc}(t) = 1 \tag{2.3}$$

Finding solutions to meeting these constraints is one of the practical implementation problems that has recieved significant interest in the past. The following analysis assumes that the constraint of 2.3 is adhered to, and that instantaneous switching occurs.

The output voltage of the matrix converter is produced by selecting each of the input phases in sequence, for predetermined periods of time. Figure 2.7 shows typical waveforms for a relatively low switching frequency. The output voltage is made up of segments taken from each of the three input phases, whilst the input current is sections from each of the three output phases. Periods of zero input current also occur when the output current is allowed to freewheel through the matrix switches. The switching of the converter devices usually occurs with a fixed repeat period, termed T_{seq}, which is analogous with the carrier period in conventional PWM schemes. Figure 2.8 shows the generalised form of the typical matrix converter switching sequence. The average behaviour of the converter at output frequencies well below the switching frequency can be determined by defining a modulation duty cycle for each switch (eg. $m_{Aa}(t) = \frac{t_{Aa}}{T_{seq}}$ where t_{Aa} refers to the time for which S_{Aa} is ON and T_{seq} is the sequence time of the PWM pattern). The modulation strategies, as given in equations 2.4 and 2.5 can then be defined using these continuous time functions.

Note that in equations 2.4 and 2.5, v_x & i_x $(x = a, b, c)$ are now values averaged over the sequence time.

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} m_{Aa}(t) & m_{Ba}(t) & m_{Ca}(t) \\ m_{Ab}(t) & m_{Bb}(t) & m_{Cb}(t) \\ m_{Ac}(t) & m_{Bc}(t) & m_{Cc}(t) \end{bmatrix} \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \tag{2.4}$$

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = \begin{bmatrix} m_{Aa}(t) & m_{Ab}(t) & m_{Ac}(t) \\ m_{Ba}(t) & m_{Ba}(t) & m_{Bc}(t) \\ m_{Ca}(t) & m_{Cb}(t) & m_{Cc}(t) \end{bmatrix} \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} \tag{2.5}$$

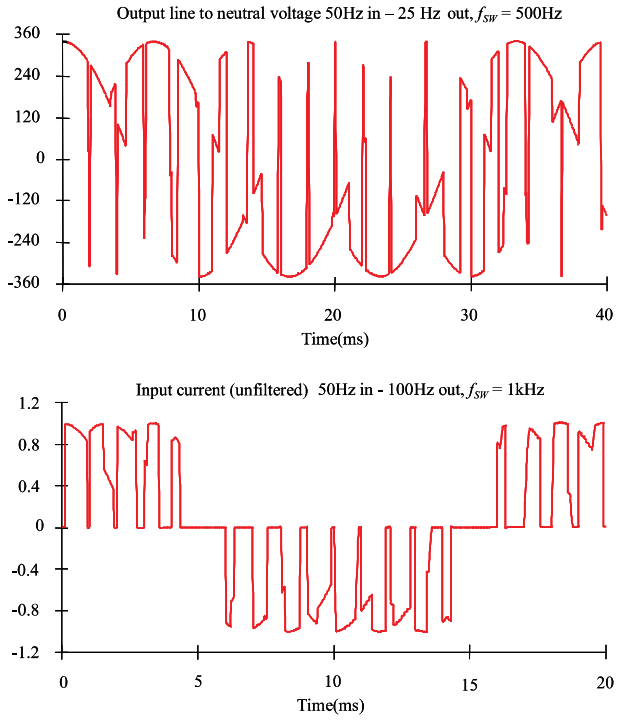

Figure 2.7: Typical Matrix Converter waveforms a,Output Voltage. b,Input Current

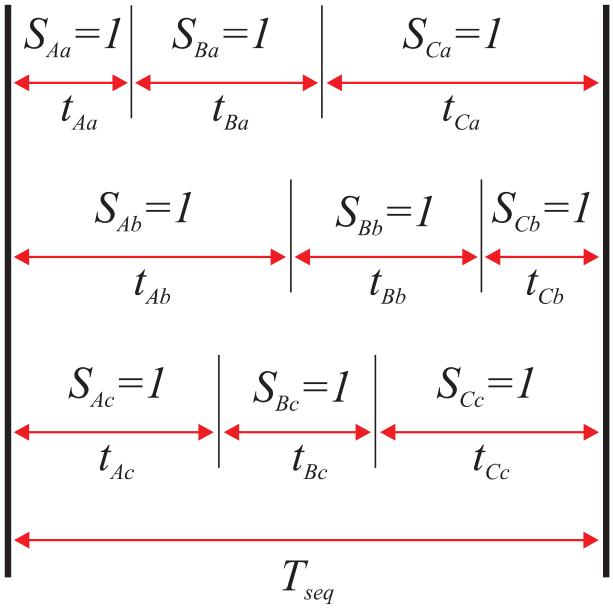

Figure 2.8: General Form of Matrix Converter Switching Pattern

A more compact notation for equations 2.4 and 2.5 is given in 2.6, where M(t) is termed the modulation matrix.

$$\begin{aligned}[v_o(t)] &= [M(t)][v_i(t)] \\ [i_i(t)] &= [M(t)]^T[i_o(t)]\end{aligned} \tag{2.6}$$

The constraint equation, 2.3 can now be written as in 2.7.

$$\sum_{K=A,B,C} m_{Ka}(t) \; = \sum_{K=A,B,C} m_{Kb}(t) \; = \sum_{K=A,B,C} m_{Kc}(t) = 1 \tag{2.7}$$

2.3.2.1 The Modulation Problem and Basic Solution

The modulation problem is usually posed on the basis that sinusoidal output voltages, $v_o(t)$ and sinusoidal input currents, $i_i(t)$ are the aim. Then, given a set of input voltages,$v_i(t)$ and an assumed set of output currents, $i_o(t)$ as in 2.8, one must derive a modulation matrix M(t) such that equation 2.9 and the constraint equation 2.7 are satisfied.

$$[v_i(t)] = V_{im} \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{2\pi}{3}) \\ \cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix} \qquad [i_o(t)] = I_{om} \begin{bmatrix} \cos(\omega_o t + \phi_o) \\ \cos(\omega_o t + \phi_o + \frac{2\pi}{3}) \\ \cos(\omega_o t + \phi_o + \frac{4\pi}{3}) \end{bmatrix} \tag{2.8}$$

$$[v_o(t)] = qV_{im}\begin{bmatrix}\cos(\omega_o t)\\ \cos(\omega_o t+\frac{2\pi}{3})\\ \cos(\omega_o t+\frac{4\pi}{3})\end{bmatrix} \qquad [i_i(t)] = q\frac{\cos\phi_o}{\cos\phi_i}I_{om}\begin{bmatrix}\cos(\omega_i t+\phi_i)\\ \cos(\omega_i t+\phi_i+\frac{2\pi}{3})\\ \cos(\omega_i t+\phi_i+\frac{4\pi}{3})\end{bmatrix} \tag{2.9}$$

Where

q = Voltage Transfer Ratio

ω_i = Input Frequency

ω_o = Output Frequency

ϕ_i = Input Phase Displacement Angle

ϕ_o = Output Phase Displacement Angle

Venturini described two basic solutions to this problem [28], as given in equations 2.10 and 2.11.

$$[M1(t)] = \frac{1}{3}\begin{bmatrix}1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3})\\ 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3})\\ 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t)\end{bmatrix} \tag{2.10}$$

with $\omega_m = (\omega_o - \omega_i)$

$$[M2(t)] = \frac{1}{3}\begin{bmatrix}1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3})\\ 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t)\\ 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3})\end{bmatrix} \tag{2.11}$$

with $\omega_m = (\omega_o + \omega_i)$.

With the solution of equation 2.10 the same phase displacement is seen at the input as at the output, ie. $\phi_i = \phi_o$. The solution of equation 2.11 gives reversed phase displacement at the input with respect to that of the output, ie. $\phi_i = -\phi_o$. the two solutions can be combined using equation 2.12, providing control over the input displacement factor.

$$[M(t)] = \alpha_1[M1(t)] + \alpha_2[M2(t)] \qquad \text{where } \alpha_1 + \alpha_2 = 1 \tag{2.12}$$

Unity displacement factor at the input, irrespective of the displacement factor at the output can be achieved by setting $\alpha_1 = \alpha_2$. Alternatively, a leading (capacitive) displacement factor at the input with a lagging (inductive) displacement factor at the output, or vice versa can be achieved, by varying α_1 and α_2.

If $\phi_i = \phi_o$ is used, the modulation function can be expressed in the more compact form of equation 2.13.

$$m_{Kj} = \frac{t_{Kj}}{T_{seq}} = \frac{1}{3}\left(1 + \frac{2v_K V_j}{V_{im}^2}\right) \quad \text{for } K = A, B, C \text{ and } j = a, b, c \tag{2.13}$$

The basic modulation algorithm described by equation 2.13 operates such that the average output voltages (taken over the switching sequence) are equal to the target output voltages $[v_o(t)]$, during that switching sequence. If this is to be the case the output voltages must, under all operating conditions, fit within the input voltage envelope. This solution therefore yields a maximum output voltage ratio (q) of 50%, as is indicated in figure 2.9. This basic method is ideally suited to real time implementation, however the 50% voltage ratio implies that this algorithm is of little practical use.

2.3.2.2 The Optimum Amplitude Algorithm

An improvement in the output voltage to 87% can be achieved by modifying the target output voltage matrix to include third harmonics of the input and output frequencies [29]. this can be achieved by implementing the common mode addition technique described in [30]. With this development, significantly more of the input voltage envelope is made use of, as illustrated in figure 2.10. The third harmonics will naturally cancel in a three-phase load, in the same manner as is seen in a conventional inverter. Achieving this requires modification of equation 2.9 to produce equation 2.14.

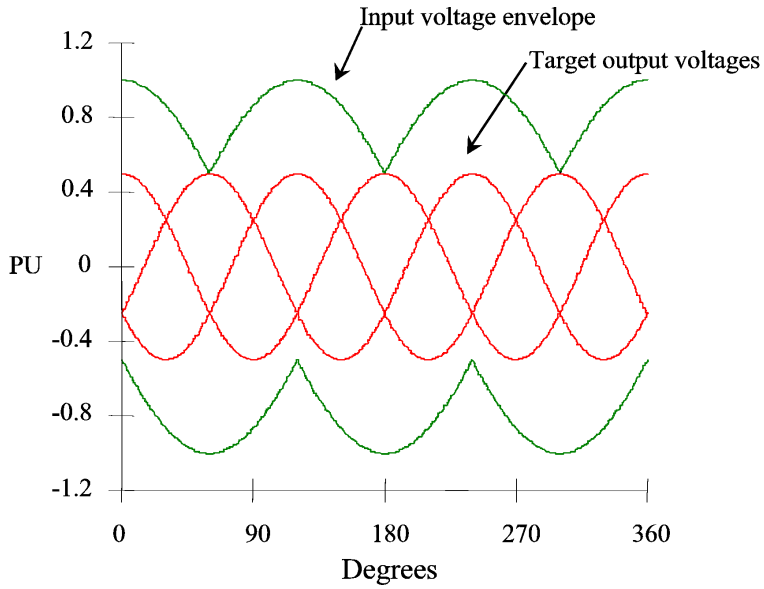

Figure 2.9: Theoretical Waveforms Illustrating the 50% Voltage Ratio Limit

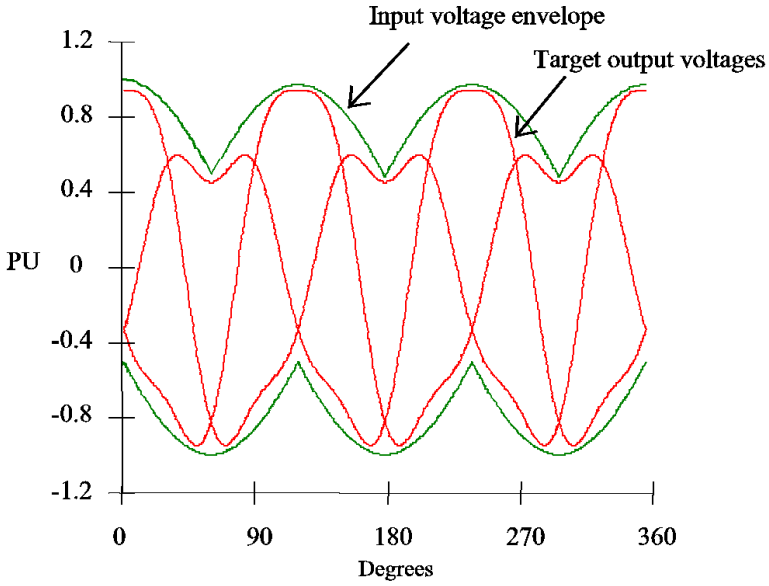

Figure 2.10: Theoretical Waveforms Illustrating the Third Harmonic Addition to Obtain the 87% Optimum Voltage Ratio Limit

$$[v_o(t)] = qV_{im} \begin{bmatrix} \cos(\omega_o t) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \\ \cos(\omega_o t + \frac{2\pi}{3}) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \\ \cos(\omega_o t + \frac{4\pi}{3}) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \end{bmatrix} \tag{2.14}$$

With the addition of the triple harmonics, equation 2.13 is modified to take the form of equation 2.15, in order to achieve a displacement factor of unity [29].

$$\begin{aligned} m_{Kj} &= \frac{1}{3}\left(1 + \frac{2v_K V_j}{V_{im}^2} + \frac{4q}{3\sqrt{3}}\sin(\omega_i t + \beta_K)\sin(3\omega_i t)\right) \quad \text{for } K = A, B, C \text{ and } j = a, b, c \\ \beta_K &= 0, \frac{2\pi}{3}, \frac{4\pi}{3} \quad \text{for } K = A, B, C \text{ respectively} \end{aligned} \tag{2.15}$$

The solution provided in equation 2.14 is used in real-time implementations of the Venturini algorithm, and can be easily processed by modern microprocessors, providing switching frequencies of tens of kilohertz. If desired, input displacement factor control away from unity can be introduced, by incorporating a phase shift between the actual input voltages, and those inserted into equation 2.14. This does however reduce the output voltage ratio from 0.87.

2.3.2.3 Scalar Modulation Approach

A scalar modulation approach can be used with the matrix converter [31] [32]. This approach is based on taking instantaneous input voltage measurements, and comparing their relative magnitudes in order to determine the switching signals. Subscripts are assigned to the input phases based on table 2.2, before then calculating the modulation duty cycles using equation 2.16.

Condition	Subscript to Assign
Phase polarity different to that of the other two	M
Of the two remaining phases:	
Phase with lowest absolute magnitude	L
Remaining Phase	K

Table 2.2: Scalar Modulation input Phase Subscript Assignment

$$\begin{aligned} m_{Lj} &= \frac{(v_j - v_M)v_L}{1.5V_i m^2} \\ m_{Kj} &= \frac{(v_j - v_M)v_K}{1.5V_i m^2} \\ m_{Mj} &= 1 - (m_{Lj} + m_{Kj}) \text{ for } j = a, b, c \text{ respectively} \end{aligned} \tag{2.16}$$

Common-mode addition is again used with the target output voltages v_j in order to achieve the q value of 0.87. Although this method appears quite different to the optimum Venturini approach, virtually identical switch timings are produced. Equation 2.17 expresses the modulation duty cycles for the scalar modulation approach in the form of equation 2.15.

$$\begin{aligned} m_{Kj} &= \frac{1}{3}\left(1 + \frac{2v_K V_j}{V_{im}^2} + \frac{2}{3}\sin(\omega_i t + \beta_K)\sin(3\omega_i t)\right) \quad \text{for } K = A, B, C \text{ and } j = a, b, c \\ \beta_K &= 0, \frac{2\pi}{3}, \frac{4\pi}{3} \quad \text{for } K = A, B, C \text{ respectively} \end{aligned} \tag{2.17}$$

Equations 2.15 and 2.17 are identical when a q value of $\frac{\sqrt{3}}{2}$ is used. the only difference between the optimum Venturini and scalar methods is that q is worked into the right most term in the Venturini method, whereas it is fixed at its maximum value in the scalar approach. This has a negligable effect on the output voltage, apart from at low switching frequencies, where the optimum Venturini method is seen to be superior.

2.3.2.4 Space Vector Modulation Approach

The space vector modulation method is commonly used in the control of conventional PWM inverters, and originates from the use of the "Space Phasor" method used in analysing three phase machines. The approach is particularly favoured by those working in the area of field oriented (or vector) control, as it allows the visualisation of the time and spatial relationships between the resultant current and flux vectors (or space phasors) in a number of reference frames. The use of space vector modulation with matrix converters was first presented in [33], where a new PWM control technique for forced commutated cycloconverters, based on the space vector representation of the voltages in the complex plane was introduced.

2.3.2.4.1 Space Phasors Defined in equation 2.18 is the target output voltage space phasor, in terms of the line to line voltages.

$$\overrightarrow{\mathbf{V}}_o(t) = \frac{2}{3}(v_{ab} + av_{bc} + a^2 v_{ca}) \quad \text{where } a = e^{j2\pi/3} \tag{2.18}$$

On an Argand diagram, multiplication by a corresponds to a rotation of 120° and a^2 by 240°. On the same diagram, $\overrightarrow{\mathbf{V}}_o(t)$ is a vector of constant length $(qV_{im}\sqrt{3})$ rotating at frequency ω_o. The basis of space vector modulation, in all drives, is that the possible output voltages of the converter (achieved via each permissible switching state) are expressed in the same form as equation 2.18. At each sampling instant, the position of $\overrightarrow{\mathbf{V}}_o(t)$ is compared with each of the possible output vectors and the desired output voltage is synthesised by time averaging (within the switching interval) between adjacent output vectors, to give the correct mean voltage. This process is a relatively simple one with conventional DC link inverters, as only eight possible switching states exist. Six of these are at the vertices of a regular hexagon, whilst the final two give zero volts, and are referred to as zero vectors. Therefore, the location and length of the possible output space vectors are fixed for a DC link inverter. The twenty seven possible switching states seen with the matrix converter, and the fact that the input voltages are time varying, makes implementation of

space vector control on the matrix converter a far more complex problem.

2.3.2.4.2 Matrix Converter Output Space Phasors Table 2.3 presents the twenty seven possible switching states for a three phase to three phase matrix converter, along with the output voltages produced. The output voltages given in this table may be classified using three groups:

Group I Each output line is connected to a different input line
– constant amplitude, rotating (in either direction) at the supply angular frequency.

Group II Two output lines are connected to a common input line, the remaining output line is connected to one of the other two input lines
– varying amplitude, fixed position occupying one of 6 positions regularly spaced 60° apart.

Group III All output lines are connected to the same input line
– zero amplitude at the origin.

2.3.2.4.3 Selection of Switching States A number of methods may be used to select the vectors used to produce the required output voltage at each sampling instant. Described here is a simple method although other, more sophisticated possibilities exist, which also control the space vector of the input current, giving better results [34]. The concept in all cases is however the same.

The rotating vectors of Group I are not used. The vectors from group II are separated into three subgroups, as defined in table 2.3. The six vectors in each subgroup produce a space vector along a fixed direction. These directions are mutually displaced for the three subgroups, by 120°. The amplitude and polarity of the space phasor along the defined direction varies depending upon which of the line to line voltages is used. This produces a hexagon of possible vectors, as given in figure 2.11. As an example, subgroup IIa can produce either vector 1 or 4. A number of switching states will produce each of these

Group	Output phase voltages			Output line to line voltages		
	v_a	v_b	v_c	v_{ab}	v_{bc}	v_{ca}
I	v_A	v_B	v_C	v_{AB}	v_{BC}	v_{CA}
	v_A	v_C	v_B	$-v_{CA}$	$-v_{BC}$	$-v_{AB}$
	v_B	v_A	v_C	$-v_{AB}$	$-v_{CA}$	$-v_{BC}$
	v_B	v_C	v_A	v_{BC}	$-v_{CA}$	v_{AB}
	v_C	v_B	v_A	v_{CA}	v_{AB}	v_{BC}
	v_C	v_B	v_A	$-v_{BC}$	$-v_{AB}$	$-v_{CA}$
IIa	v_A	v_A	v_B	0	v_{AB}	$-v_{AB}$
	v_A	v_A	v_C	0	$-v_{CA}$	v_{CA}
	v_B	v_B	v_A	0	$-v_{AB}$	v_{AB}
	v_B	v_B	v_C	0	v_{BC}	$-v_{BC}$
	v_C	v_C	v_A	0	v_{CA}	$-v_{CA}$
	v_C	v_C	v_B	0	$-v_{BC}$	v_{BC}
IIb	v_B	v_A	v_A	$-v_{AB}$	0	v_{AB}
	v_C	v_A	v_A	v_{CA}	0	$-v_{CA}$
	v_A	v_B	v_B	v_{AB}	0	$-v_{AB}$
	v_C	v_B	v_B	$-v_{BC}$	0	v_{BC}
	v_A	v_C	v_C	$-v_{CA}$	0	v_{CA}
	v_B	v_C	v_C	v_{BC}	0	$-v_{BC}$
IIc	v_A	v_B	v_A	v_{AB}	$-v_{AB}$	0
	v_A	v_C	v_A	$-v_{CA}$	v_{CA}	0
	v_B	v_A	v_B	$-v_{AB}$	v_{AB}	0
	v_B	v_C	v_B	v_{BC}	$-v_{BC}$	0
	v_C	v_A	v_C	v_{CA}	$-v_{CA}$	0
	v_C	v_B	v_C	$-v_{BC}$	v_{BC}	0
III	v_A	v_A	v_A	0	0	0
	v_B	v_B	v_B	0	0	0
	v_C	v_C	v_C	0	0	0

Table 2.3: Switching States for a 3-Phase to 3-Phase Matrix Converter

vectors, but at any instant in time, only one switching state (for each vector) will produce the greatest amplitude. This occurs when the selected input line to line voltage is that with the maximum amplitude. In this case the output voltage follows the rectified envelope of the input voltages, as given in figure 2.10.

As an example consider the following. When v_{ab} is the most positive line to line voltage, selecting the first state in subgroup IIa will produce a maximum length vector in direction 1. If the third state in subgroup IIa is selected, a maximum length vector will be produced in direction 4. In a similar way, if the first state in subgroup IIb is selected, a maximum length vector will be produced in direction 3 and so on. This simple example uses only the maximum length vectors in each of directions 1 to 6. The length of these vectors is given by $\frac{2}{\sqrt{3}}V_{env}$ where V_{env} is the instantaneous value of the rectified input voltage envelope.

In order to determine the modulation times, the length and position of the required output voltage vector, $\overrightarrow{\mathbf{V}}_o(t)$, is calculated at the start of the sampling interval (T_{seq}). The required output voltage is then synthesised by switching between the two adjacent vectors from group II, and also one of the zero vectors from group III. For example, if $\overrightarrow{\mathbf{V}}_o(t)$ is located between vectors 1 and 6, as illustrated in figure 2.12, $\overrightarrow{\mathbf{V}}_o(t)$ will be generated from a weighted sum of vectors 1 and 6. the weighting is achieved through time averaging, by calulating the times spent in vector 1 (t_1) and vector 6 (t_6) during the switching sequence. Applying the sine rule to figure 2.12 yields the relationship given by equation 2.19.

$$\frac{2}{\sqrt{3}}\frac{t_1}{T_{seq}}\frac{V_{env}}{\sin(\theta)} = \frac{2}{\sqrt{3}}\frac{t_6}{T_{seq}}\frac{V_{env}}{\sin(\frac{\pi}{3}-\theta)} = \frac{\overrightarrow{\mathbf{V}}_o}{\sin(\frac{2\pi}{3}-\theta)} \tag{2.19}$$

which yields:

$$t_1 = \frac{\overrightarrow{\mathbf{V}}_o}{V_{env}}T_{seq}\sin(\theta) \qquad \text{and} \qquad t_6 = \frac{\overrightarrow{\mathbf{V}}_o}{V_{env}}T_{seq}\sin(\frac{\pi}{3}-\theta)) \tag{2.20}$$

then:

$$t_0 = T_{seq} - (t_1 + t_6) \tag{2.21}$$

where t_0 is the time spent in the zero vector.

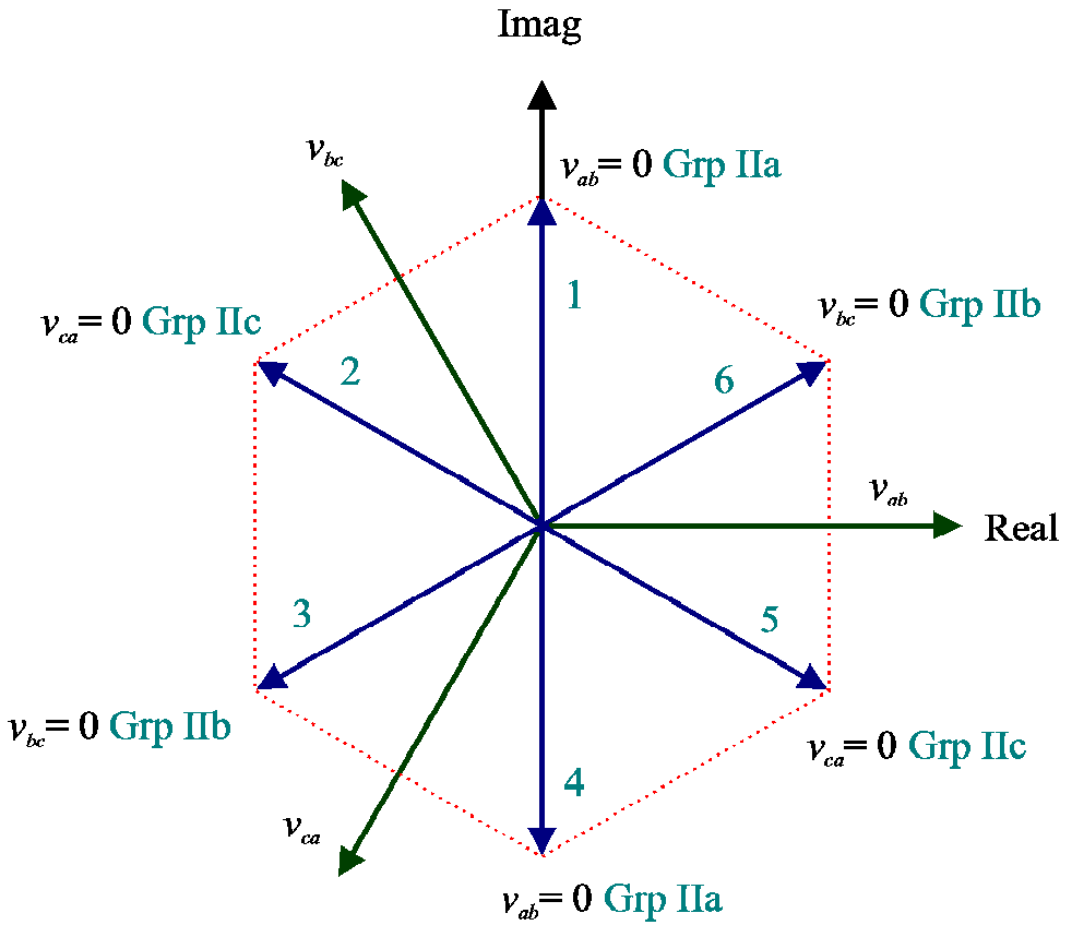

Figure 2.11: Output Voltage Space Vectors

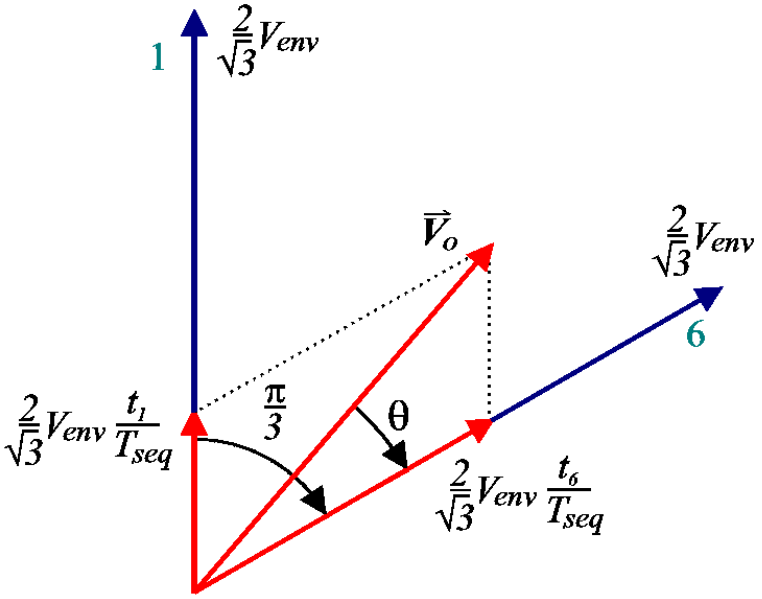

Figure 2.12: Synthesis of output voltage space phasor

There is no unique way in which the times (t_1, t_6, t_0) must be distributed within the switching sequence. Some authors suggest distributing them symmetrically with the zero state in the middle, as illustrated in figure 2.13, whilst others take the approach that this freedom should be used to minimise switching losses by performing the minimum number of switch commutations [35]. Several further variations to the space vector modulation method have been proposed [36] [34].

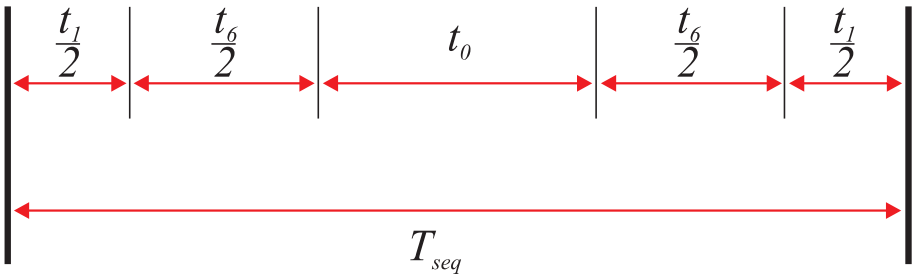

Figure 2.13: Possible Arrangement of Switching States within the Switching Sequence

A comparison of the Venturini and space vector control methods [37] has shown that the major advantage of the space vector approach lies in lower switching losses compared with

the Venturini method. The Venturini approach was however shown to produce better results in terms of the input current and output voltage harmonics.

2.3.2.5 Indirect Modulation Approach

Indirect modulation methods aim to increase the maximum voltage ratio to greater than the 86.6% limit of other methods [38] [39]. This is achieved by splitting the modulation process given in equation 2.1 into two steps, as indictated in equation 2.26. A "fictitious dc link" is generated in 2.26 by the premultiplication of the input voltages by $[A(t)]$. Postmultiplication by $[B(t)]$ then produces the desired output by modulating the "fictitious dc link". $[A(t)]$ is generally referred to as the "rectifier transformation" and $[B(t)]$ as the "inverter transformation" due to the similarity in concept with a traditional rectifier/dc link/inverter system. $[A(t)]$ is given by (2.22)

$$[A(t)] = K_A \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{2\pi}{3}) \\ \cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix}^T \tag{2.22}$$

Hence,

$$[A(t)][v_i(t)] = K_A V_{im} \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{2\pi}{3}) \\ \cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix}^T \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{2\pi}{3}) \\ \cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix} = \frac{3K_A V_{im}}{2} \tag{2.23}$$

$[B(t)]$ is given by (2.24)

$$[B(t)] = K_B \begin{bmatrix} \cos(\omega_o t) \\ \cos(\omega_o t + \frac{2\pi}{3}) \\ \cos(\omega_o t + \frac{4\pi}{3}) \end{bmatrix} \tag{2.24}$$

Hence,

$$[v_o(t)] = ([A(t)][v_i(t)])[B(t)] = \frac{3K_AK_BV_{im}}{2}\begin{bmatrix}\cos(\omega_o t)\\ \cos(\omega_o t + \frac{2\pi}{3})\\ \cos(\omega_o t + \frac{4\pi}{3})\end{bmatrix} \tag{2.25}$$

$$[v_o(t)] = ([A(t)][v_i(t)])[B(t)] \tag{2.26}$$

From (2.25) the voltage ratio is $q = \frac{3K_AK_BV_{im}}{2}$. The $[A(t)]$ and $[B(t)]$ components must be implemented by a suitable choice of the switching states. There are many ways of achieving this, which are discussed in detail in [38] and [39]. To maximise the voltage ratio, the step in $[A(t)]$ is implemented such that the most positive and most negative input voltages are selected continuously. This yields $K_A = \frac{2\sqrt{3}}{\pi}$ with a "fictitious dc link" of $\frac{3\sqrt{3}V_{im}}{\pi}$. K_B represents the modulation index of a PWM process and has the maximum value of $\frac{2}{\pi}$ [39]. The overall voltage ratio q therefore has the maximum value of $\frac{6\sqrt{3}}{\pi^2} = 105.3\%$.

The maximum voltage ratio obtainable is obviously greater than that of other methods but the improvement is obtained at the expense of the quality of either the input currents, the output voltages or both. For values of $q > 0.866$, the mean output voltage no longer equals the target output voltage in each switching interval. This inevitably leads to low frequency distortion in the output voltage and/or the input current compared to other methods with $q < 0.866$. For $q < 0.866$, the indirect method yields very similar results to the direct methods.

2.4 Summary

This chapter has provided an overview of some common forms of power electronic converter, including the current source PWM rectifier, which uses the same circuit topology as the single sided matrix converter, but applied to a different problem. The cycloconverter

was discussed as a forerunner to the conventional matrix converter, followed by a detailed review of the conventional matrix converter, and its control. Several different modulation methods were covered, including the space vector method. This can be used with the SSMC, however later in this thesis it is explained that the two are not ideally suited.

Chapter 3

Single Sided Matrix Converter DC Drive

3.1 The Single Sided Matrix Converter

The single sided Matrix Converter is a derivative of the conventional matrix converter. It is designed for supplying loads in which only one current direction is required. Here it is used to supply pulsed DC loads from a three-phase supply.

Significantly, only one IGBT is used per switch cell, compared with the two required for supplying current in both positive and negative directions in the conventional matrix converter. Whilst current can only flow in one direction through the load, both positive and negative supply voltage may be applied with respect to the potential difference across the load, enabling bi-directional power flow through the converter.

This significant difference from the conventional matrix converter means however that the standard control techniques are not suitable with this topology, as non sinusoidal outputs are required. Alternatives were developed, and this is where the new research is focussed.

3.1.1 Topology

The topology of the SSMC is very similar to that of the conventional matrix converter, and is shown in a schematic form in figure 3.1. It should be noted that figure 3.1 shows just one output phase leg. Also shown here is the voltage clamp, which is discussed in sections 5.1.4 and 5.1.5.1.

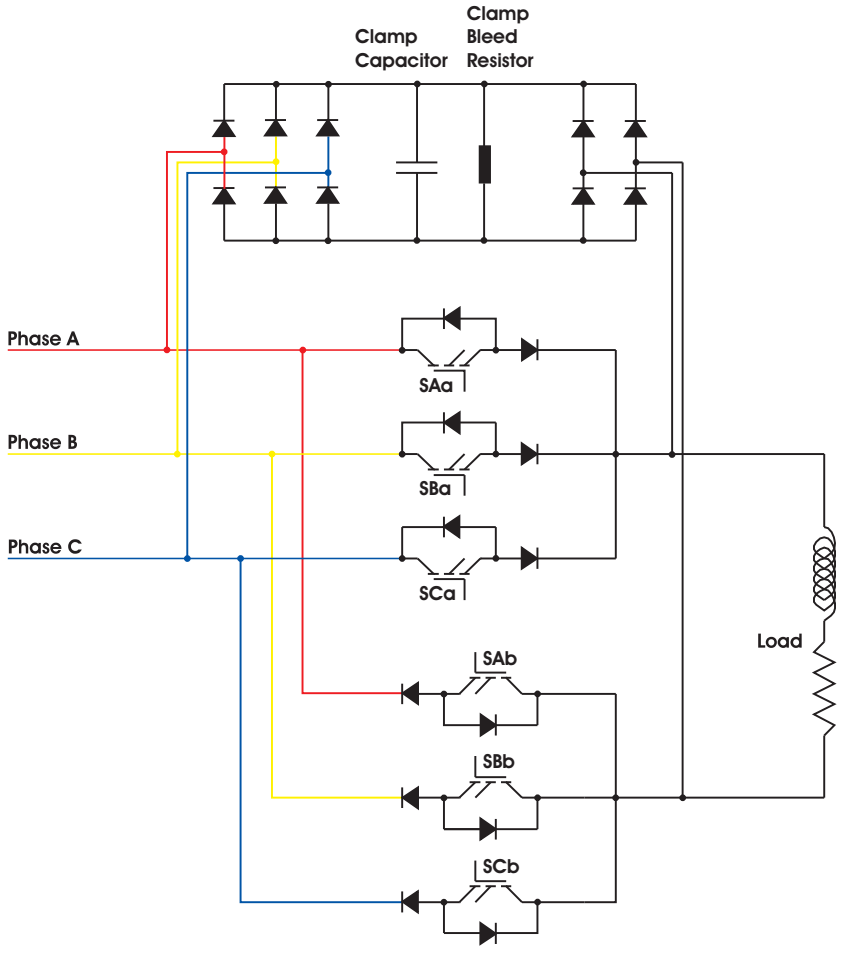

Figure 3.1: Single Sided Matrix Converter Topology - Single Output Phase

The major difference between the conventional matrix converter and the single sided matrix converter is that only one IGBT is present within each switch cell. Whilst this limits the type of load the converter can be used with to those which only require current in one direction, it is a significant advantage as it greatly simplifies the phase commutation

process. In the conventional matrix converter an incorrectly timed commutation between phases would result in a short circuit between input phases to the converter, which would potentially destroy the IGBT's, and disable the converter. However, the arrangement of IGBT and Diode in the unidirectional switch cell, means that the potential short circuit current will be blocked by the reverse biased diode.

3.1.2 Control

The now standard control technique for use with matrix converters is the space vector approach as described in section 2.3.2.4. A recent publication simulated the space vector approach with the SSMC topology and a switched reluctance motor [40], however earlier work at the University of Nottingham considered the space vector approach to produce unsatisfactory results when used with the SSMC and pulsed DC loads [41]. Two significant drawbacks have been identified with the results presented in [40]. Firstly, in order to approximate sinusoidal input currents, uncharacteristically shaped SR motor phase currents are demanded. This is a compromise, as it will reduce motor output efficiency and/or power. Secondly, the scheme adopted here will only produce the approximately sinusoidal input currents when the motor is operating at low speed. Once the motor has accelerated to such a speed that the back emf naturally limits the phase currents, no converter current limiting takes place, and therefore no phase current shaping is possible. Any attempt to shape the output currents would likely have significant effects on the motor speed.

Alternatives were therefore developed in this PhD as explained in section 3.1.2.2.

3.1.2.1 Control Platform

As with any application, the choice of control platform was important. The two options given serious consideration were a DSP (Digital Signal Processor) and an FPGA (Field Programmable Gate Array).

DSP's are popular as they are very flexible in their abilities, and are relatively easy to program and develop programs on, especially for a user familiar with the widely used 'C' programming language. The user need not be concerned with the handling of data, or ensuring data validity as this is handled by the compilation process and by the DSP itself.

FPGA's on the other hand are far more complex to develop programs for. The programmer has to consider the flow of data at every step of the program, as he or she is in fact designing a fixed circuit layout, where data cascades through a series of gates. This inherently requires a greater programming time.

Floating point DSP's are far better suited to handling complex mathematical calculations, and are a component in most power electronic drives. They are however generally serial processors, with a single core processing unit. FPGA's however process data in a parallel fashion. This ensures that there is no delay in data flow, and the time taken from data capture to an output being performed is very predictable - it can be calculated as a specific number of clock cycles. DSP's operate at far higher clock speeds than FPGA's, however the processing of data within a specific time is less predictable, depending on the number of tasks being performed by the DSP.

In some power electronic drive applications, a combination of DSP and FPGA are used. An FPGA may be used to interface with data acquisition hardware, and perform the final timing and safety critical operations in order to ensure safe and predictable operation of the drive. The DSP then forms an intermediary stage, performing the complex mathematical calculations required to implement the optimal control strategy.

It was important that the SSMC be as simple and inherently reliable as possible. The control schemes being considered, and which are discussed in section 3.1.2.2, did not require any complex calculations and were inherently more logic based, making them suitable for implementation on an FPGA. Although testing the operation of the control schemes would have been far quicker to implement using a DSP, it was decided that an FPGA would be used, as this would lead to a more inherently reliable control solution.

3.1.2.2 Control Approach

The control algorithms developed are hysteresis based. They focus entirely on controlling the converter output current to be within a predefined error band, centred on the demanded current. The three phase voltages are applied using both the single band and double band rules, and therefore introduce different frequency components into the current waveforms. Significantly, no attempt is made to control the shape of the three phase input currents, and these are inherently non-sinusoidal.

3.1.2.2.1 Single Band The single band hysteresis control scheme uses the supply phases with the most positive and most negative voltages to control the converter output current. This effectively rectifies the supply to produce an un-smoothed DC output voltage. The rectified voltage is applied to the load phase in either direction, such that the current is maintained at the reference level. This produces supply current waveforms comparable with those of a diode bridge rectifier, but with high frequency switching components

The single band control always uses large voltages to increase or decrease the output current level, which has implications on both the width of the hysteresis band, and the required load inductance.

3.1.2.2.2 Double Band The double band control scheme operates in a more intelligent way than the single band, although it is based upon the same principal. It uses both an inner and outer hysteresis band to control the output current.

Considering a three-phase sinusoidal AC supply, a supply cycle can be separated into 12 blocks as in figure 3.2, based on the points at which the phase voltages cross each other and cross zero. Within each block, three line to line voltage levels are available as in figure 3.3.

Each of these voltage levels can be applied across a load in either direction, giving three positive voltage levels, three negative voltage levels and a seventh, zero voltage available by connecting both ends of the load to the same input phase. None of these voltage levels

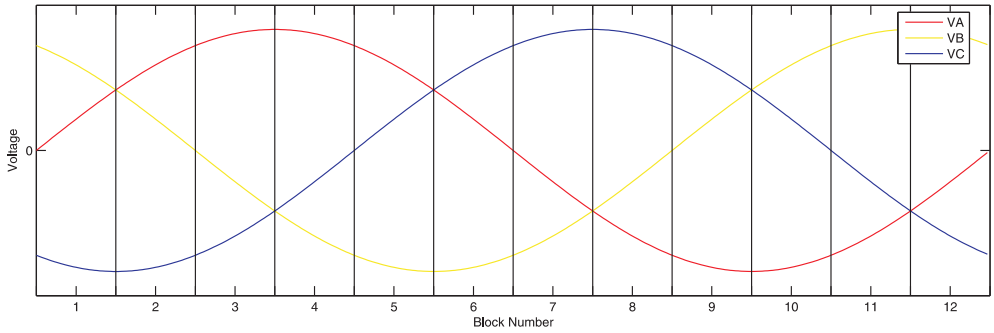

Figure 3.2: The 12 Blocks of a 3-phase AC Cycle

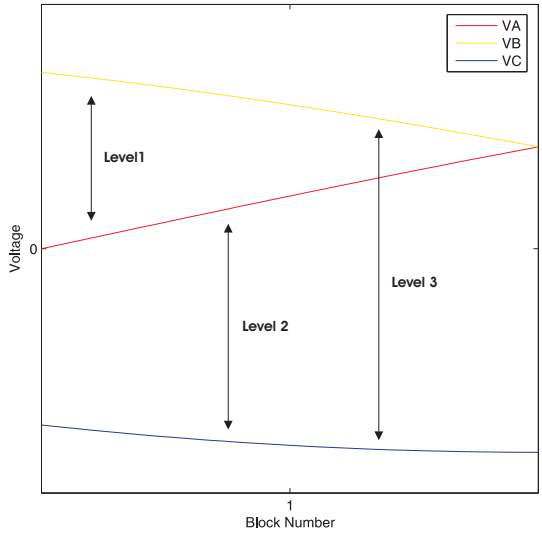

Figure 3.3: The 3 Voltage Levels Available From a 3-phase AC Supply - Block 1

are constant, however they remain within specific bands. This provides the seven voltage levels shown in figure 3.4 that can be applied to a load in order to control its current.

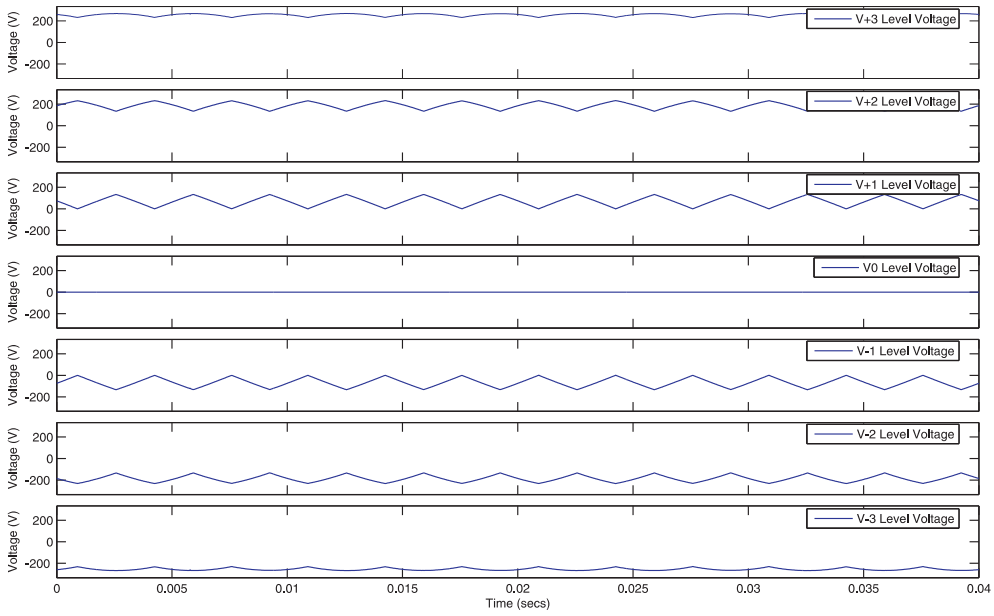

Figure 3.4: Phase to Phase Supply Voltage Levels Available From a 3-phase AC supply

When the current rises above the upper level of the inner hysteresis band (see figure 3.5) into area 2, the voltage level applied is stepped down until the current begins to reduce. At this point, the applied voltage level is held constant. If the current rises above the upper level of the outer hysteresis band (area 3) before its direction of change becomes negative, the maximum negative voltage level is automatically applied. In either case, the chosen voltage level is then maintained until the current drops below the lower level of the inner hysteresis band. The same principal is then applied until the direction of change of current becomes positive.

Figure 3.5: Double Bands

3.1.3 Advantages over other Power Converters

The single sided Matrix Converter simplifies the usual commutation problem encountered with conventional Matrix Converters, as no short circuit path exists between input phases. In addition, comparing the converter to the standard rectifier/inverter topology, this is a simple drive to construct, whilst also offering inherent bi-directional power flow. The Matrix Converter eradicates the need for the DC link capacitor which is both bulky and intolerant to extremes of temperature. In certain applications, such as those related to aircraft or integrated motor drives, this can be a major disadvantage.

3.2 Suitable Motors

The SSMC supplies current in only one direction. It is therefore not suitable for use with a motor that requires sinusoidal excitation. The three types of motor that could be driven by the SSMC are:

- DC Commutator Motor

- An unconventionally supplied or modified Trapezoidal Brushless DC motor
- Switched Reluctance Motor

The DC commutator motor could be used with the single sided Matrix Converter, as it only draws unidirectional current. However there would be little advantage except in current bandwidth when compared with a fully controlled thyristor bridge.

A novel form of the Trapezoidal Brushless DC motor, and a Switched Reluctance motor were tested with the SSMC, and are discussed in further detail.

As the focus of this work is fault tolerance and high reliability, complete electrical isolation between phases is important. For this reason, it was decided that each motor phase should be separately excited. This is usually the case with Switched Reluctance motors, however certain winding configurations and phase numbers in Brushless PMDC motors allow for Star or Delta connection of the phases. It is possible that this would be feasible with the SSMC, for certain configurations, however a fault with one phase may have serious implications for the operability of the other phases.

3.2.1 Switched Reluctance

The Switched Reluctance Motor has both a salient stator and rotor, consisting of a stack of laminations, with phase windings on the stator poles. The motor operates on the principal of attracting its moving part such that the reluctance of the magnetic path through the conducting phase winding is minimised.

Many different configurations of rotor and stator pole numbers are possible. The simplest form has just two stator poles and two rotor poles (referred to as a 2-2 SR motor) as in figure 3.6, usually with a winding on each stator pole. Diametrically opposite windings are connected either in series or parallel, producing a phase, which is supplied with pulses of current. The single phase motor has multiple drawbacks however, including starting problems, indeterminable rotational direction, and very high torque ripple. Configurations

with more rotor and stator poles are therefore often used, one common form being the 6-4 SR motor, which has six stator poles and four rotor poles (see figure 3.7). Again, diametrically opposite windings are connected, in this case forming three independent phases. The phases are energised sequentially, producing a more continuous and therefore smoother torque output than the single phase version. Rotational direction may be controlled with this configuration, by controlling the phase conduction sequence. In either case the switching of the phases must be synchronised with the rotor position, which is usually derived from a shaft encoder. Sensorless methods have also been used [42] [43] [44].

Figure 3.6: 2-2 SR Motor

The inductance profile of each motor phase for a 6-4 SR motor is as in figure 3.8. The constant inductance occurs as a rotor slot passes a stator pole. As a rotor pole starts to overlap a stator pole the inductance rises, reaching a peak as the two are fully aligned. The inductance then decreases as the rotor pole moves away from the aligned position, until no overlap exists. At this point the inductance becomes constant once again.

A further common form of Switched Reluctance motor is the 12-8, as shown in figure 3.9, which has the inductance profile shown in figure 3.10. This is again a three phase machine, but due to the doubling of pole numbers, produces a smoother torque output. This motor is

Figure 3.7: 6-4 SR Motor

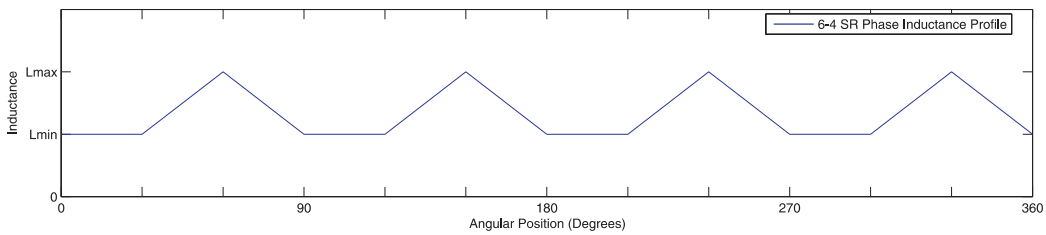

Figure 3.8: 6-4 SR Motor Phase Inductance

better suited to lower speed, higher torque applications than the 6-4.

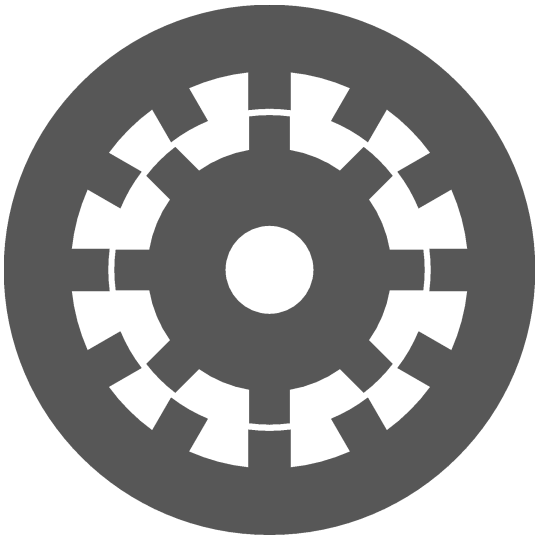

Figure 3.9: 12-8 SR Motor

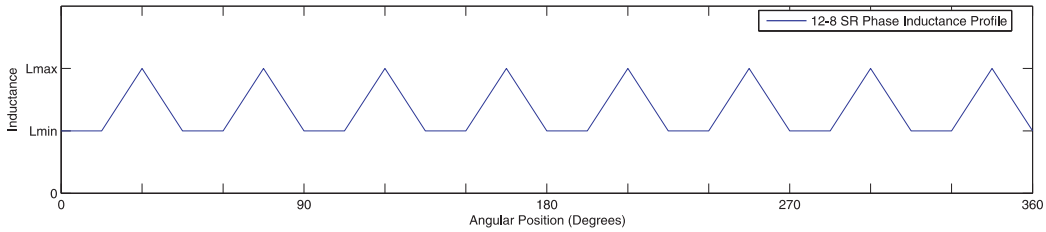

Figure 3.10: 12-8 SR Motor Phase Inductance

Motoring torque is produced by the motor when current flows in a phase which has a rising inductance, this being as the overlap between the rotor and stator poles is increasing, approaching the aligned position. Any current flowing in the phase when the poles have passed the aligned position, and the inductance is decreasing, will produce a negative or regenerative torque. This can be seen by referring to equation 3.1 which describes torque production for the linear, unsaturated SR motor. Switched reluctance motors are often operated in the non-linear magnetic region, however the torque remains a function of the square of the current.

$$T_e = \frac{1}{2} i^2 \frac{dL}{d\theta} \tag{3.1}$$

The torque being a function of current squared makes it independent of current direction and therefore ideal for use with the SSMC.

The Switched Reluctance motor makes a good choice where fault tolerance is important. The rotor has no windings or magnets, and is therefore cheap and easy to produce, and physically robust. The lack of magnets also means that the operational temperature of the motor is only restricted by the winding insulation. A further advantage is that the stator windings are of the concentrated type, thus they are simple both to wind and to assemble on the motor. This implies that a malfunction with one of the coils will not affect the other phases, and may not therefore disable the motor (depending on the number of phases).

Unfortunately, even an SR motor with a high number of rotor and stator poles produces significant torque ripple and vibration. It is possible to reduce this, with complex control of the phase currents, but not without adversely affecting the power or efficiency of the motor. The SR motor also operates most efficiently with a small airgap, which can be problematic when combined with the vibration casued by the torque ripple. Finally, SR motors generally produce a large amount of heat, which can again cause problems associated with the small air gap. This would be accentuated further if the motor were operated in a hot environment.

3.2.2 Trapezoidal Permanent Magnet DC

The trapezoidal brushless PMDC motor has a laminated rotor and stator. The rotor contains permanent magnets, whilst the stator construction is similar to that of an AC induction motor. The toothed stator has multiple phase windings, the excitation of which is synchronised with the rotor position, using either a shaft position sensor, or a sensorless method.

The arrangement of magnets on the rotor and winding distribution on the stator produce

a trapezoidal back EMF waveform within each of the phase windings as the rotor rotates. When pulses of positive and negative current are supplied to the phase windings by the power electronic converter, synchronised with the trapezoidal back EMF, the rotor rotates and produces a torque. There is clearly a limitation here associated with using a three phase brushless PMDC motor with the SSMC, as the SSMC can only supply current in one direction. Therefore only the positive (or negative) current pulses may be supplied to each phase.

An investigation into the most appropriate brushless PMDC motor configuration for use with the SSMC, in terms of producing a highly fault tolerant drive, was carried out as part of the 'Surface Actuation of Thin and Optimised Wings' (SATOW) project. This is a project undertaken between the Electrical and Electronic Engineering Department at the University of Nottingham, and Smiths Aerospace, along with a number of other universities and private companies. The SATOW project was partially funded by the UK Department of Trade and Industry (DTI) under the 'Civil Aircraft and Technology Demonstration' (CARAD) programme.

The SATOW project focussed on designing an electro hydraulic actuator (EHA) to control the ailerons on a large passenger aircraft. The ailerons are the flight control surfaces on the rear edge of the wing. Currently these use hydraulic actuators which are fed from a central hydraulic pump within the aircraft. The aerospace industry is looking to eliminate the need for the centralized hydraulic system in order to reduce the weight, and therefore fuel consumption of aircraft, as well as reducing maintenance costs.

The particular solution that the SATOW project developed uses an electric motor to drive a local hydraulic pump, which in turn drives a rotary hydraulic actuator. This type of system is known as an electro hydraulic actuator, or EHA. The alternative would be an electro mechanical actuator (EMA), which uses a purely mechanical system between the motor and the surface which is being moved. EHA's are generally favoured as, if a failure occurs with the actuator, a bypass valve can be opened allowing the hydraulic fluid to 'freewheel', with one of the auxiliary actuators taking over control of the surface. This 'freewheeling' is generally more difficult or impossible to achieve using a purely mechanical system of

gearboxes and ballscrews.

Commonly, brushless PMDC motors have three phases. Figure 3.11 gives the back EMF for a single phase winding, for both the ideal, and real cases. The winding method used on the stator implies that the back EMF should take the form of the ideal case, however in practice fringing has the effect of rounding the corners, and a trapezoidal back EMF is produced. Note that the real case data given in figure 3.11 is taken from data sampled from an actual motor, which does not produce the smooth flat tops that would normally be expected. The shape and period of the back EMF waveform is determined by the magnet arrangements, and is independent of the phase number.

Figure 3.12 shows the common phase conduction periods, assuming negative currents can be supplied. It is of course possible to rotate the motor using just the positive current pulses, although this results in only half the total current flowing into the machine, and therefore only half the torque output, compared with the same motor when supplied with both positive and negative currents. The more significant drawback of a three phase configuration, with only uni-directional current, relates to the fault tolerant capabilities of the drive. If one phase fails, the motor will only produce torque for a maximum of two thirds of each revolution. The motor would not run well in this state, and would be liable to stalling if any load were applied. Therefore, a motor configuration where at least two phases always conduct and produce torque would be preferred. This means increasing the number of phases in the machine, which in turn, unfortunately means that more power electronic switches will be required in the converter. Increasing the complexity of the converter should generally be avoided, when fault tolerance is the primary concern, as increasing the number of switches increases the probability of a failure in a single switch. Clearly there is a balance to be reached.

A four phase motor was considered. Assuming two phases conducting at any time implies a phase conduction period of 180 degrees, as can be seen in figure 3.13. For efficient operation of the motor, current should only flow in the phase during the flat part of the back EMF waveform, as given in figure 3.11. This typically spans between 120 and 150 degrees. Allowing the phase to conduct for 180 degrees, would clearly not give efficient operation

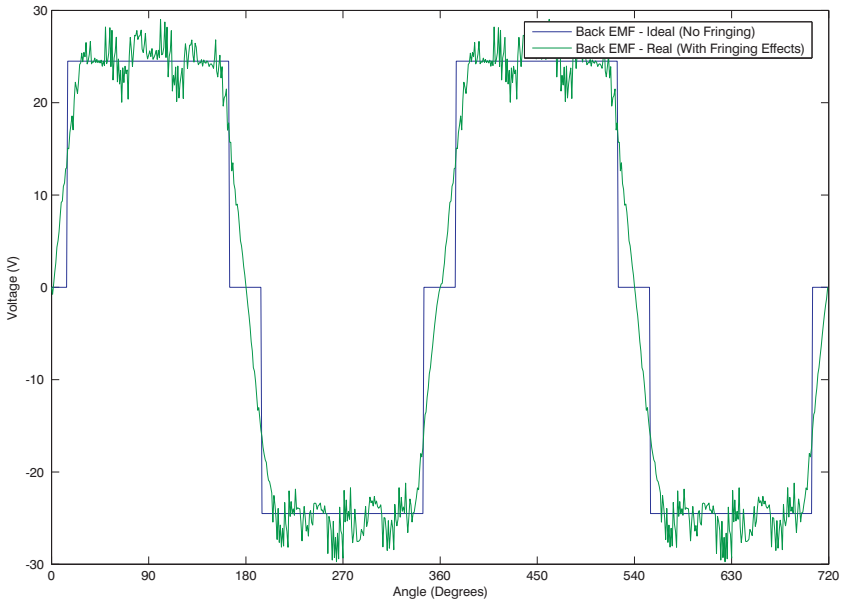

Figure 3.11: PMDC Motor Back EMF (Phase A)

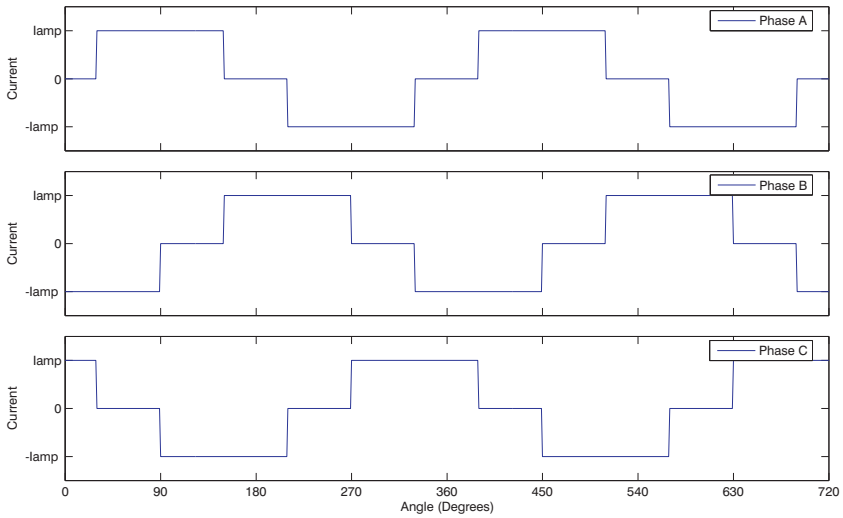

Figure 3.12: 3 Phase PMDC Motor Phase Conduction Periods

of the motor, as current would be flowing during the rising and falling sections of the back EMF, producing negligible torque. A four phase configuration would therefore not make a good choice.

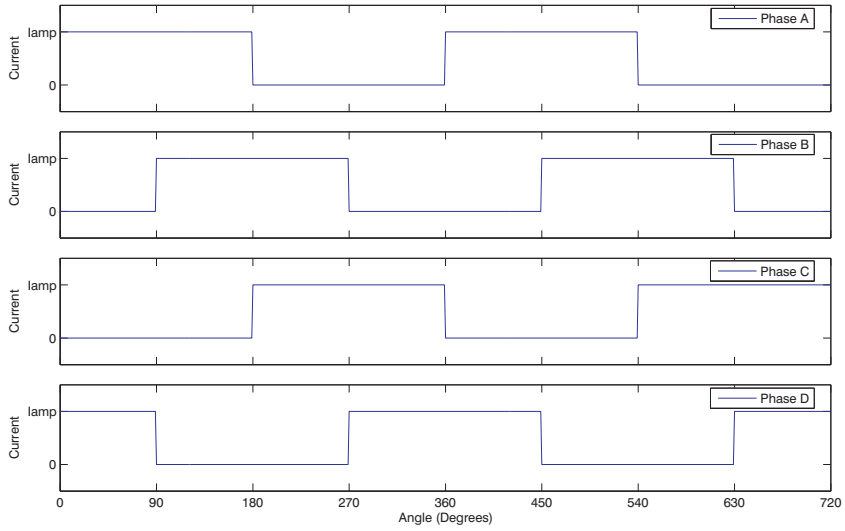

Figure 3.13: 4 Phase PMDC Conduction Periods

A five phase motor was also considered. Figure 3.14 shows the phase conduction periods necessary in order to ensure that under non-fault conditions, two phases will always conduct. Examining this will show a necessary conduction period of 144 degrees. This is within the 150 degrees that the flat part of the back EMF usually spans and therefore makes a good choice of phase number for the fault tolerant machine.

A five phase motor was designed for the SATOW [45] project. This motor was designed to run at a maximum speed of 12,000 rpm, with a peak power output of 12kW, using uni-directional currents. The resistance and inductance are as given in table 3.1, while the motor itself can be seen in figure 3.15.

Phase Resistance (ohms)	0.121
Phase Inductance (mH)	0.55

Table 3.1: Five Phase PMDC Motor Characteristics

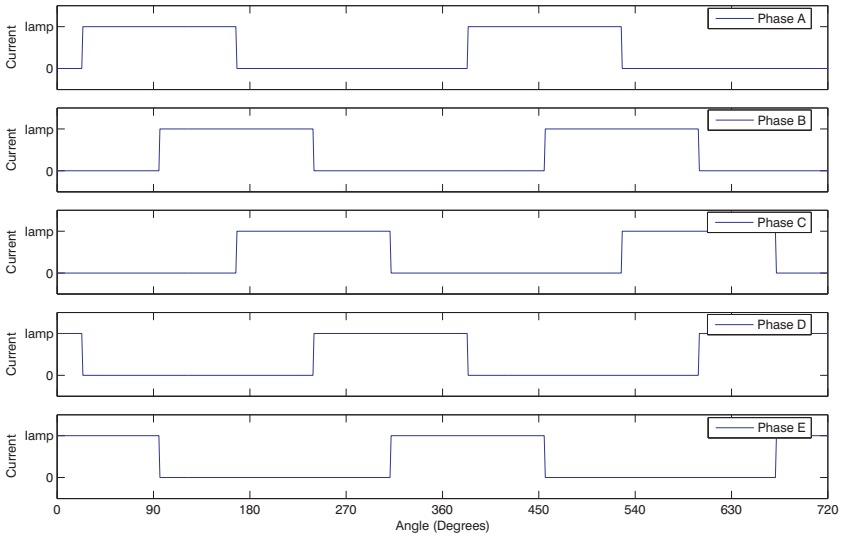

Figure 3.14: 5 Phase PMDC Conduction Periods

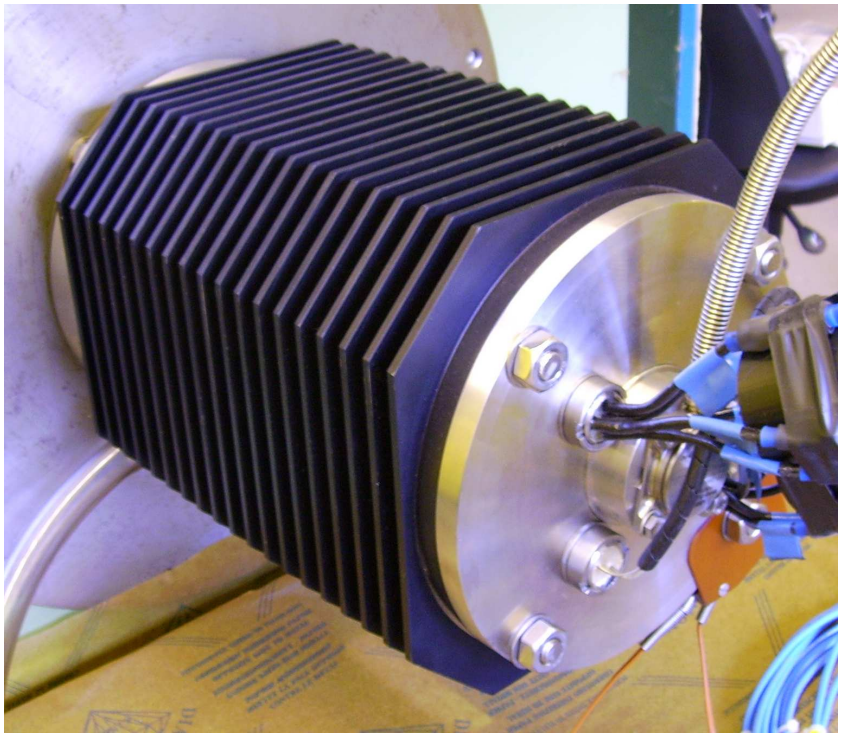

Figure 3.15: SATOW PMDC Motor Photo

3.3 Summary

This chapter has introduced the novel single sided matrix converter. Two control strategies have been proposed namely the single band, and novel double band techniques, and consideration has been given to the most appropriate way in which to implement the control. The result of this is that an FPGA is the favoured platform due to the reliable, predictable way in which they operate, and the suitability of such a chip for implementation of the logic based control schemes.

Finally, consideration has been given to the types of motor with which the SSMC could be used. The two most suitable motors have been identified as the switched reluctance motor, and the trapezoidal PMDC machine, with both being strong contenders for use in high reliability, fault tolerant drives.

Chapter 4

Single Sided Matrix Converter Simulation

Simulations were performed using the Simpower block set within the Simulink environment of Matlab, in order to verify the operation of the SSMC using both the single and double band control schemes proposed. This involved modelling both the converter and the motors with which it was to be used. Initial simulations were performed for a three phase input, single phase output converter, feeding a load including both inductive and resistive elements. Once operation of both control schemes had been verified, the models were expanded to include additional output phase legs, and to drive both a simplified model of a 3 phase Switched Reluctance motor and, as part of the SATOW project, a 5 phase trapezoidal Permanent Magnet DC motor. The Switched Reluctance motor and single and double band SSMC controller models used, along with the results obtained for operation with both motors, are presented in the following sections of this chapter. The definitions of the logic signals used here were first proposed in [46].

4.1 Switched Reluctance Motor Model

Accurate simulation of the operation of a Switched Reluctance motor requires a complex model [47] [48]. These motors are normally operated in the non-linear region of the magnetic characteristic curve of the steel, making in-depth knowledge of the specific motor being used necessary for such a model. At the time that the simulations were performed, the version of Simulink being used did not include a Switched Reluctance motor model. The specifics of the motor finally used to test the experimental SSMC were also unknown at this point, so another SR motor was used as the basis for the simulations. This was a 6/4 SR motor, with the properties as given in table 4.1. The motor can be seen in figure 4.1.

Phase Resistance (ohms)	0.8163
Aligned Inductance (mH)	0.015
Unaligned Inductance (mH)	0.0032

Table 4.1: Simulated Switched Reluctance Motor Characteristics

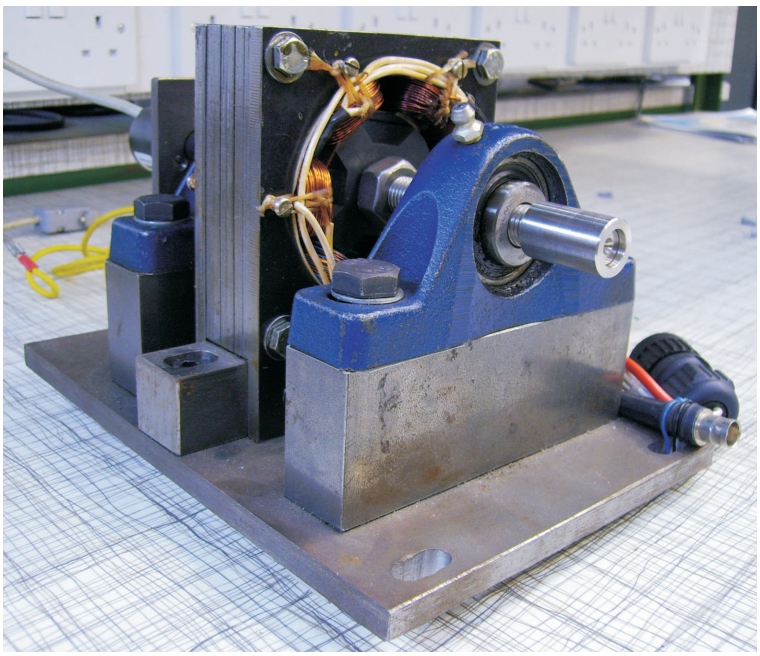

Figure 4.1: Simulated SR Motor Photo.

As the primary reason for performing the simulations was to verify the operation of the

SSMC, and the control schemes proposed, it was decided that simulations based on a simple linear model of the electrical characteristics of the Switched Reluctance motor would be sufficient, if it can be assumed that the motor supply characteristics ensure operation within the linear magnetic region of the steel. The linear model used was based on equation 4.1, which models the resistive, inductive and back EMF elements of the phase respectively.

$$V_P = iR + L\frac{di}{dt} + \omega i\frac{dL}{d\theta} \tag{4.1}$$

Where

V_P = Phase Voltage
i = Phase Current
R = Phase Resistance
L = Phase Inductance
ω = Rotor Rotational Velocity
θ = Rotor Angular Position

The block used within Simulink to simulate the motor can be seen in figure 4.2. The resistive element of the phase is simply modelled using a resistor. The inductive element is modelled as in figure 4.3. This is an implementation of equation 4.2, discretised to give equation 4.3. The step time block at the left of figure 4.3 is the fixed step time used by the solver ie. Δt. The 'Inductance Lookup L' block is a lookup table representing the changing inductance values with position. This has been determined for the fixed speed produced by the specific current level and switching angles, and was obtained experimentally.

$$V_L = L\frac{di}{dt} \tag{4.2}$$

Where

V_L = Inductive Voltage Element
i = Phase Current
L = Phase Inductance

$$i_{(t)} = \frac{V_L \Delta t}{L} + i_{(t-1)} \tag{4.3}$$

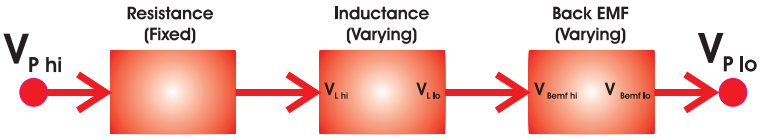

Figure 4.2: Linear Switched Reluctance Motor Model.

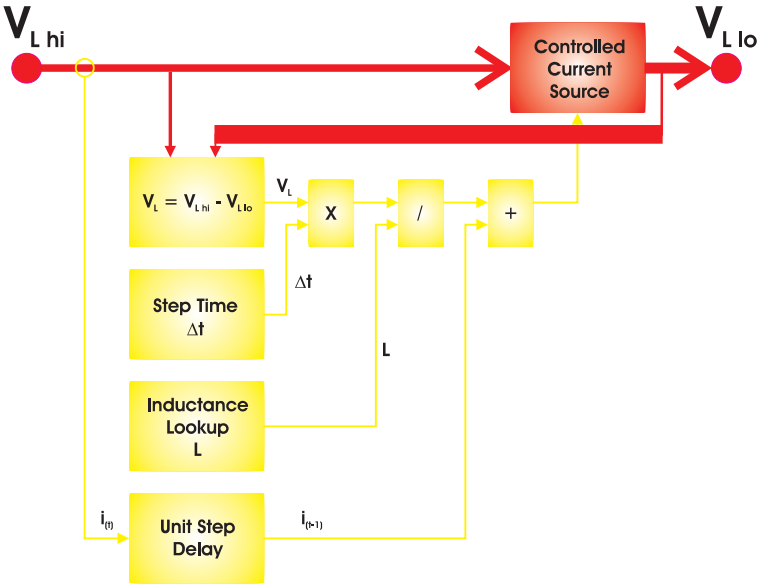

Figure 4.3: Linear Switched Reluctance Motor Model - Controlled Inductance.

The Back EMF Element of the Switched Reluctance motor phase is modelled as in figure 4.4. Referring back to equation 4.1, one can see that the Back EMF is as in equation 4.4. The model implements equation 4.4 in the form of equation 4.5.

$$V_{Bemf} = \omega i \frac{dL}{d\theta} \tag{4.4}$$

Where

V_{Bemf} = Phase Back EMF

i = Phase Current

L = Phase Inductance

ω = Rotor Rotational Velocity

θ = Rotor Angular Position

$$V_{Bemf} = \omega i \frac{dL}{dt} \frac{dt}{d\theta} \tag{4.5}$$

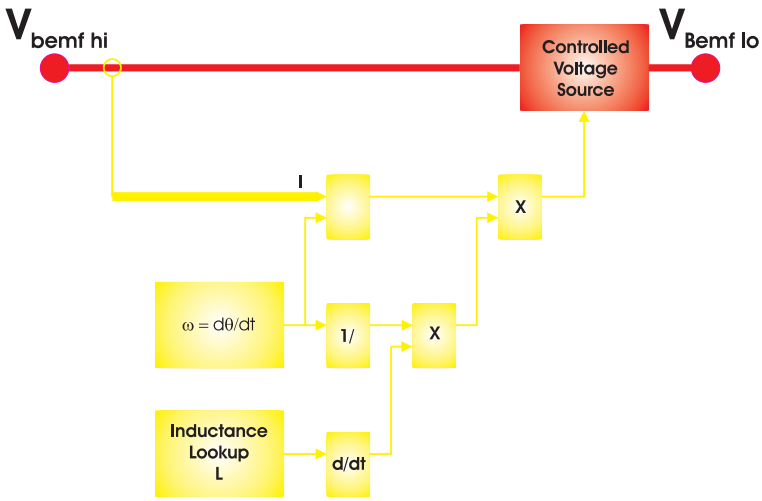

Figure 4.4: Linear Switched Reluctance Motor Model - Back EMF.

The model operates based on knowledge of the speed obtained for a specific 6-4 3-phase Switched Reluctance motor, operated at specific current levels and switching angles. The motor has the characteristics given in table 4.1, while table 4.2 shows the unloaded speeds obtained for the specific current limit levels and switching angles. Both the switch on and switch off angles are measured from the fully aligned position, this being when the rotor pole is fully aligned with the stator pole of the phase being considered.

Current Limit (A)	Switching Angles (degrees)		Speed (rpm)
	Turn On	Turn Off	
2.3	30	0	530
3.4	50	10	3080

Table 4.2: Switched Reluctance Motor Experimental Data - Simulated Motor

The flux linkage against current curves for the motor being considered are given in figure 4.5. These were obtained experimentally. Comparing the currents used in table 4.2 with figure 4.5 validates the assumption that the motor is operated in the linear magnetic region of the steel.

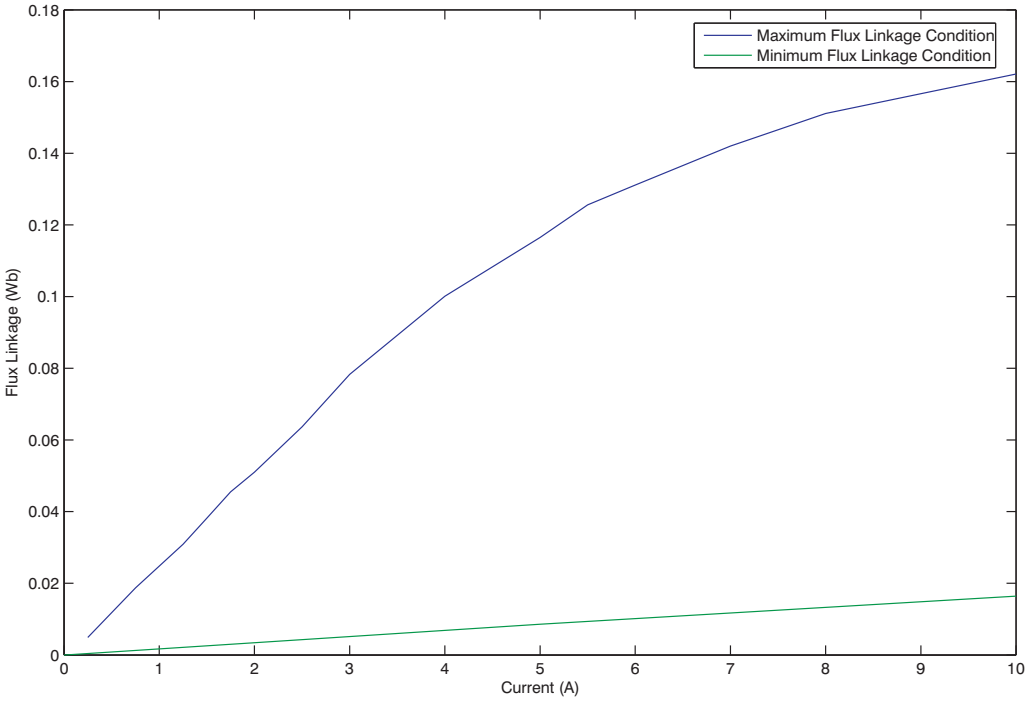

Figure 4.5: Flux Linkage against Current Curve for Simulated Motor.

The Switched Reluctance motor model was verified by simulating it with a model of the drive which had been used to power the motor, and obtain the data in table 4.2. Figure 4.6 and figure 4.7 present the current waveforms for a single current pulse, and show the good match obtained between the experimental and simulation results at the two speeds.

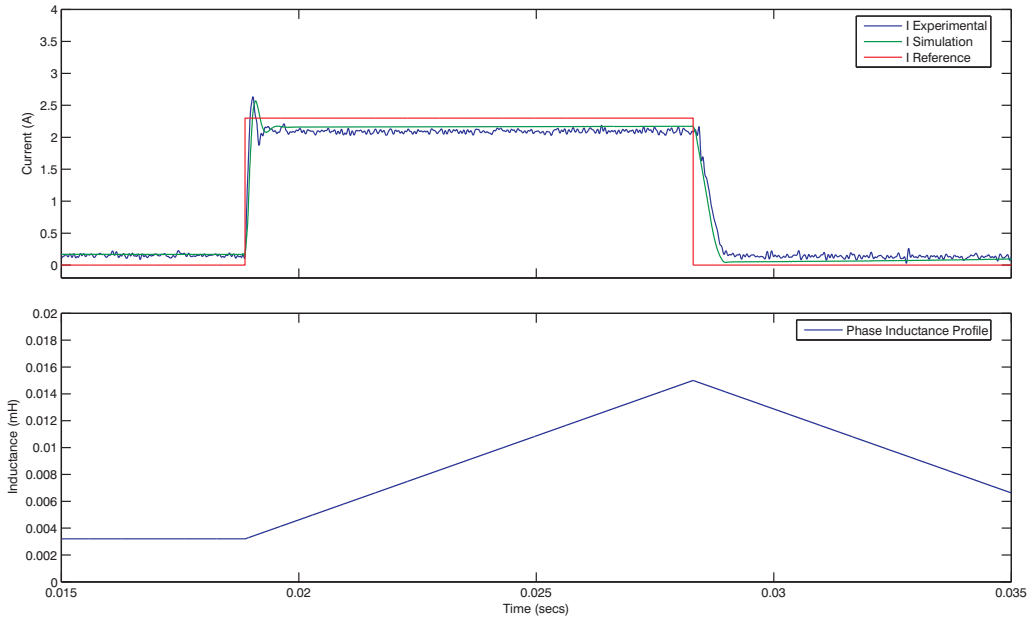

Figure 4.6: Linear Switched Reluctance Motor Model Verification - 530 rpm.

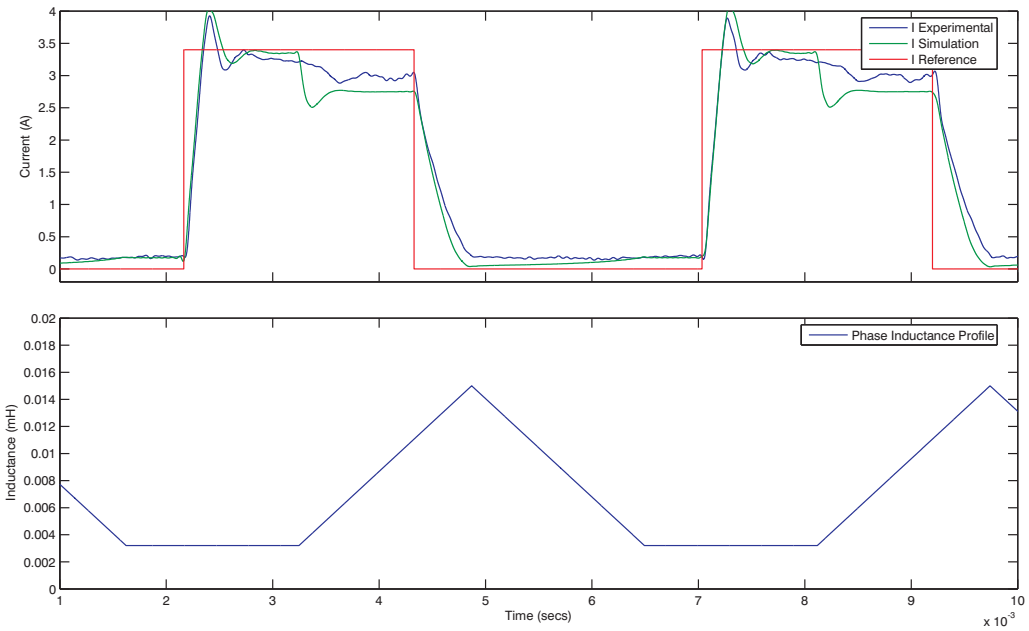

Figure 4.7: Linear Switched Reluctance Motor Model Verification - 3080 rpm.

4.2 Trapezoidal PMDC Motor Model

The simulations performed for the trapezoidal PMDC motor were undertaken by Xiaoyan Huang as part of the SATOW project [45]. The model used is an implementation of the basic equation describing the electrical behaviour of the trapezoidal PMDC motor, as given in equation 4.6. A schematic showing the way in which the equation is implemented in Simulink can be seen in figure 4.8.

$$V = IR + L\frac{di}{dt} + E_{BEMF} \tag{4.6}$$

The resistive and inductive elements are simply modelled using series RLC branches within Simulink. The back EMF is generated using a controlled voltage source, taking a back EMF reference signal as its input. This back EMF signal is acquired from a lookup table, which converts time values to back EMF voltages. The lookup table was produced from

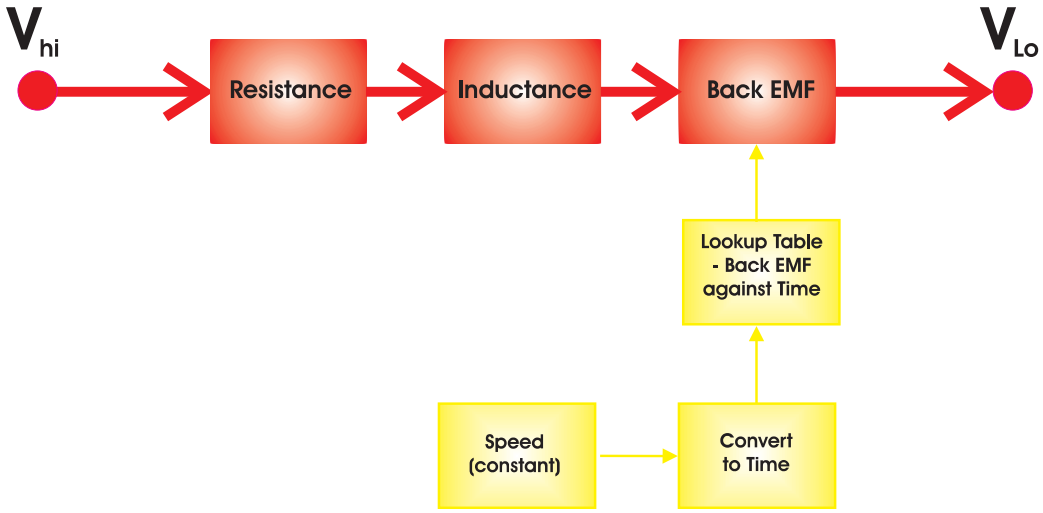

Figure 4.8: Trapezoidal PMDC Motor Model Schematic.

a detailed finite element simulation performed as part of the motor design procedure. The finite element analysis was undertaken using MagNet software produced by Infolytica. The back EMF profile can be seen in figure 4.9.

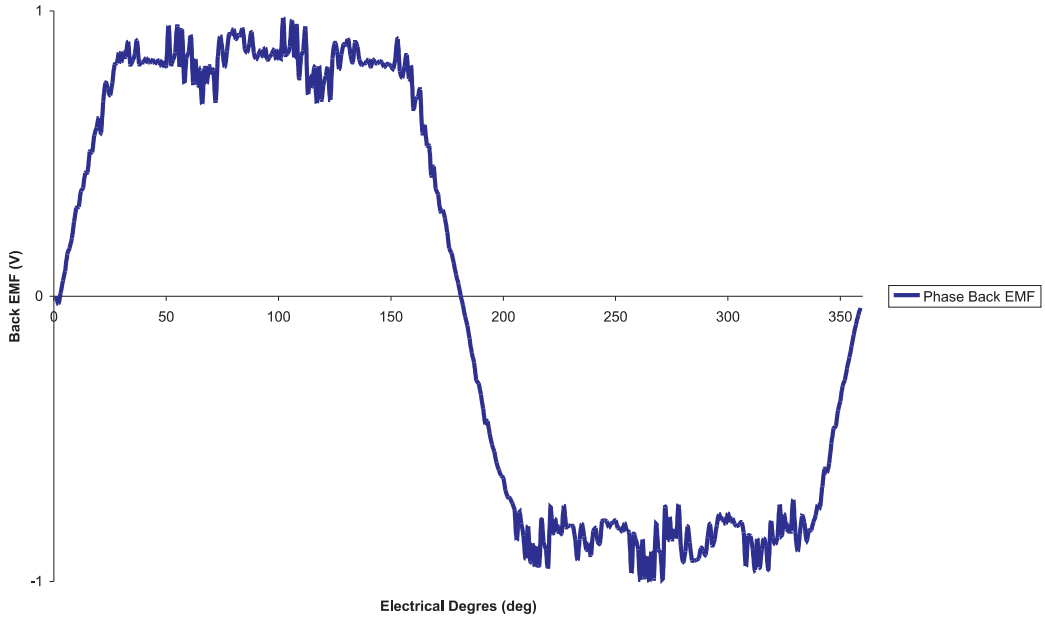

Figure 4.9: Trapezoidal PMDC motor Back EMF Profile from MagNet Simulation.

4.3 Single Band Controller Model

The SSMC single band current controller main control block can be seen in figure 4.10. The input signals to the controller are the X,Y,Z signals denoting the input phase voltage states, the current reference/demand and current feedback signals, and the value for half the hysteresis band width. The only outputs from the controller are the six IGBT gate drive signals, labelled as in figure 3.1.

Firstly the current error is calculated. This, along with the band half signal are then fed into the hysteresis band block, which determines the state of the error, with respect to the hysteresis band. The contents of the hysteresis band block can be seen in figure 4.11. The error signal is compared with both the band half signal, and the inverted band half signal. In this way, the full band width is created - half being positive and half being negative, with ideally an error signal of zero when the current is at the demand value. The two outputs of the hysteresis band block are termed U1 and U2, with U1 representing the upper level of the hysteresis band and U2 representing the lower level. The logic values representing the

states are given in table 4.3

U1	U2	State
0	0	Error Below Band
0	1	Error Within Band
1	0	Impossible State
1	1	Error Above Band

Table 4.3: SB - Hysteresis Band Block Output Signal States

The outputs from the hysteresis band block are fed into the voltage level identifier block, figure 4.12. This block determines whether the most positive or most negative voltage should be applied, based on the current and previous states of U1 and U2, as in table 4.4

U1	U2	Q1'	Q2'	Q1	Q2
0	0	X	X	1	1
0	1	0	1	0	0
1	1	X	X	0	0
0	1	1	0	1	1

Table 4.4: SB - Voltage Level Identifier Truth Table

The final block in the single band control scheme is the Gating Signal Circuit Block, as given in figure 4.13. This takes as its inputs signals Q1 and Q2, as well as the X,Y,Z signals representing the input voltage state. The first half of the block (the logic based section) determines which 2 of the IGBT's should be turned on assuming a positive voltage is required out of the converter, causing an increase in current. The Gating Signal Logic block then applies the truth table in table B.1 in appendix B, which takes into account the polarity of the output voltage required. Finally, the IGBT gate drive signals are output from the Gating Signal Circuit block, and then the Single Band Controller block.

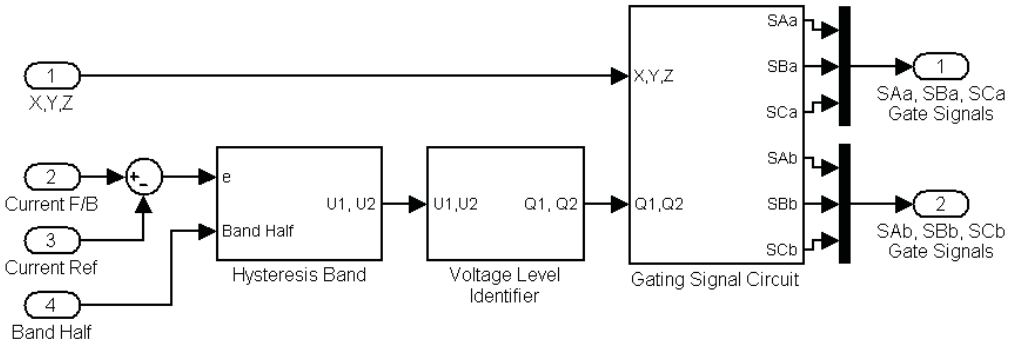

Figure 4.10: Single Band Controller - Top Level.

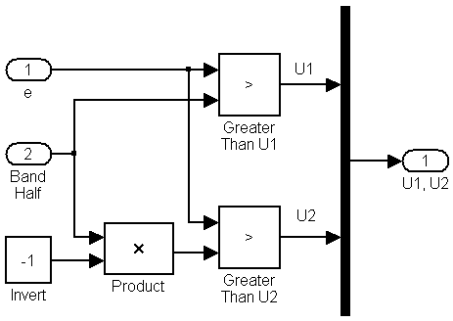

Figure 4.11: Single Band Controller - Hysteresis Band.

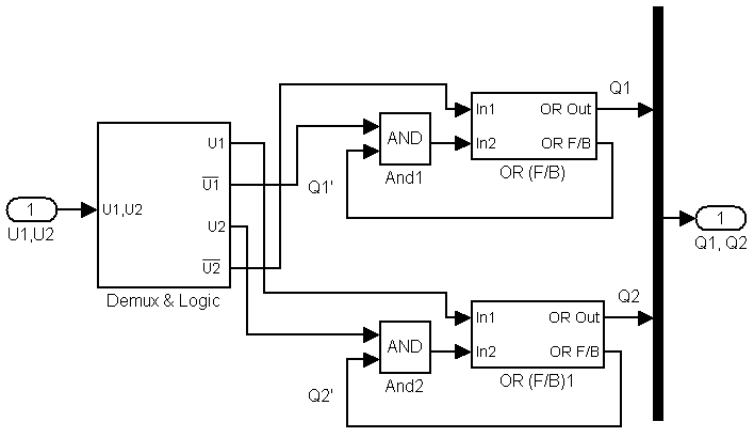

Figure 4.12: Single Band Controller - Voltage Level Identifier.

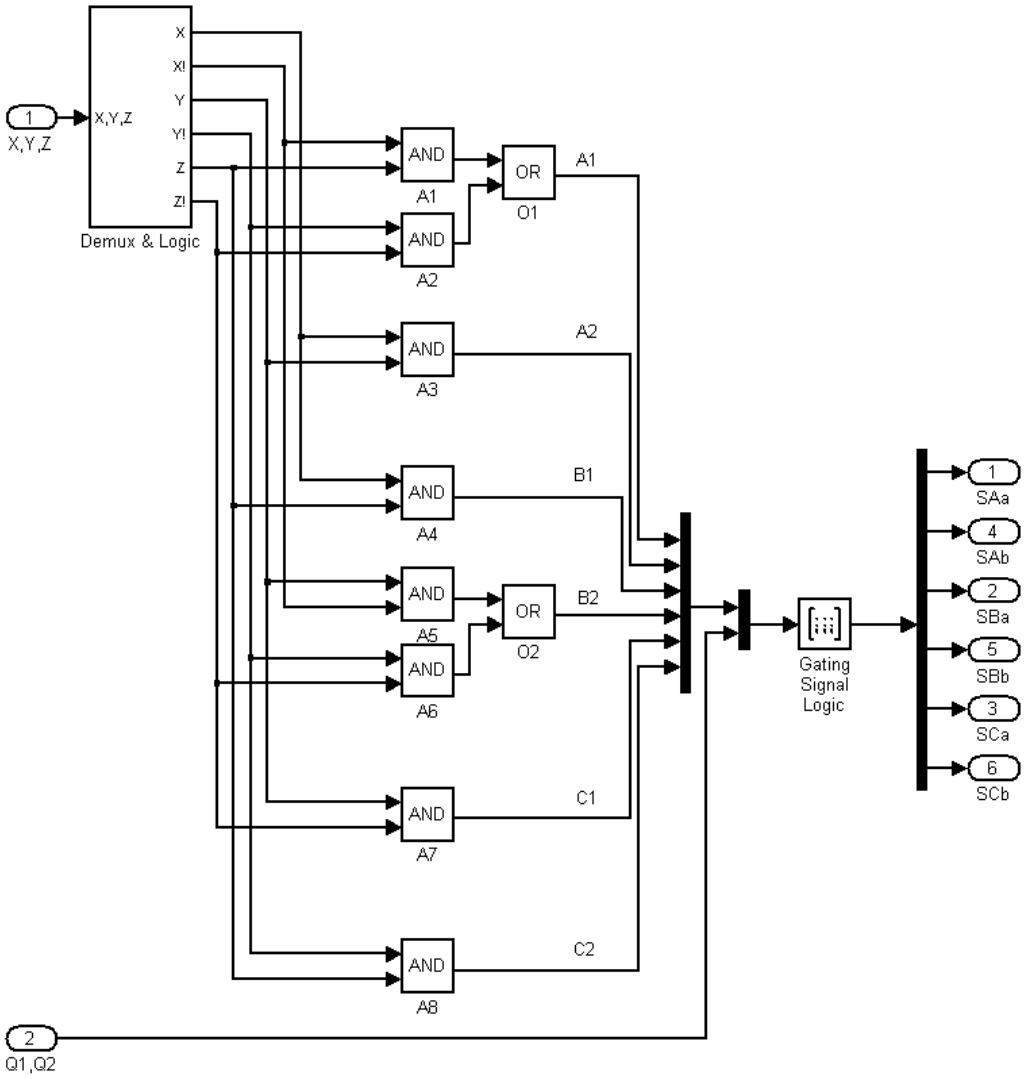

Figure 4.13: Single Band Controller - Gating Signal Circuit.

4.4 Double Band Controller Model

The double band controller is constructed as in figure 4.14. This has a very similar structure to the single band controller, however five additional input signals are present. Signals A,B,C supply additional information regarding the input voltage state, this being whether each of the input voltages is positive or negative, with a 1 indicating a positive voltage. The fourth additional input is the half value for the second hysteresis band, while the fifth is the clock used by the stepping mechanism in the double band controller.

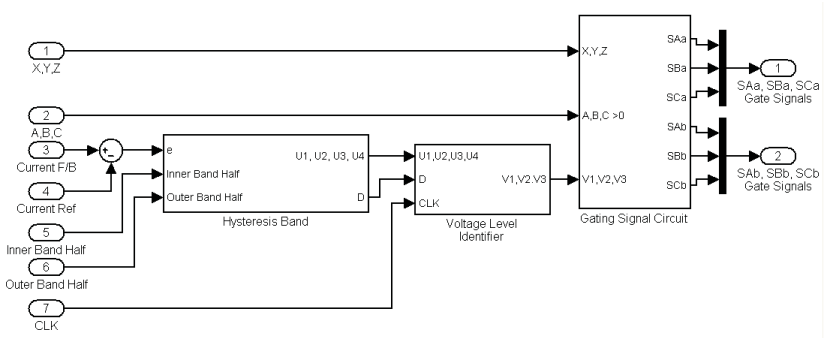

Figure 4.14: Double Band Controller - Top Level.

Initially, the current error signal is calculated. This is then fed into the Hysteresis band block, as shown in figure 4.15, along with the two hysteresis band half values. Five signals are then derived. Signal D represents the direction of change of current, and is calculated by differentiating the error signal, and comparing it with zero, to produce a logic signal. the other four signals determine the state of the error signal with respect to the two hysteresis bands, as given in table 4.5.

The Voltage Level identifer block then follows, as shown in figure 4.16. One can see that all input states are fed into a combinatorial logic block, along with the previous output states. A triggered subsystem block is used to introduce the stepping clock, used to step the voltage levels up and down, when the error signal is within the outer hysteresis band. The truth table used by the combinatorial logic block is available in table C.1 in appendix C. The output signals, V1, V2, V3 are a logic representation of the desired output voltage

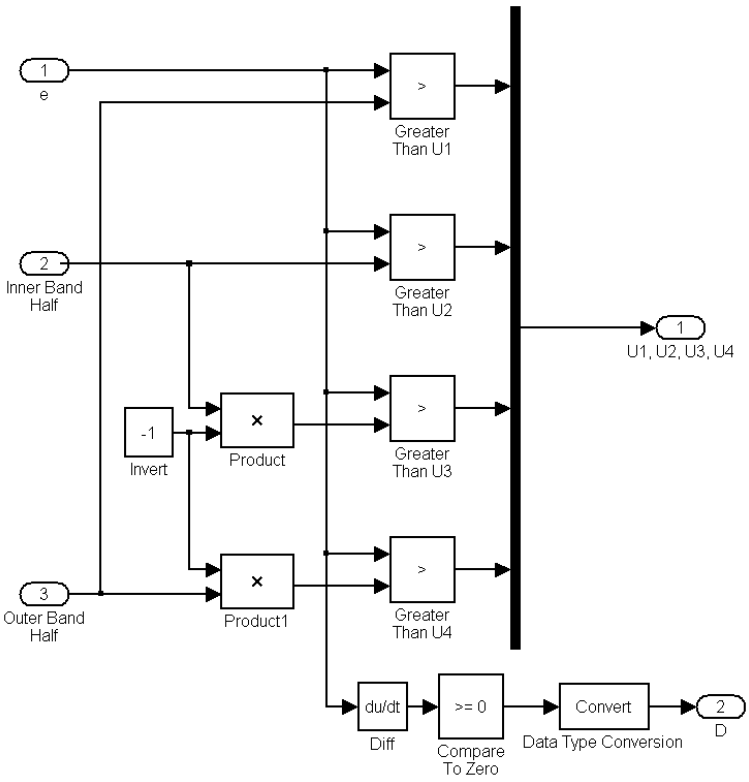

Figure 4.15: Double Band Controller - Hysteresis Band.

U1	U2	U3	U4	Error State
0	0	0	0	Below Outer Band
0	0	0	1	Between Lower Inner band and Lower Outer Band Limits
0	0	1	1	Within Inner Band
0	1	1	1	Between Upper Inner Band and Upper Outer Band Limit
1	1	1	1	Above Outer Band

Table 4.5: DB - Hysteresis Band Block Output Signal States

level, as given in table 4.6.

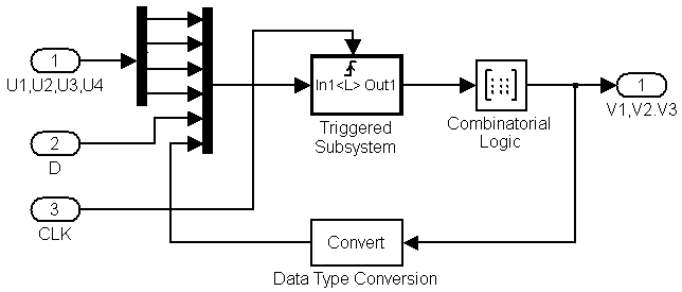

Figure 4.16: Double Band Controller - Voltage Level Identifier.

Output Voltage Level	V1	V2	V3
V+3	0	0	0
V+2	0	0	1
V+1	0	1	1
V0	0	1	0
V-1	1	1	0
V-2	1	0	0
V-3	1	0	1

Table 4.6: DB - Voltage Level Coding Logic

The final block is the Gating Signal Circuit, which compares the desired output voltage level with the input voltage states, in order to determine the required IGBT gating signals. The operation of this block is separated into two halves, both of which are implemented by a combinatorial logic block. the first of these is the Gating Signal Logic block, which implements the truth table given in table C.2 in appendix C. The intermediary signals produced here are termed U, A, B and C. The letters A, B and C refer to the input phases

A, B and C respectively, and the logic signals produced represent the two phases which should be connected across the load. For example A=1 , B=1 , C=0 would imply that input phases A and B should be used. The third signal, U represents the direction in which the input voltages should be connected across the load. These four signals are finally decoded by the Switch Logic combinatorial logic block, producing the double band controller IGBT gating signals. The truth table for this block is available in table C.3 in appendix C.

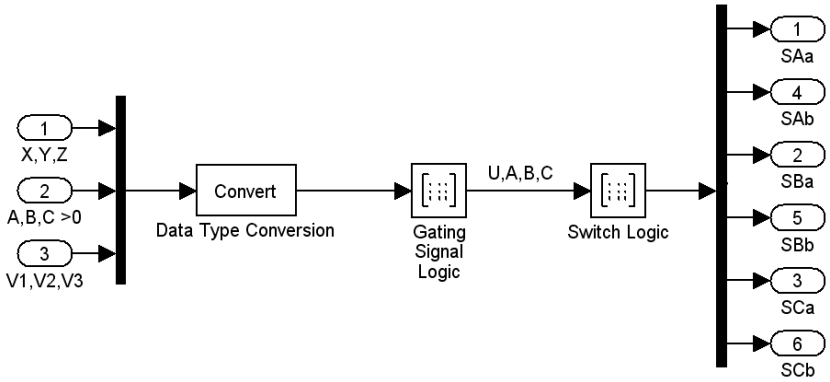

Figure 4.17: Double Band Controller - Gating Signal Circuit.

4.5 Inductive/Resistive Load

The aim of the initial simulations was to test the operation of the proposed control schemes for the SSMC. For this reason a simple load was used with a fixed resistance and inductance. The properties of this load are given in table 4.7. The first set of simulation results presented are of the single band control scheme, followed by those of the double band scheme. In both cases the hysteresis bands were sized to give an IGBT switching frequency of approximately 10kHz. The supply voltage used is 110V rms phase to neutral at a frequency of 50Hz.

Load Resistance (ohms)	0.8163
Load Inductance (mH)	0.01

Table 4.7: Inductive Load Characteristics

4.5.1 Pulsed Output Current

Presented first are simulation results for a pulsed output current demand, using the inductive/resistive load. The intention is to demonstrate the ability of each control scheme to control the output current around the demand value. In addition, explanations of the operation of each control scheme are given with, finally, a visual comparison of the output current quality for each scheme.

As can be seen in figure 4.18a, the single band control scheme correctly controls the output current of the converter around a reference value. Figure 4.18b shows the current error signal, along with the single hysteresis band, whilst figure 4.18c shows the voltage applied to the load at the output of the converter.

When the demanded current is zero, the error signal is central within the 2 bounds of the hysteresis band. During this time the most negative of the supply phases is always connected across the output of the converter as can be seen, however while the current is zero, the output stage diodes are reverse biassed and the load actually sees zero voltage across its terminals. Once a positive current demand is applied, the error signal becomes negative, leaving the hysteresis band, and the most positive voltage available is applied. The current then rises until the error signal comes within the band and reaches the top bound. At this point the inputs are switched and the most negative voltage is applied. This sequence continues whilst the demand signal is positive, in this case maintaining the current around the 25 amp demand. Once the demand signal drops to zero, the error signal again leaves the band, this time to the positive side, and the most negative voltage is therefore applied. Clearly the rate of change of current with the single band method is dependant only upon the supply voltage and the inductance of the load.

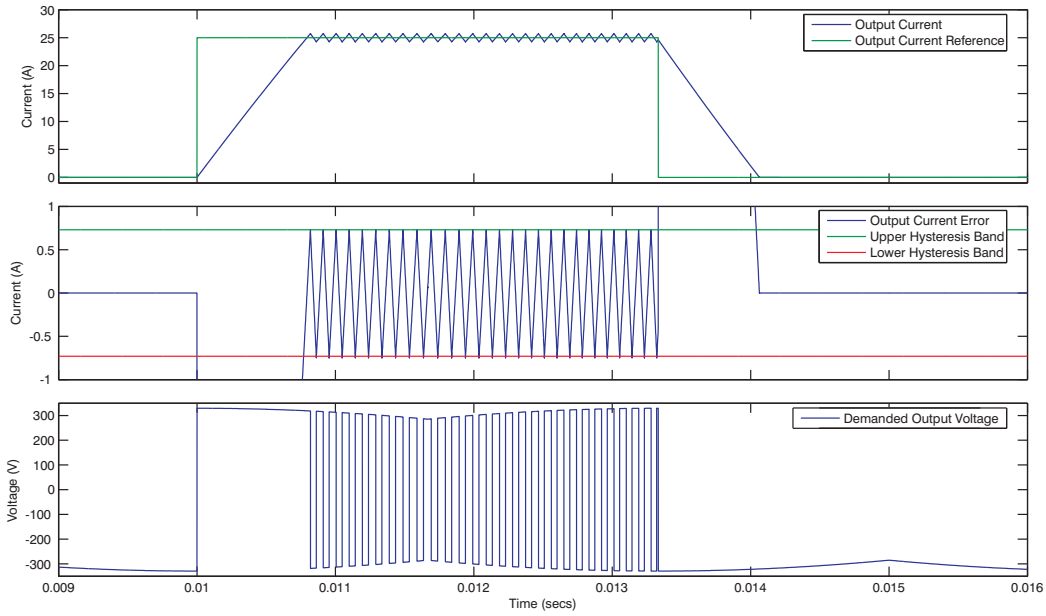

Figure 4.18: RL Load, SB Control, Pulsed Output a, Output Current with Reference. b, Output Current Error with Hysteresis Band. c, Demanded Output Voltage.

Presented in figure 4.19 are the results for the same supply and load conditions as in figure 4.18, however in this case using the double band control scheme. The actual and reference currents can be seen in figure 4.19a. Note that this is for the same amplitude and period as in figure 4.18. Figure 4.19b shows the current error signal, along with both the inner and outer hysteresis bands. Note here that the outer band is the same width as that of the band used with the single band control scheme in figure 4.18. Figure 4.19c presents the voltage applied at the output of the SSMC, while figure 4.19d shows the respective voltage level applied (ranging from +3 for the most positive voltage level, to -3 for the most negative voltage level, in integer increments). These voltage levels correspond to the actual voltages available by connecting the two ends of the load to different supply phases, as given in figure 3.4.

In this case, when an output current of zero is required, the demand is actually set to be a large negative value. This is the way in which both control schemes were actually implemented in the experimental converter, and is done to ensure that any small measurement inaccuracies would not lead to erroneous switching. For this reason, the error

signal stays high above the hysteresis bands when zero current is required, and voltage level V-3 is used, ensuring that the most negative supply voltage is applied across the load. When the demand becomes positive at t=0.01, the error signal crosses through the hysteresis bands, and on passing the lower level of the outer hysteresis band, voltage level V+3 is immediately applied, connecting the most positive supply voltage across the load. The current then begins to rise, and at approximately t=0.0108 the error signal passes back within the outer hysteresis band. Voltage level V+3 is maintained until the error signal passes the upper level of the inner hysteresis band. At this point, the voltage levels are stepped down until the output current begins to decrease. In this case this occurs once level V0 is applied. This voltage level is maintained until the current reaches the lower level of the inner band, at which point the voltage level is stepped up, one level at a time, until a change in direction of change of output current is observed. In this case this occurs when voltage level V+1 is applied. This process continues for the period of positive demand current. Interestingly here, one can see that as time increases, the amplitude of voltage level V+1 decreases linearly towards zero, as can be observed in figure 3.4, reaching zero in this simulation at approximately t=0.0117. Because of this, level V+1 becomes incapable of maintaining the error signal within the inner band, and several short pulses of level V+2 are applied, with a drop to level V+1 being enough to see the current begin to decrease. From approximately t=0.012, level V+1 has increased to the point where it is great enough to create an increase in current again. From this point on, the voltage levels switch between V+1 and V0, with the periods of application of positive voltage decreasing as the amplitude of level V+1 increases. Once the required current switches to zero, the demand becomes negative and the current error immediately passes above the upper level of the outer band. At this point, level V-3 is selected and the most negative supply voltage is applied across the load, ensuring the most rapid decrease of current.

Presented in figure 4.20 is a direct comparison of the output current seen using both the single band (4.20a) and the double band (4.20b) control. As mentioned previously, the hysteresis bands in both cases were configured to give an average IGBT switching frequency of approximately 10kHz. One can see that as the double band control scheme generally applies lower voltages across the load in order to maintain the required current, a much tighter inner hysteresis band can be used than the band used in the single band

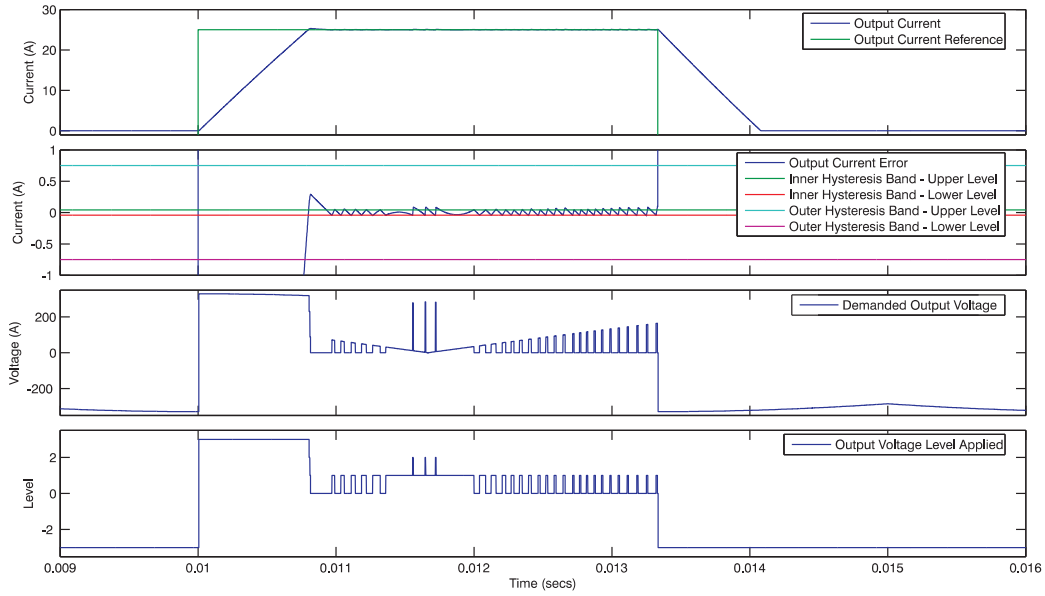

Figure 4.19: RL Load, DB Control, Pulsed Output a, Output Current with Reference. b, Output Current Error with Hysteresis Bands. c, Applied Output Voltage. d, Applied Output Voltage level.

scheme. The highest voltage level is however still available, allowing the tracking of large demand changes in the same way as with the single band scheme.

4.5.2 Continuous Output Current

This section presents the simulation results for a continuous output current demand, as is shown in figure 4.21, using identical supply and load conditions as for the pulsed output simulations. Again, the hysteresis bands have been set to achieve an average output switching frequency of 10kHz.

The continuous output current allows for the distribution of current between the input phases to be observed, as is presented for one input phase in figure 4.22. With the single band method, shown in figure 4.22a, the similarity of the current waveform with that of a diode bridge rectifier is visible, as current is only drawn from that phase when its voltage

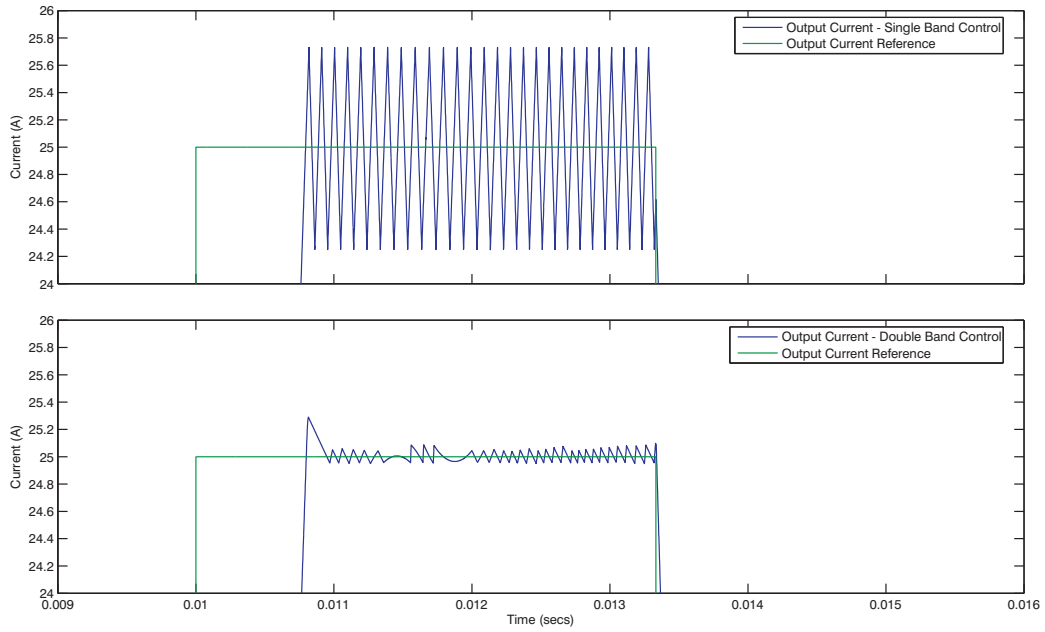

Figure 4.20: RL Load, Pulsed Output Current with Reference a, SB Control. b, DB Control.

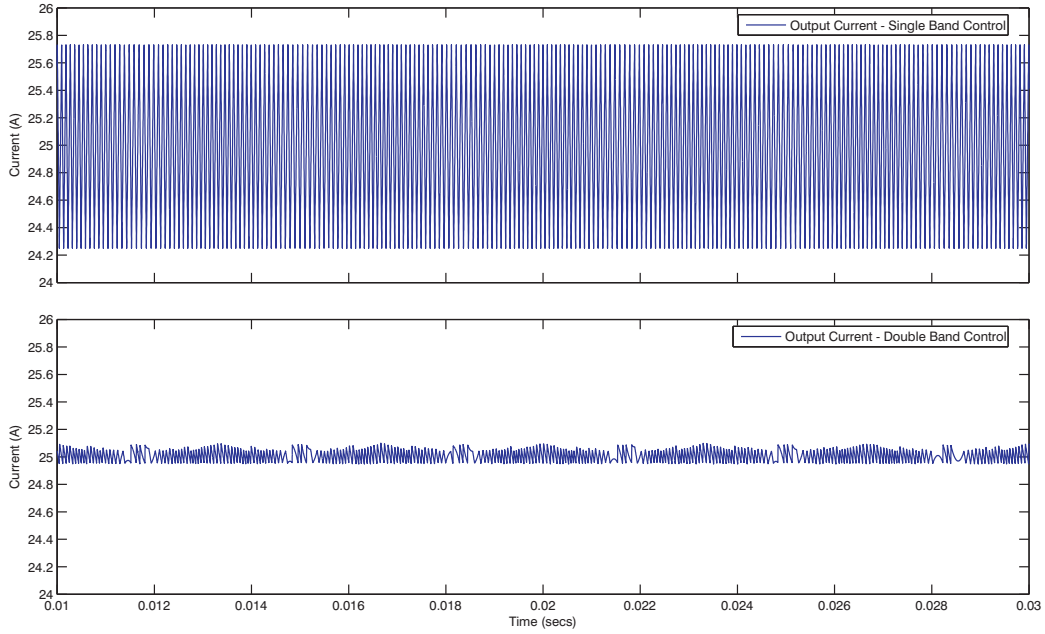

Figure 4.21: RL Load, Continuous Output Current with Reference a, SB Control. b, DB Control.

is greater than that of the other phases. There are however high frequency switching components, due to the hysteretic switching of the output currents. These high frequency switching components would normally be filtered out by a lineside filter, as in a standard matrix converter.

Presented in figure 4.22b are the input voltage and current waveforms for the double band control scheme. One can see here that the current is generally drawn from the supply at the point where the phase voltage is lower, as the voltage level applied at the output of the converter will either be zero, 1 or 2, as was shown in figure 4.19d.

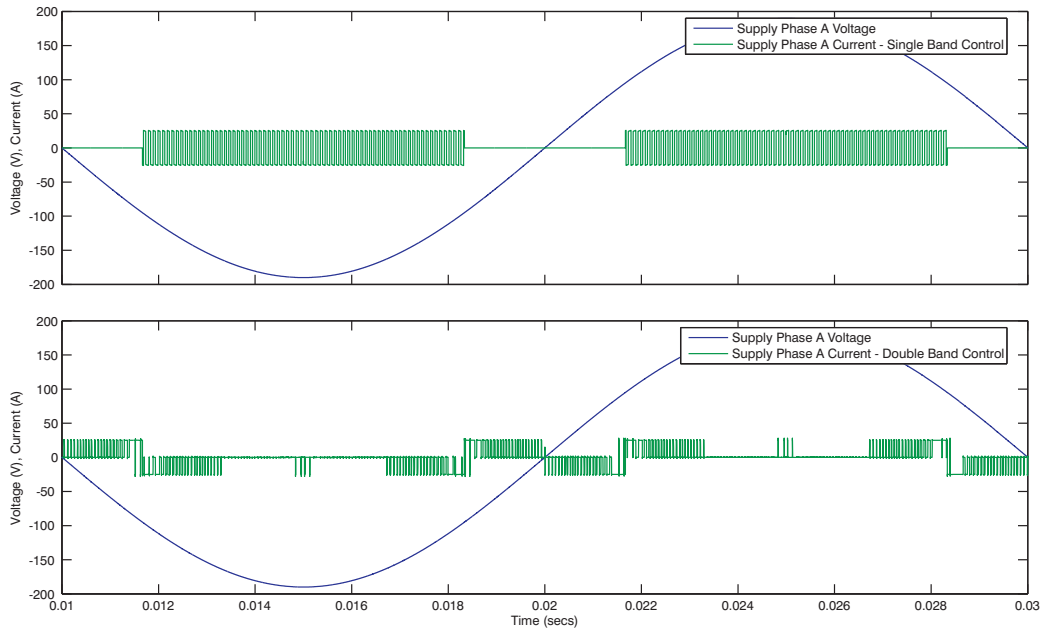

Figure 4.22: RL Load, Continuous Output Current, Input Voltage and Current a, SB Control. b, DB Control.

4.5.3 Fourier Analysis of Pulsed Current in RL Load

It is clear from figure 4.22 that using either the single or double band control schemes, and irrespective of the type of load, the input current to the SSMC is not sinusoidal. This is the unfortunate consequence of using a simple control scheme to provide good control

of output currents. For this reason, a number of Fourier analyses of the supply phase currents are presented, using the inductive/resistive load with pulsed output currents on three phases, in order to get a feeling for the harmonics present, and the effect of varying the pulse periods (which is the effect differing motor speeds have) on the harmonic content. These are presented in the following sections.

4.5.3.1 Single Band Control

Presented here are results of input current Fourier analyses for four conditions of operation of the SSMC, using the single band control scheme. The conditions are as in table 4.8. Figures 4.23, 4.24, 4.25 and 4.26 show the input voltage and current for one input phase, along with the output current reference and output current of the three output phases, for each of the conditions.

Case	Pulse Period (ms)	Current Band Width (A)	Approx Switching Frequency (kHz)
1	3.33	1.46	10.5
2	1.67	1.46	10.5
3	1.11	1.46	10.5
4	3.33	2.92	5.25

Table 4.8: Fourier Analysis Single Band Simulation Conditions

Figures 4.27 to 4.34 then present the Fourier analyses for the respective input currents. Plots of both the first 25 and the first 400 harmonics are shown for each case, showing the effect on both low and high frequencies.

Firstly, comparing the low frequency ranges for the three different pulse periods (cases 1,2,3), as given in figures 4.27, 4.29 and 4.31, one can see that as the pulse period decreases, the fundamental component also decreases. Also, the low harmonics generally decrease, and the higher harmonics (within this low frequency range) increase. Notably, the amplitude of the fundamental is, in all cases comparable with or lower than the other

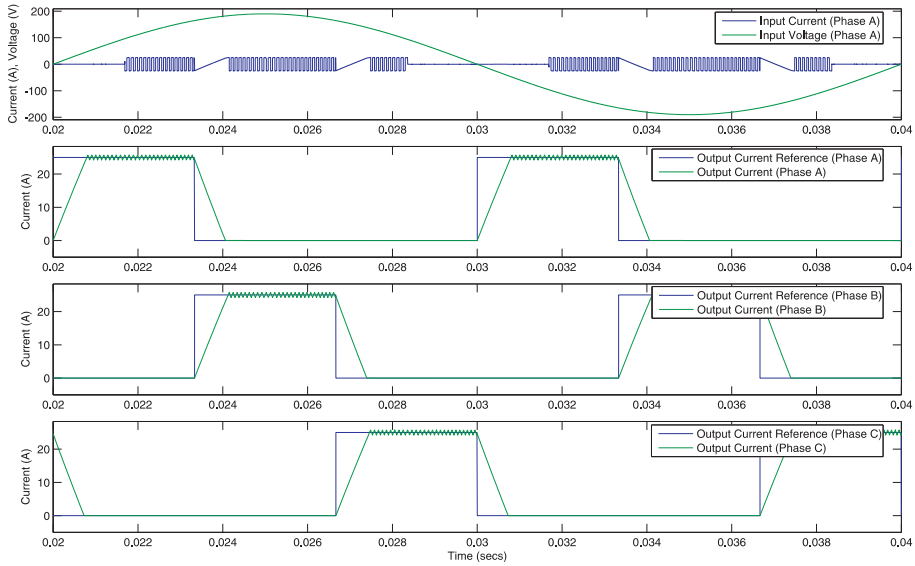

Figure 4.23: RL Load, SB Control, Pulsed Output Current (Period 3.33ms), Band 1.46A, a, Input Voltage and Current. b, Output Current and Reference (Phase A). c, Output Current and Reference (Phase B). d, Output Current and Reference (Phase C).

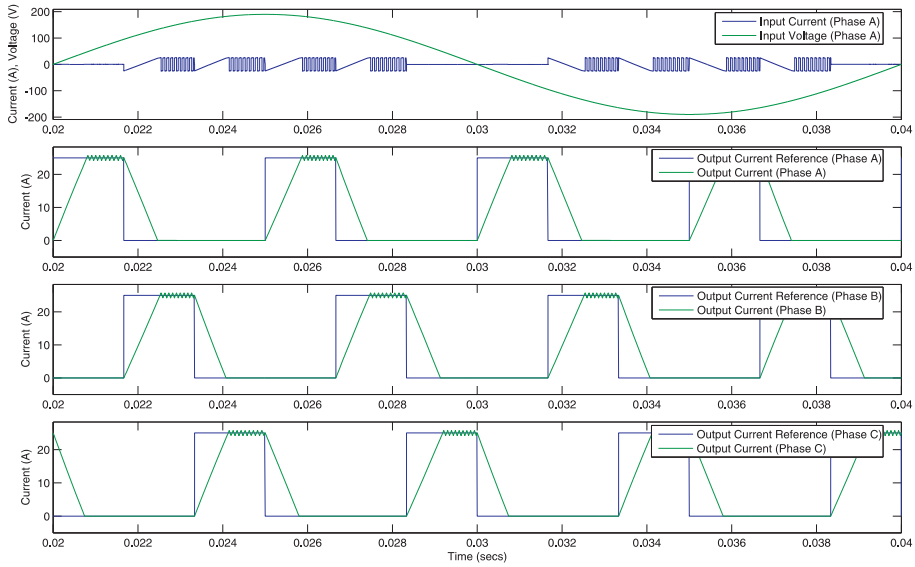

Figure 4.24: RL Load, SB Control, Pulsed Output Current (Period 1.67ms), Band 1.46A, a, Input Voltage and Current. b, Output Current and Reference (Phase A). c, Output Current and Reference (Phase B). d, Output Current and Reference (Phase C).

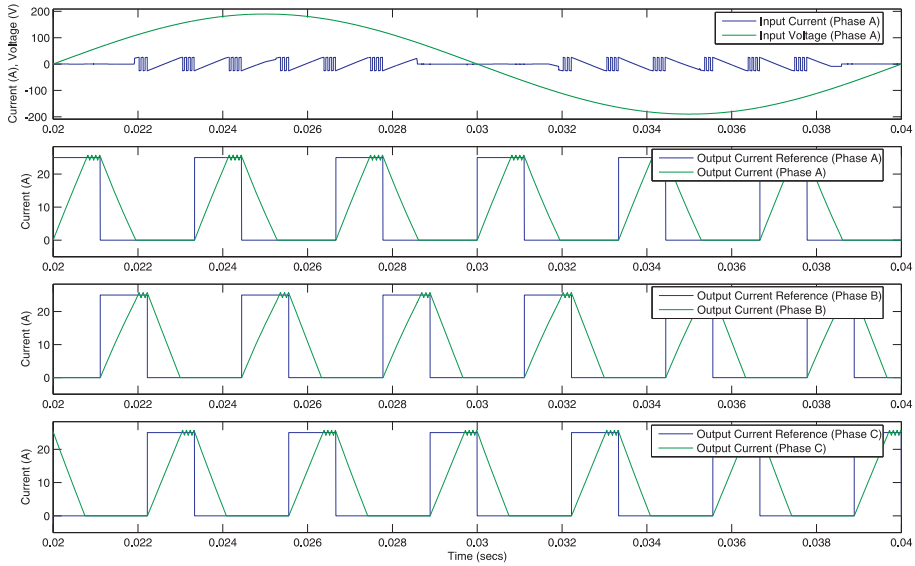

Figure 4.25: RL Load, SB Control, Pulsed Output Current (Period 1.11ms), Band 1.46A, a, Input Voltage and Current. b, Output Current and Reference (Phase A). c, Output Current and Reference (Phase B). d, Output Current and Reference (Phase C).

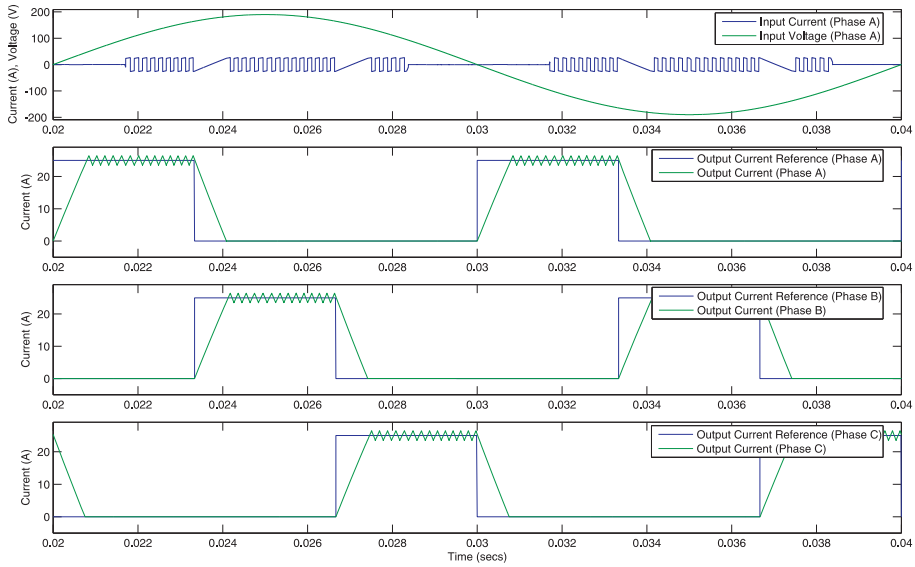

Figure 4.26: RL Load, SB Control, Pulsed Output Current (Period 3.33ms), Band 2.92A, a, Input Voltage and Current. b, Output Current and Reference (Phase A). c, Output Current and Reference (Phase B). d, Output Current and Reference (Phase C).

harmonics, as would have been expected simply from viewing figures 4.23, 4.24 and 4.25.

Considering the high frequency components shown in figures 4.28, 4.30 and 4.32, one can see that as the pulse period decreases, the high amplitudes around the 200th harmonic (around the hysteretic switching frequency) tend to decrease. This is reflecting the fact that as the pulse periods decrease, less hysteretic switching occurs, as the current spends proportionately more time increasing from and decreasing to zero. This is clear when considering figures 4.23, 4.24 and 4.25.

Comparing figures 4.27 and 4.33, which have the same pulse period, but differing current hysteresis bands widths (cases 1 and 4), one can see little variation in any of the low frequency harmonics. However, figures 4.28 and 4.34 make the decrease in switching frequency clear, as the high amplitude switching frequency harmonics have shifted down to just above the 100th harmonic.

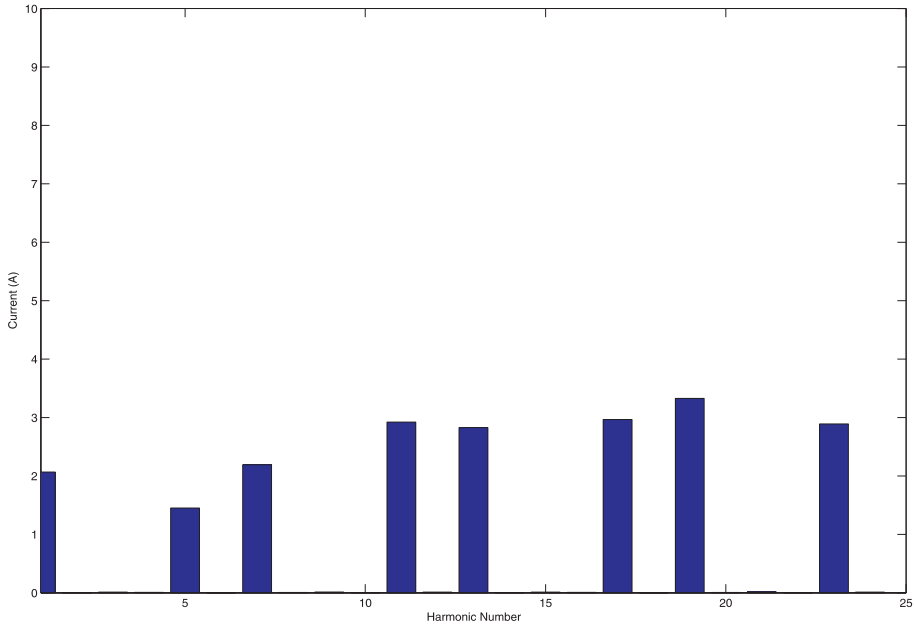

Figure 4.27: RL Load, SB Control, Pulsed Output Current (Period 3.33ms), Band 1.46A, Fourier Analysis (25 Harmonics), Fundamental Frequency 50Hz

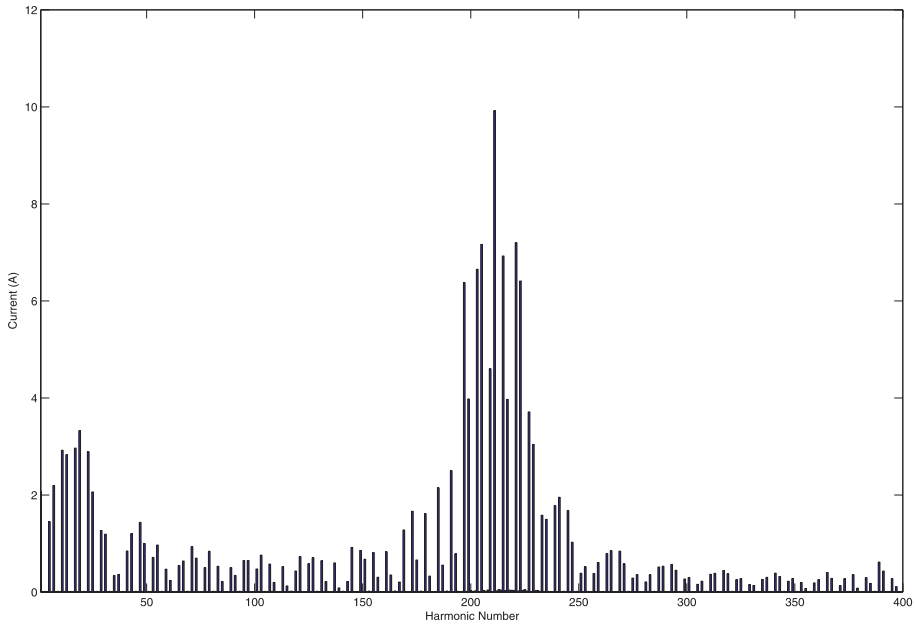

Figure 4.28: RL Load, SB Control, Pulsed Output Current (Period 3.33ms), Band 1.46A, Fourier Analysis (400 Harmonics), Fundamental Frequency 50Hz

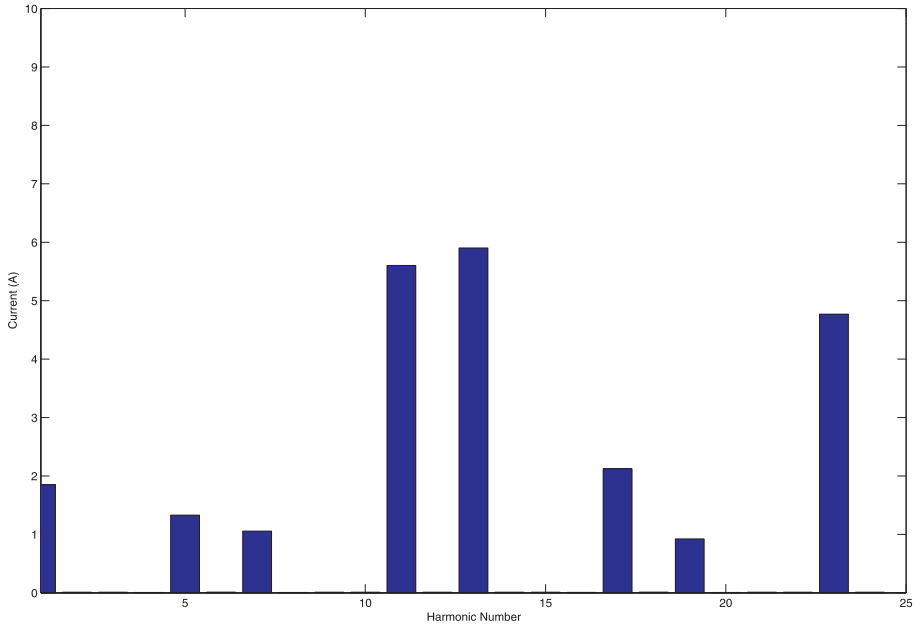

Figure 4.29: RL Load, SB Control, Pulsed Output Current (Period 1.67ms), Band 1.46A, Fourier Analysis (25 Harmonics), Fundamental Frequency 50Hz

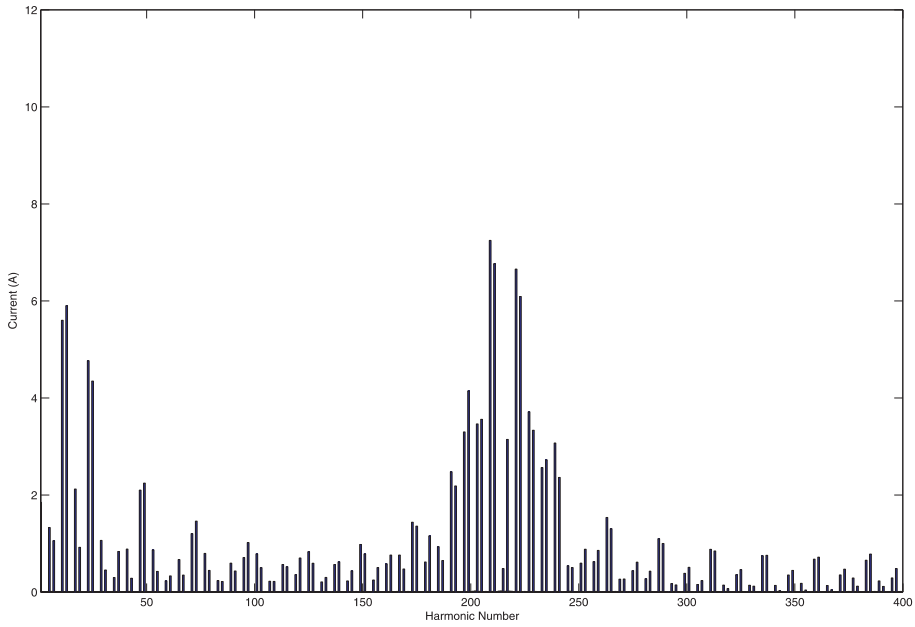

Figure 4.30: RL Load, SB Control, Pulsed Output Current (Period 1.67ms), Band 1.46A, Fourier Analysis (400 Harmonics), Fundamental Frequency 50Hz

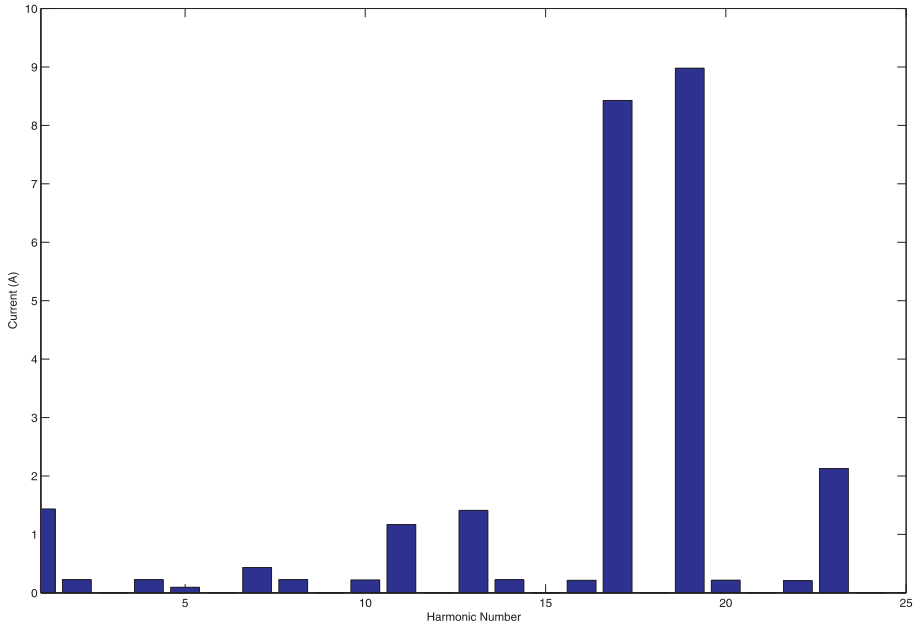

Figure 4.31: RL Load, SB Control, Pulsed Output Current (Period 1.11ms), Band 1.46A, Fourier Analysis (25 Harmonics), Fundamental Frequency 50Hz

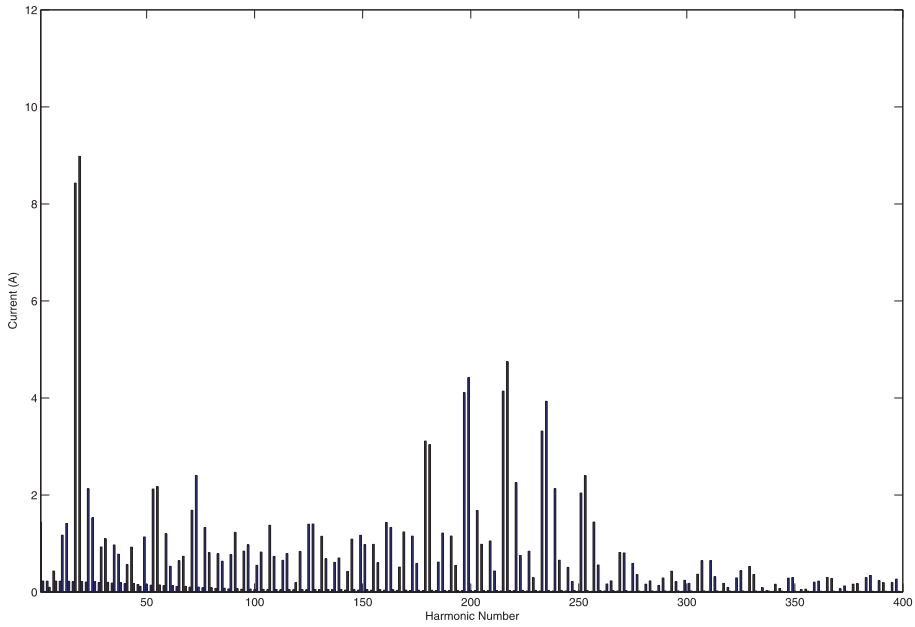

Figure 4.32: RL Load, SB Control, Pulsed Output Current (Period 1.11ms), Band 1.46A, Fourier Analysis (400 Harmonics), Fundamental Frequency 50Hz

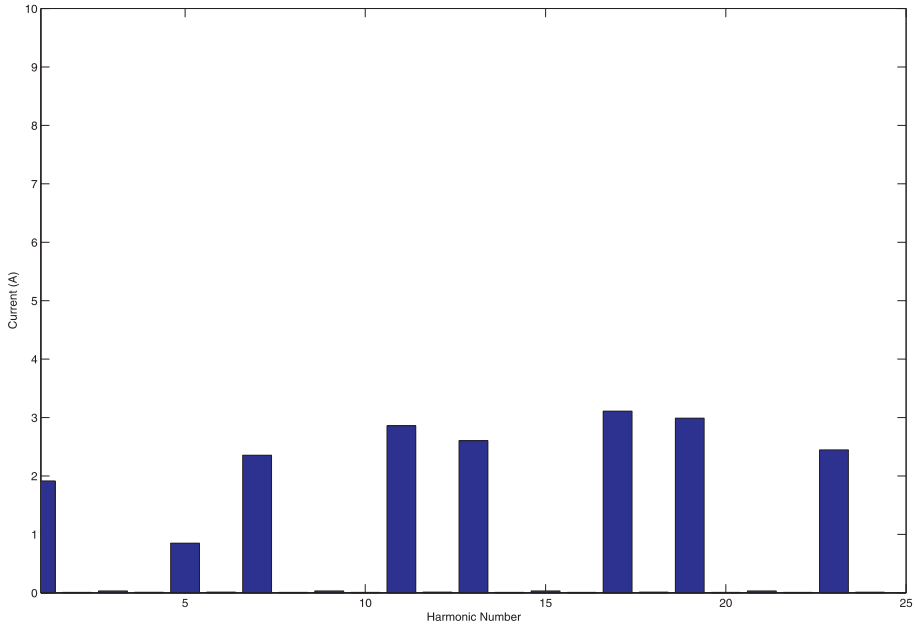

Figure 4.33: RL Load, SB Control, Pulsed Output Current (Period 3.33ms), Band 2.92A, Fourier Analysis (25 Harmonics), Fundamental Frequency 50Hz

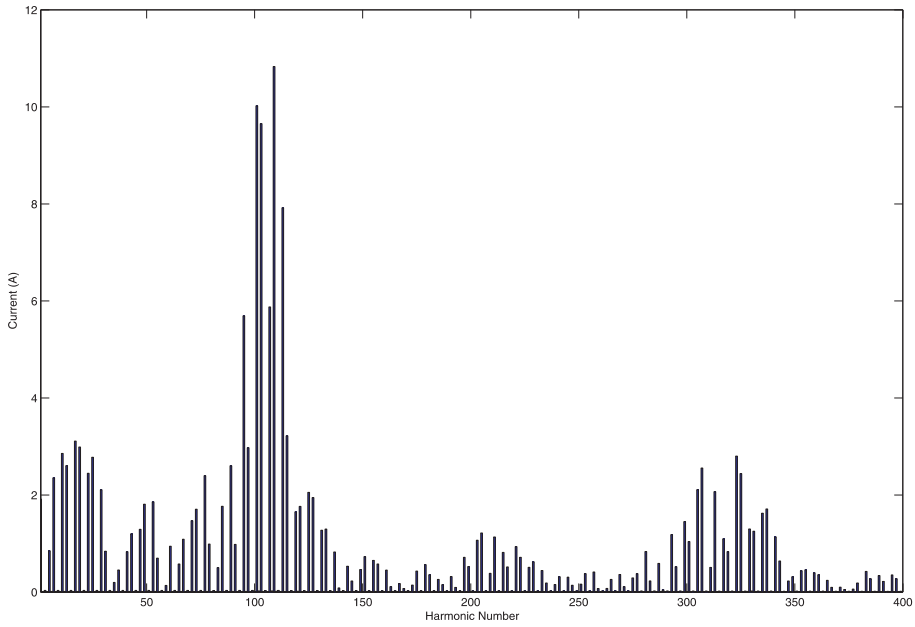

Figure 4.34: RL Load, SB Control, Pulsed Output Current (Period 3.33ms), Band 2.92A, Fourier Analysis (400 Harmonics), Fundamental Frequency 50Hz

4.5.3.2 Double Band Control

As a comparison with the single band current control results, Fourier analyses have been performed on similar cases using the double band control scheme. The conditions are as in table 4.9, while figures 4.35, 4.36, 4.37 and 4.38 show the input voltage and current and output currents for the four cases.

Case	Pulse Period (ms)	Inner Band Width (A)	Outer Band Width(A)	Approx Switching Frequency (kHz)
1	3.33	0.065	0.5	10.5
2	1.67	0.065	0.5	10.5
3	1.11	0.065	0.5	10.5
4	3.33	0.13	0.5	5.25

Table 4.9: Fourier Analysis Single Band Simulation Conditions

Fourier analyses are presented for the first 25 and the first 400 harmonics for each case. Considering figures 4.39, 4.41, and 4.43, one can again see the general decrease in amplitude of lower harmonics (5th, 7th, 11th, 13th) and increase in amplitude of the higher ones (17th, 19th) as the pulse period decreases, however this is not such a clear pattern as was seen with the single band scheme. Again however, it is clear that the fundamental component is not of a significant amplitude compared with the low harmonics near to it.

Considering the higher frequencies as shown in figures 4.40, 4.42 and 4.44, the switching frequency harmonics are greatly reduced in amplitude, reflecting the fact that the inner hysteresis band is approximately 1/20th of the size of the hysteresis band used with the single band scheme, and therefore harmonics due to switching within the band are greatly reduced. One can still however see the reduction in amplitude of the switching frequency harmonics (around the 200th harmonic) as the pulse period decreases, reflecting the fact that proportionately less hysteretic switching takes place, as was also seen with the single band case.

Comparing figures 4.39 and 4.45, one can see no change in amplitude of low frequency

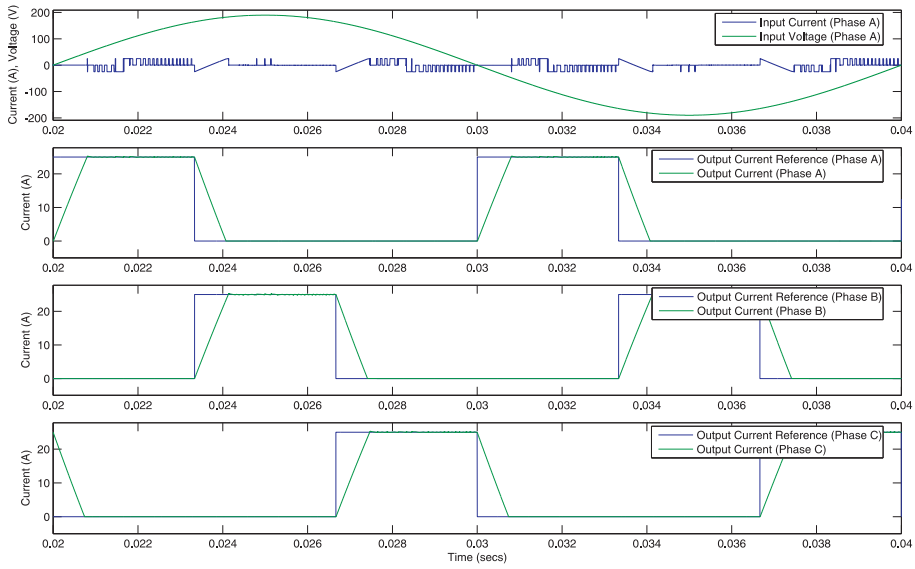

Figure 4.35: RL Load, DB Control, Pulsed Output Current (Period 3.33ms), Inner Band 0.065A, Outer Band 0.5A, a, Input Voltage and Current. b, Output Current and Reference (Phase A). c, Output Current and Reference (Phase B). d, Output Current and Reference (Phase C).

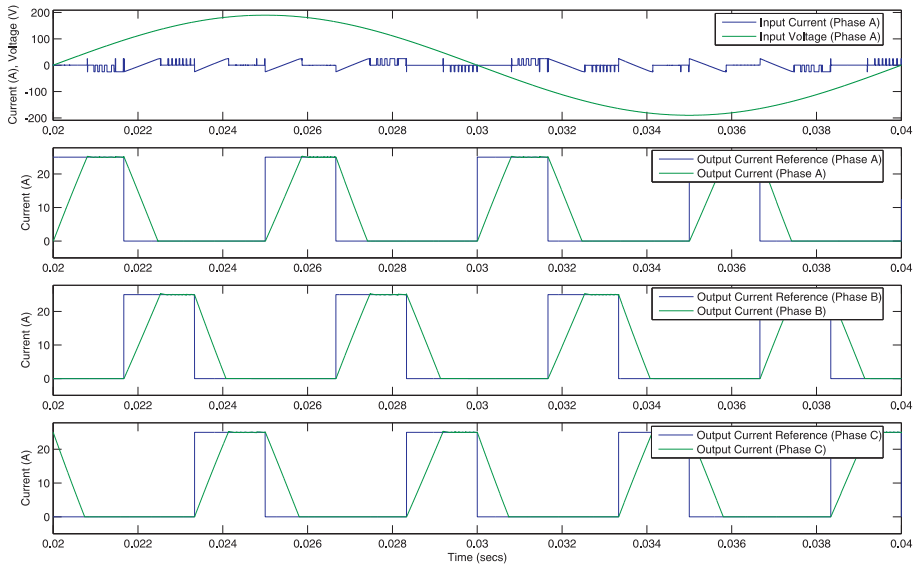

Figure 4.36: RL Load, DB Control, Pulsed Output Current (Period 1.67ms), Inner Band 0.065A, Outer Band 0.5A, a, Input Voltage and Current. b, Output Current and Reference (Phase A). c, Output Current and Reference (Phase B). d, Output Current and Reference (Phase C).

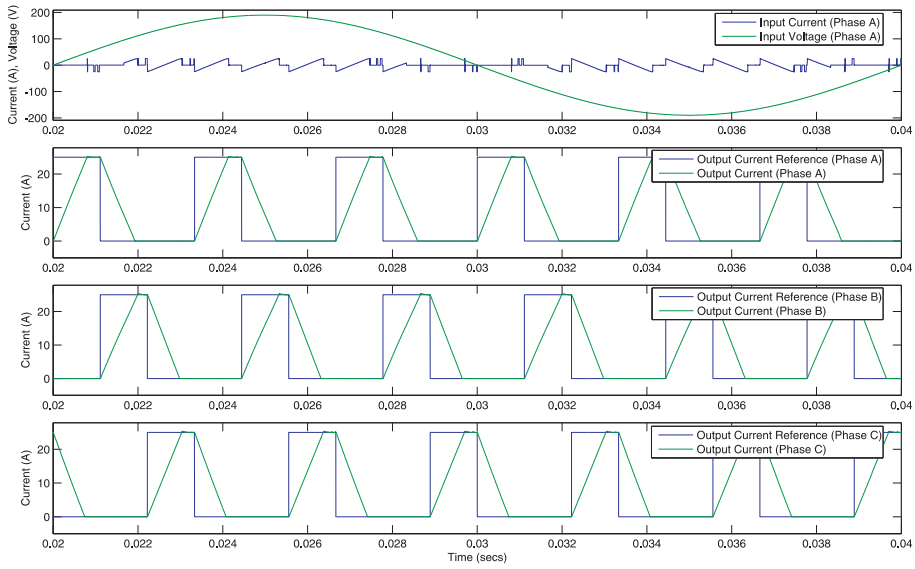

Figure 4.37: RL Load, DB Control, Pulsed Output Current (Period 1.11ms), Inner Band 0.065A, Outer Band 0.5A, a, Input Voltage and Current. b, Output Current and Reference (Phase A). c, Output Current and Reference (Phase B). d, Output Current and Reference (Phase C).

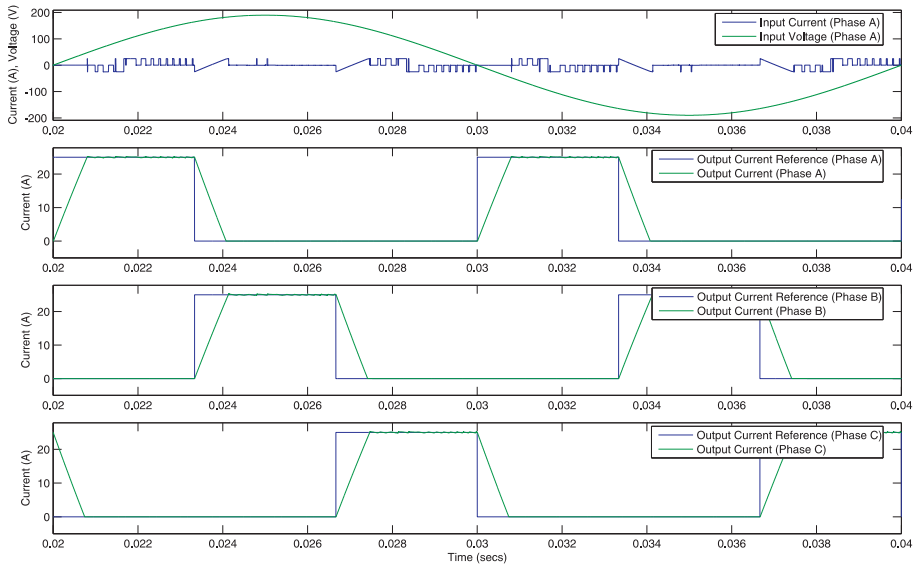

Figure 4.38: RL Load, DB Control, Pulsed Output Current (Period 3.33ms), Inner Band 0.13A, Outer Band 0.5A, a, Input Voltage and Current. b, Output Current and Reference (Phase A). c, Output Current and Reference (Phase B). d, Output Current and Reference (Phase C).

harmonics with reduced switching frequency, as would be expected. Figures 4.40 and 4.46 however show the shift in switching frequency harmonics, from around the 200th harmonic for the high switching frequency, to around the 100th harmonic for the lower switching frequency.

4.5.3.3 Summary

The main observation that can be made is that there is no clear pattern to the distribution and amplitude of harmonics generated by the SSMC when supplying pulses of current to a multiphase load. This is due to the freedom that the controller has been given in controlling the output currents of the pulsed power type load. It is however clear that the fundamental component is never particularly large compared with the other low frequency components that are produced. As the pulse periods decrease (with what would be increasing motor speed) and less hysteretic switching takes place, the lowest harmonics tend to decrease, while some of the higher ones increase. This would tend to indicate that filtering of the supply currents would be more effective for higher motor speeds than lower ones, however the large amplitude of these harmonics would indicate that a large LC input filter would be required.

Comparing the single band results with those from the double band scheme, one can say that for each of the four cases considered, the first 25 harmonics produced by the single band control scheme are always lower than those produced by the double band control scheme. The higher (switching frequency harmonics) are always higher with the single band control scheme, but these are easier to filter out with a lineside filter. This implies that although the double band scheme produces better output currents, the input currents drawn by the SSMC will need more filtering.

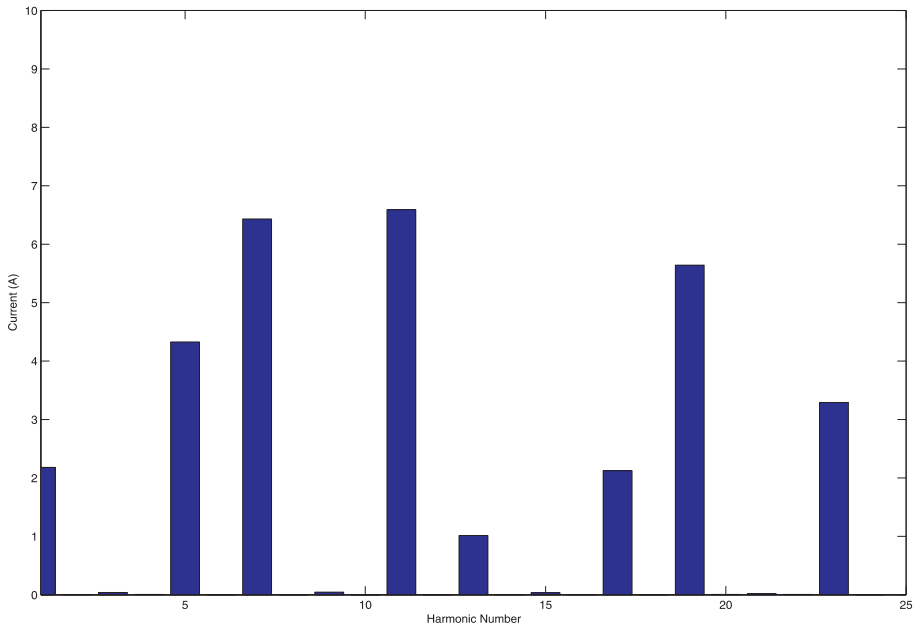

Figure 4.39: RL Load, DB Control, Pulsed Output Current (Period 3.33ms), Inner Band 0.065A, Outer Band 0.5A, Fourier Analysis (25 Harmonics), Fundamental Frequency 50Hz

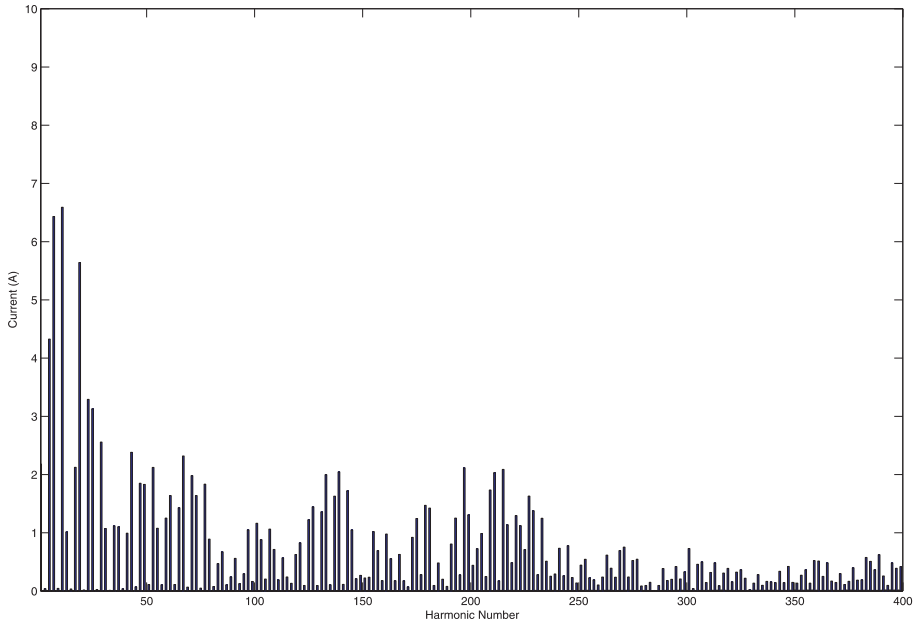

Figure 4.40: RL Load, DB Control, Pulsed Output Current (Period 3.33ms), Inner Band 0.065A, Outer Band 0.5A, Fourier Analysis (400 Harmonics), Fundamental Frequency 50Hz

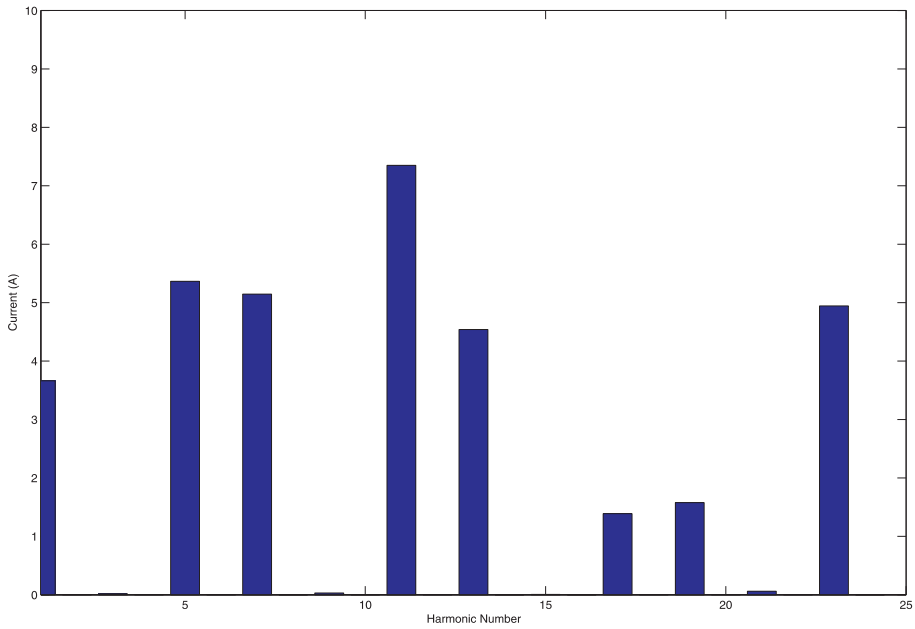

Figure 4.41: RL Load, DB Control, Pulsed Output Current (Period 1.67ms), Inner Band 0.065A, Outer Band 0.5A, Fourier Analysis (25 Harmonics), Fundamental Frequency 50Hz

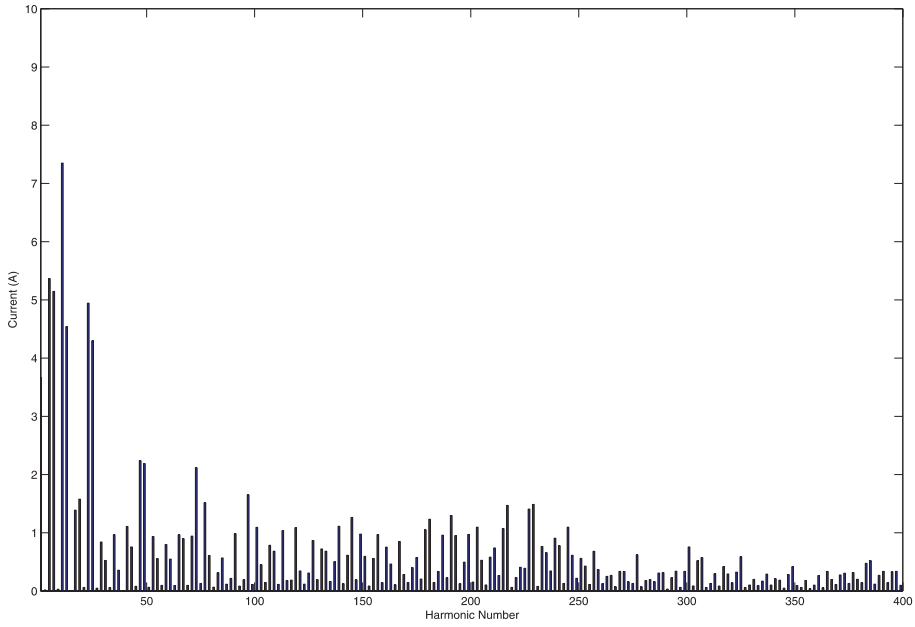

Figure 4.42: RL Load, DB Control, Pulsed Output Current (Period 1.67ms), Inner Band 0.065A, Outer Band 0.5A, Fourier Analysis (400 Harmonics), Fundamental Frequency 50Hz

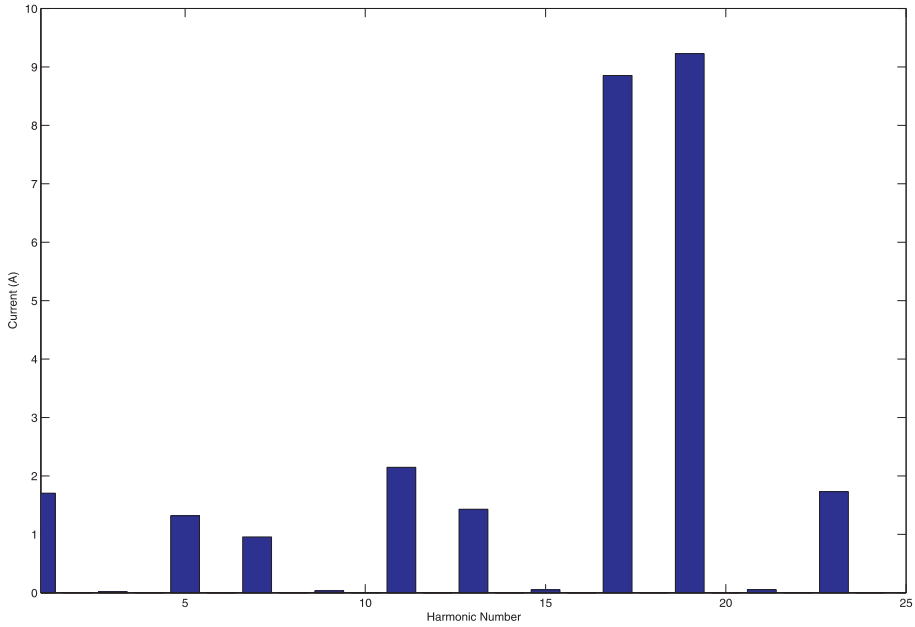

Figure 4.43: RL Load, DB Control, Pulsed Output Current (Period 1.11ms), Inner Band 0.065A, Outer Band 0.5A, Fourier Analysis (25 Harmonics), Fundamental Frequency 50Hz

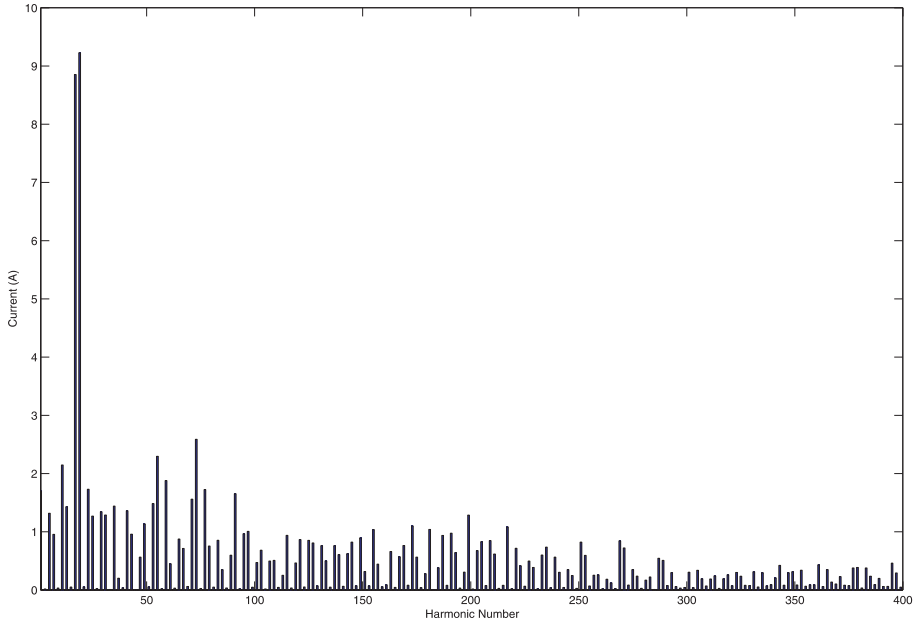

Figure 4.44: RL Load, DB Control, Pulsed Output Current (Period 1.11ms), Inner Band 0.065A, Outer Band 0.5A, Fourier Analysis (400 Harmonics), Fundamental Frequency 50Hz

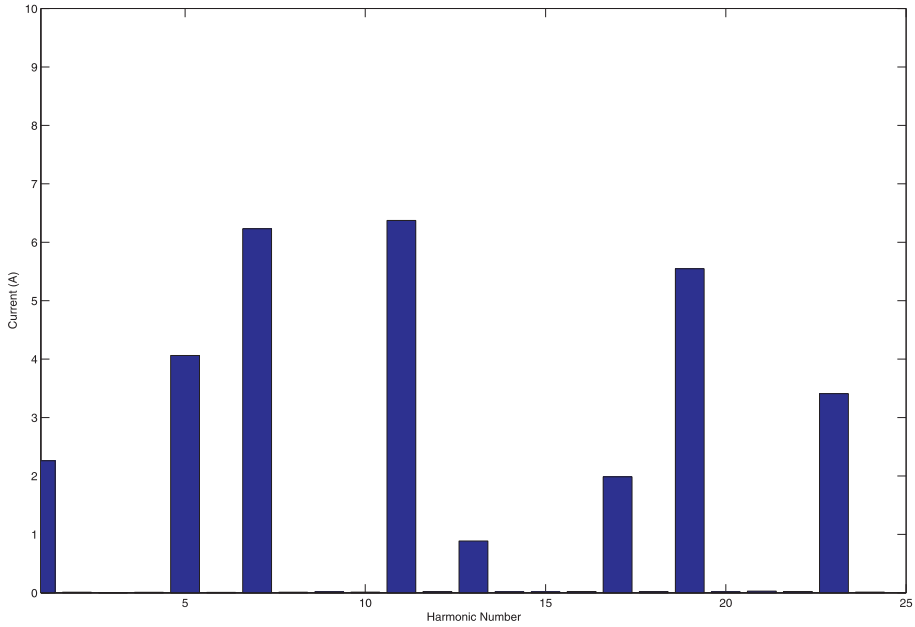

Figure 4.45: RL Load, DB Control, Pulsed Output Current (Period 3.33ms), Inner Band 0.13A, Outer Band 0.5A, Fourier Analysis (25 Harmonics), Fundamental Frequency 50Hz

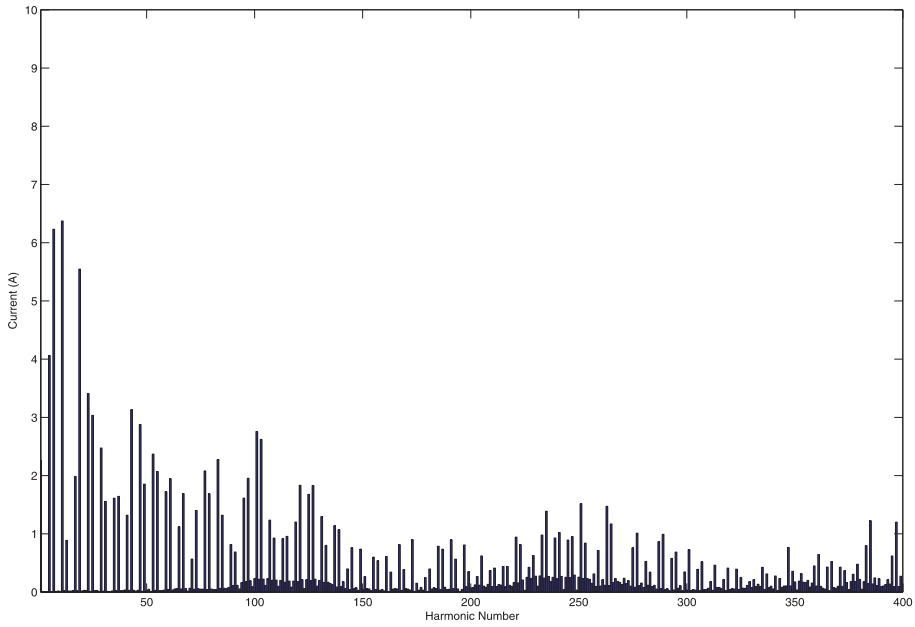

Figure 4.46: RL Load, DB Control, Pulsed Output Current (Period 3.33ms), Inner Band 0.13A, Outer Band 0.5A, Fourier Analysis (400 Harmonics), Fundamental Frequency 50Hz

4.5.4 Device Loss Estimation and Comparison

The two control schemes considered for use with the SSMC apply significantly different voltages to the load. It was therefore thought that significantly different losses would be incurred in the power devices of the converter. For this reason, simulations were performed with the SSMC supplying the same three phase RL load as given in table 4.7. Further conditions of the simulation were as given in table 4.10.

RMS Supply Voltage (V)	134
Current Amplitude (A)	25
Current Pulse Period (s)	0.01
SB Band Width (A)	0.73
DB Inner Band Width (A)	0.73
DB Outer Band Width (A)	1.5

Table 4.10: Loss Estimation Simulation Conditions

As a fair comparison between control strategies, the double band controller hysteresis bands have been widened, to produce the same output current ripple as given by the single band control scheme. The simulation performed produced the loss figures given in table 4.11.

	Single Band	Double Band
Conduction Loss (W)	23.12	23.49
Switching Loss (W)	13.81	1.60

Table 4.11: Switching and Conduction Loss Figures for Single Band and Double Band Control Schemes.

The main reduction in switching loss seen with the double band control scheme is due to the much lower frequency of switching, due to the much smaller change in voltage applied to the load at each switching instant.

4.6 Switched Reluctance Motor Load

Presented in this section are simulation results using the SSMC model with the linear Switched Reluctance motor model described in section 4.1. Simulation results for the two motor speeds at which the model was validated are presented, with the SSMC operating using both single and double band control schemes. The supply voltage used has been reduced such that the voltage applied across the motor phases is approximately equal to that used with the drive from which the model was validated.

4.6.1 Speed - 530 rpm

The first motor speed at which the model was validated is 530 rpm. This used the switching angles and current limit given in table 4.2. Figure 4.47 presents the phase current demand value, along with the actual current for each of the three motor phases, controlled using the single band control scheme, and shows the way in which the phase currents are applied.

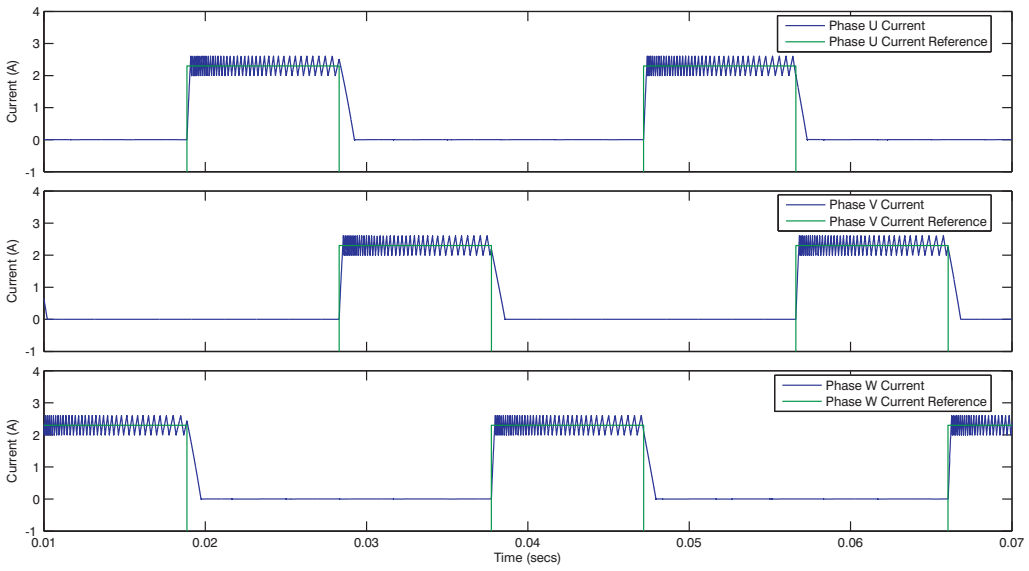

Figure 4.47: Linear SRM Model (530 rpm), SB Control, Three Phase Output Currents.

Presented in figure 4.48a are the phase current and demand signal for phase U of the

converter output, along with the error signal and hysteresis band in figure 4.48b, and the applied output voltage in figure 4.48c. One can see that the current is controlled as was described in section 4.5.1. A point to note however is that during the periods of zero current, the current error does not reach zero. This is due to the fact that when a zero current is required, the actual demand current is set to a negative value in order to ensure that erroneous switching does not occur. The nature of the SSMC topology means that the negative current is not supplied. This holds the current firmly at zero, but has the effect that the current error is non-zero.

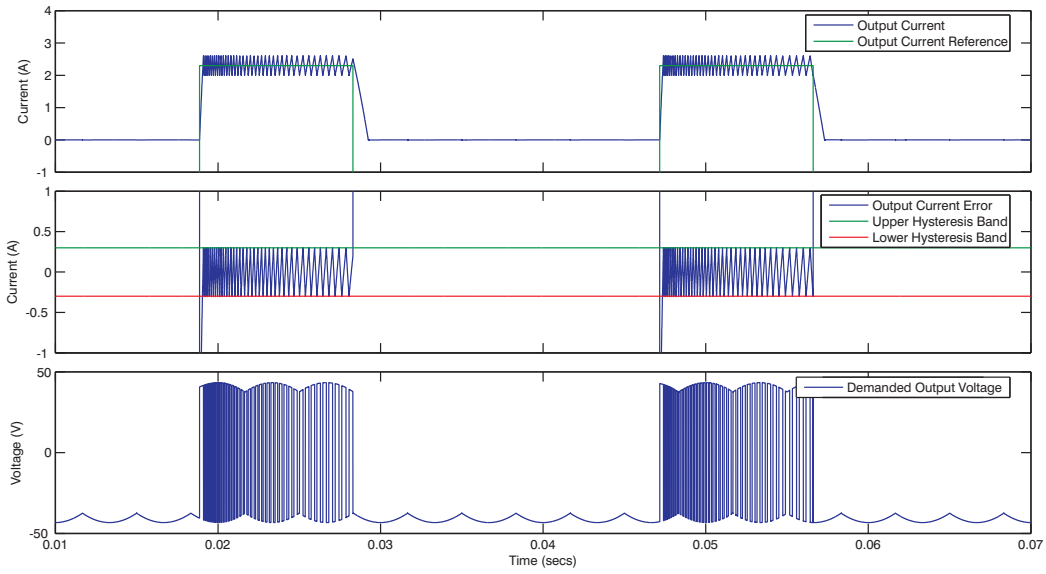

Figure 4.48: Linear SRM Model (530 rpm), SB Control, Phase U a, Output Current with Reference. b, Output Current Error with Hysteresis Band. c, Demanded Output Voltage.

Presented in figure 4.49 are the three phase converter output currents controlled using the double band control scheme. One can again see the way in which the double band control scheme is able to control the output current within a much tighter hysteresis band, whilst maintaining a similar average switching frequency as that of the double band method.

Figure 4.50a presents the output and demand current for phase U, along with the current error signal and hysteresis bands in figure 4.50b. The applied output voltage can be seen in figure 4.50c. One can again see the way in which the double band control scheme controls the current to be within the inner hysteresis band, as was described in section 4.5.1.

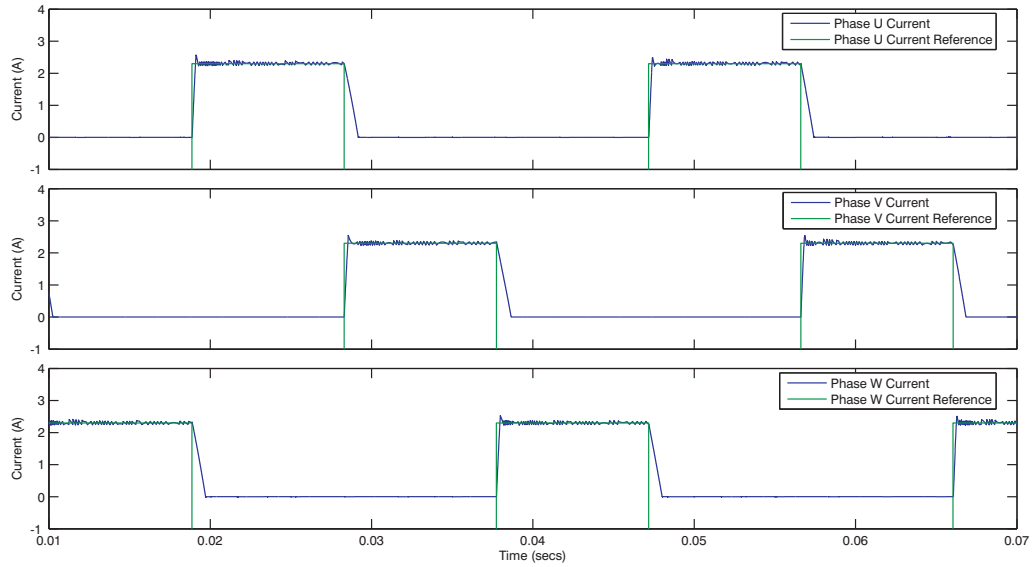

Figure 4.49: Linear SRM Model (530 rpm), DB Control, Three Phase Output Currents.

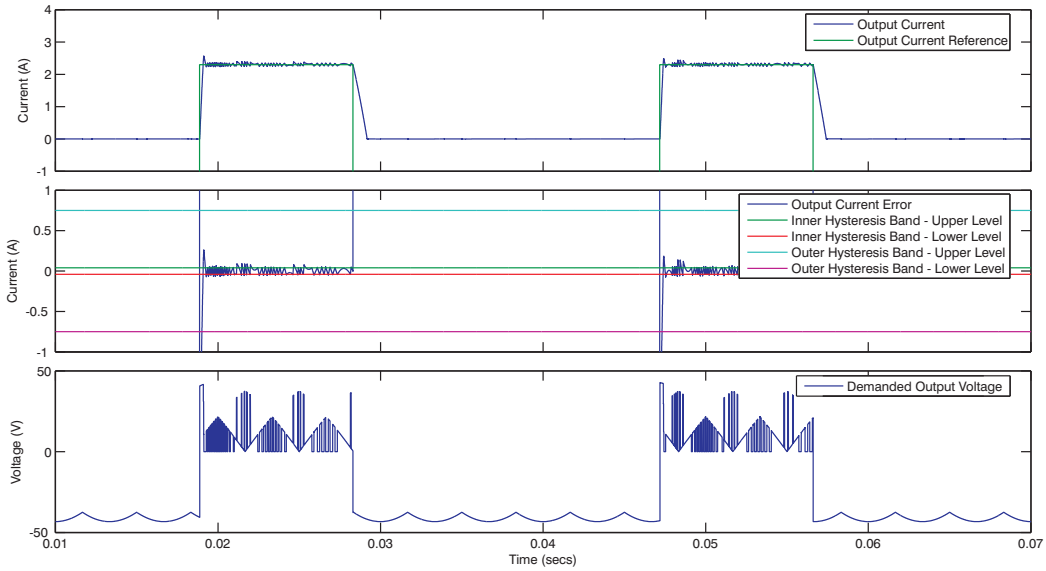

Figure 4.50: Linear SRM Model (530 rpm), DB Control, Phase U a, Output Current with Reference. b, Output Current Error with Hysteresis Bands. c, Demanded Output Voltage.

Figure 4.51 compares a single output current pulse for one phase, using the single band control scheme (4.51a) and the double band control scheme (4.51b). The first point to note is again the way in which the double band control scheme contains the current within a tighter band than the single band scheme, whilst maintaining approximately the same average switching frequency. The influence of the changing motor phase inductance is also visible here, which increases linearly over the period of the current pulse (which spans the full 30 mechanical degrees over which the motor poles rotate from just beginning to overlap, to being fully aligned. The linear increase in inductance corresponds with a linear decrease in switching frequency in the single band controlled current. A similar decrease in switching frequency can be seen for the double band case, however the use of different voltage levels makes this less clear.

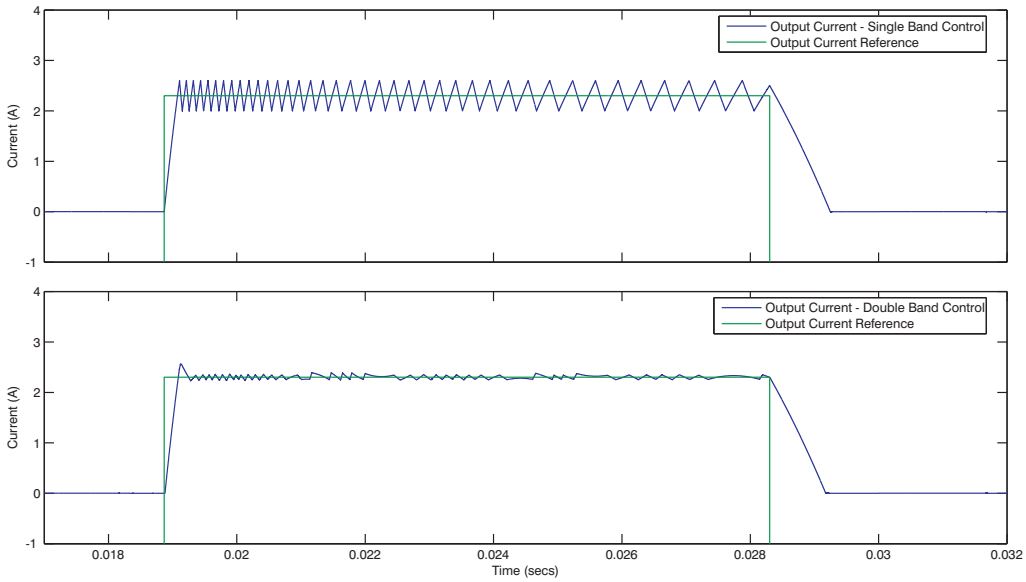

Figure 4.51: Linear SRM Model (530 rpm) Output Current with Reference a, SB Control. b, DB Control.

Presented in figure 4.52 are the input voltage and current waveforms for one input phase. Figure 4.52a is of the single band control, and it is again clear that all current drawn from the respective phase occurs whilst its voltage amplitude is greater than that of the other two phases. Figure 4.52b gives the input current using the double band scheme, and one can see the more random distribution of current drawn. Most current is however drawn from

each phase whilst the voltage amplitude is lower, as the lower voltage levels are generally used at the converter output.

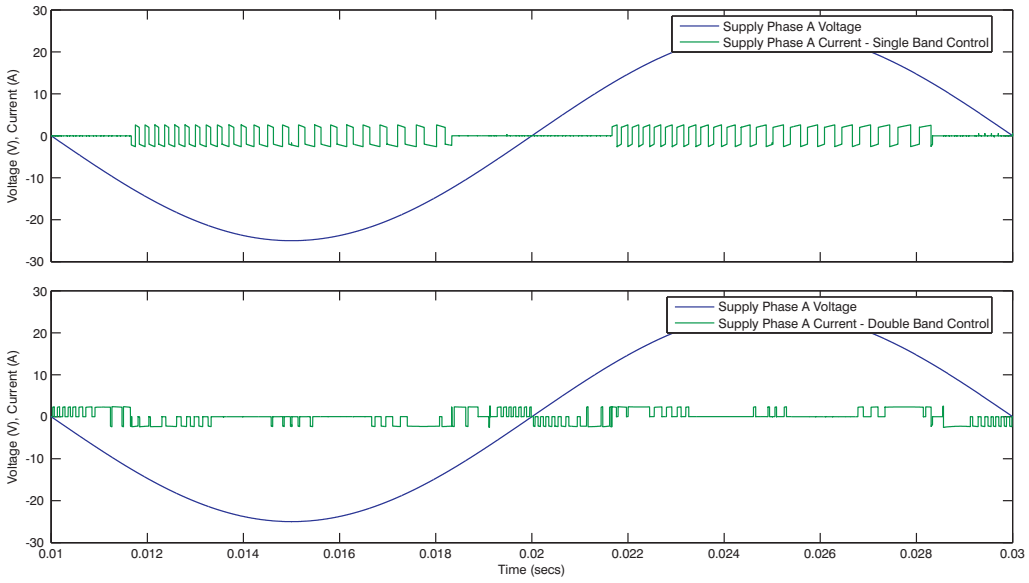

Figure 4.52: Linear SRM Model (530 rpm), Input Voltage and Current a, SB Control. b, DB Control.

4.6.2 Speed - 3080 rpm

The second motor speed at which the model was validated is 3080 rpm, using the switching angles and current limit given in table 4.2. Figure 4.53 presents the phase current demand value, along with the actual current for each of the three motor phases, controlled using the double band control scheme, and shows the way in which the phase currents are applied.

The effect of the motor back EMF is now visible, as the rotational speed has increased. As the phase current is now turned on before the rotor and stator poles begin to overlap, the phase inductance is constant. This implies that the rate of change of inductance with rotor position is zero, and the back EMF will be zero, as given in equation 4.4. Half way through the current pulse, as the rotor reaches 30 degrees from alignment with the stator pulse, the rotor and stator poles begin to overlap, and the inductance begins to increase

at a fixed rate. The dL/dθ component of equation 4.4 is now positive, and a back EMF is seen, which opposes the voltage applied by the converter. This in turn implies that an insufficient voltage is seen across the phase winding to maintain the current at the demand value, and creates the dip in current seen over the second half of each current pulse. At higher rotational speeds the back EMF becomes much greater, and the current will rarely meet the demand value. Speed control is then maintained using the switching angles.

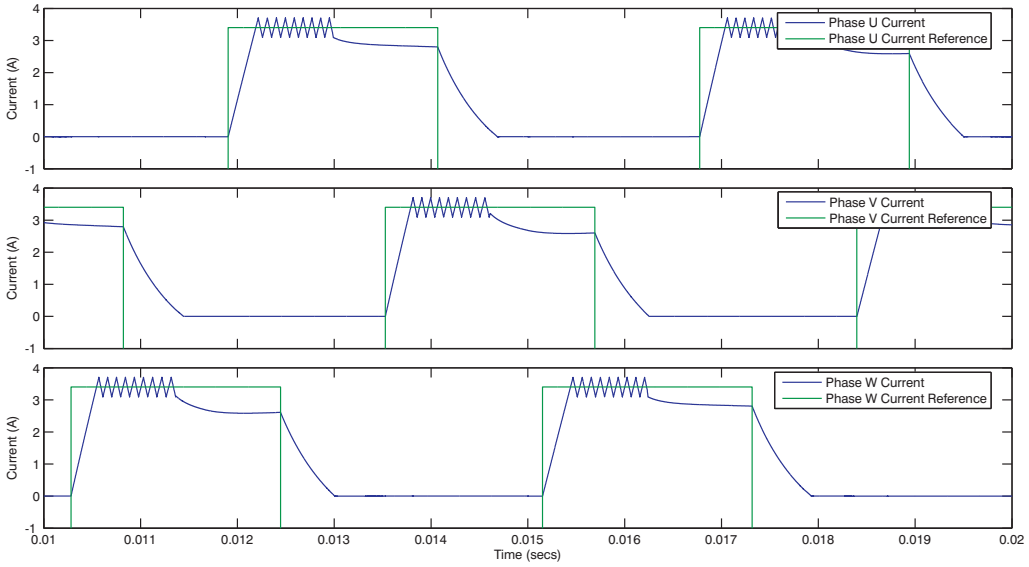

Figure 4.53: Linear SRM Model (3080 rpm), SB Control, Three Phase Output Currents.

Presented in figure 4.54a is the current demand and actual current for output phase U, using the single band method. Figure 4.54b shows the error signal, and one can see how the effect of the phase back EMF pushes the current below the lower level of the hysteresis band. When this occurs, the most positive supply voltage is constantly applied, as seen in figure 4.54c, however it is not of a large enough amplitude to pull the output current up to the demand value.

Figure 4.55 presents the three output phase currents when controlled using the double band control scheme. The effect of the phase back EMF is identical as that observed with the single band scheme. Control of the current within the small inner hysteresis band is again clear.

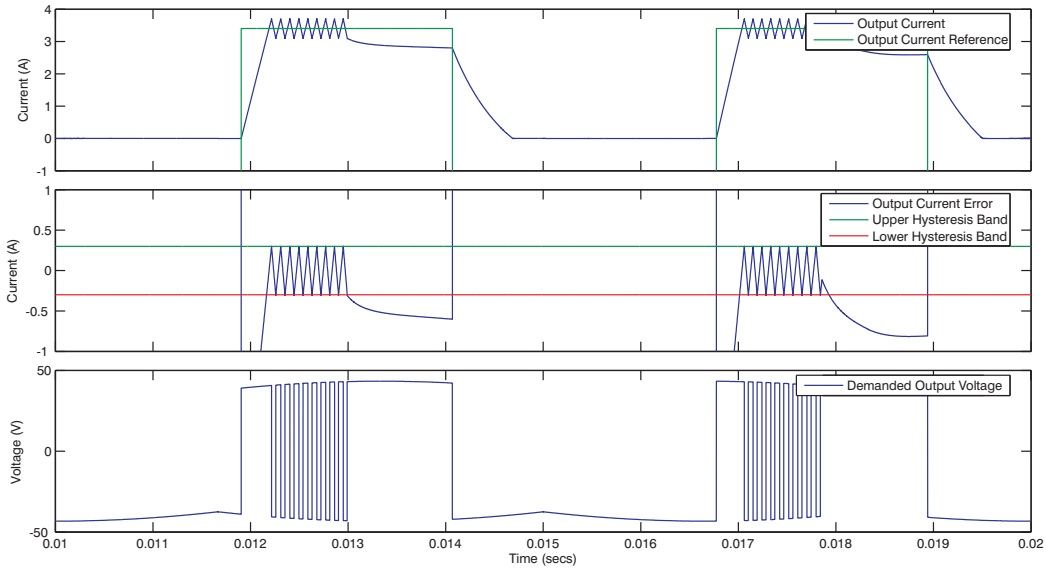

Figure 4.54: Linear SRM Model (3080 rpm), SB Control, Phase U a, Output Current with Reference. b, Output Current Error with Hysteresis Band. c, Demanded Output Voltage.

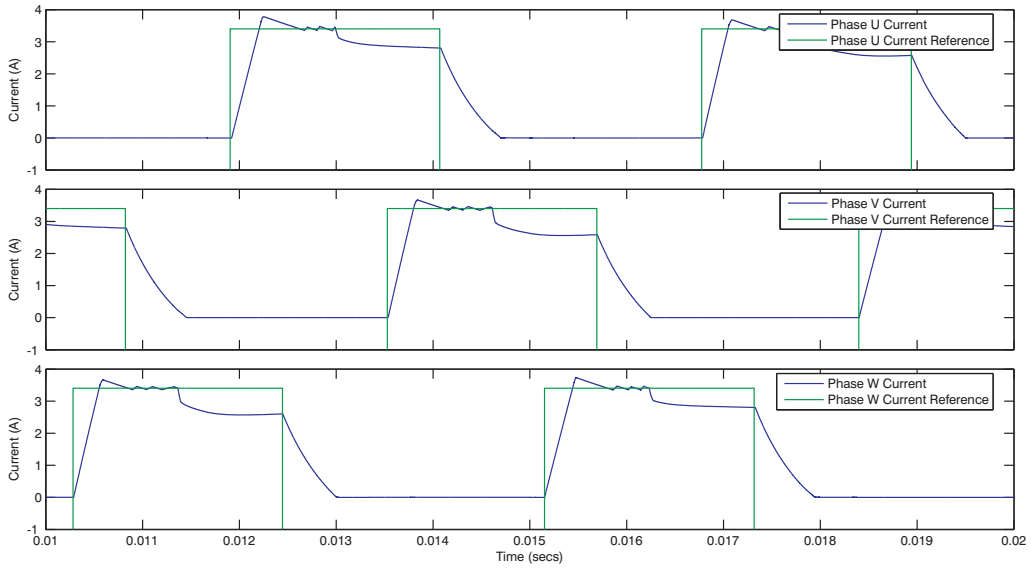

Figure 4.55: Linear SRM Model (3080 rpm), DB Control, Three Phase Output Currents.

Viewing the double band current error signal, as given in figure 4.56b, and the applied output voltage given in figure 4.56c, one can see that only a small number of switching transitions occur before the effect of the back EMF pulls the current signal outside of the inner hysteresis band, and the applied output voltage is quickly stepped up to level 3. One can see how this will remove a large proportion of the high frequency switching components from the input current.

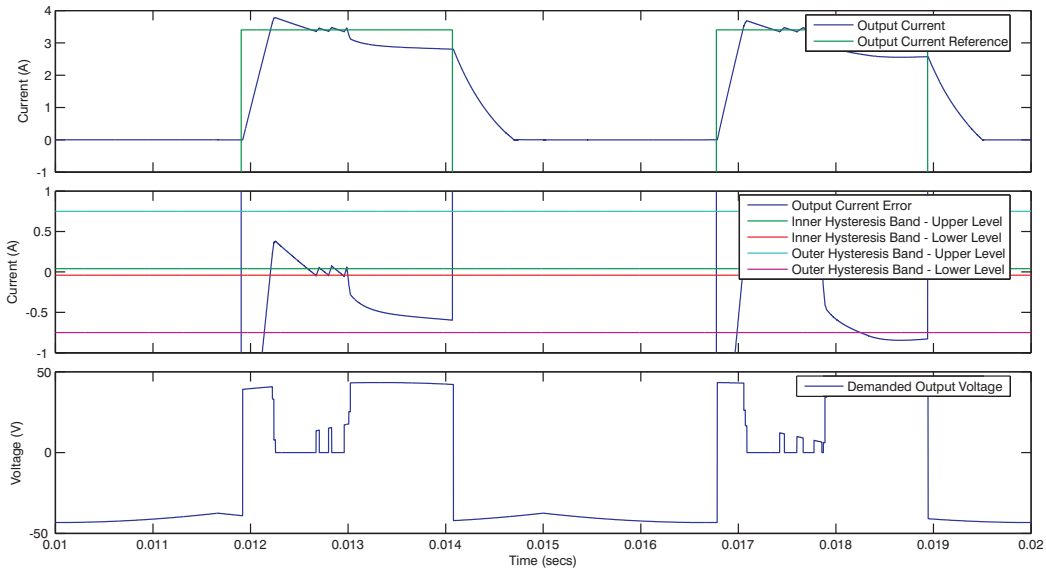

Figure 4.56: Linear SRM Model (3080 rpm), DB Control, Phase U a, Output Current with Reference. b, Output Current Error with Hysteresis Bands. c, Demanded Output Voltage.

Presented in figure 4.57 is a comparison of the output current when controlled using both the single and double band control schemes. It is clear that the effect of the back EMF will have a large effect on the number of high frequency switching occurances in the input current of the converter. One should also note the constant switching frequency visible here. This is due to the fact that during the first half of the current pulse, the phase inductance is at its minimum value, and is constant. Once the rotor reaches the point where the inductance starts to increase, half way through the current pulse, the back EMF opposes the supply voltage and the current drops outside the hysteresis band, causing the most positive voltage to be applied constantly. There is therefore no hysteretic switching once the inductance starts to increase, and no increase in switching frequency. Also worth noting is the constant

rate of increase of current at the start of the pulse, compared with the decreasing rate of decrease of current at the end of the pulse. This is due to the constant low inductance during the first half of the pulse, compared with the linearly increasing inductance during the second half of the pulse, as can be seen in figure 4.7.

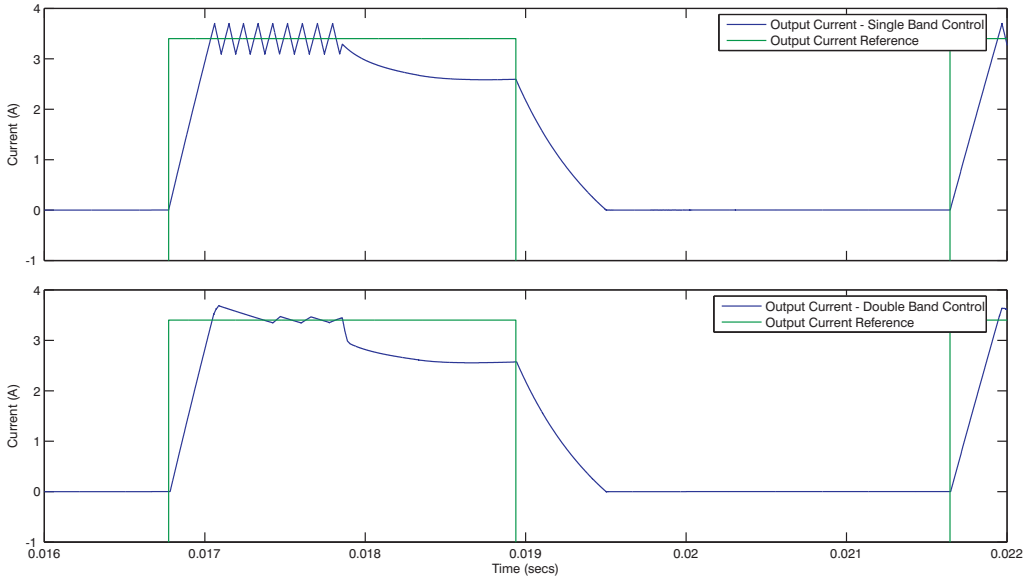

Figure 4.57: Linear SRM Model (3080 rpm) Output Current with Reference. a, SB Control. b, DB Control.

Figure 4.58 presents the input voltage and current of a single input phase, with output current controlled using both the single and double band methods. One can again see that with the single band scheme, all current is drawn from the input phase whilst its voltage amplitude is greater than that of the others. However, with the double band method, as well as short current pulses being drawn from the phase whilst its voltage amplitude is low as with the low speed condition shown in figure 4.52, large blocks of current are drawn from the phase when its amplitude is greater than that of the other two phases. This is due to the effect of the back EMF, and the fact that for half of each output current pulse, the most positive voltage is constantly applied.

One can also see the effect of the overlapping output phase pulses. This is visible in figure 4.53 and figure 4.55, as the hysteretic switching component of the first half of one phase

pulse is superimposed on the smooth current of the second half of the previous phase pulse. This is visible with both control schemes.

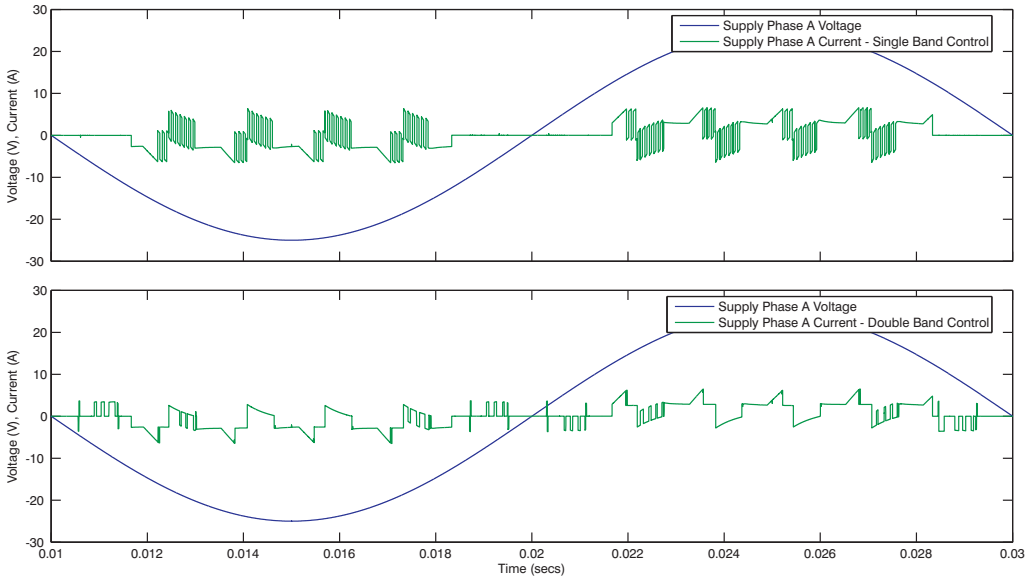

Figure 4.58: Linear SRM Model (3080 rpm), Input Voltage and Current a, SB Control. b, DB Control.

4.7 PMDC (SATOW) Motor Load

A small number of simulation results are presented from the SATOW project, which uses a five phase version of the SSMC to drive a custom designed and built trapezoidal PMDC motor, using a supply voltage of 115V rms, variable in frequency from 400 Hz to 800 Hz. The intention here is simply to show that the SSMC can be used to drive such a motor, and results are presented for the lower speed of 2000 rpm, and the higher speed of 12,000 rpm, at which this motor is designed to operate. Only results for control using the double band control scheme are presented, as this motor has been designed to have a low inductance of 0.55 mH, as specified in table 3.1. Control using the single band control scheme would require switching frequencies far higher than those appropriate with the currently available IGBTs in order to provide a relatively smooth, constant current output

throughout the demand pulse.

The five phase output currents for the low speed of 2000 rpm are presented in figure 4.59. One can see the way in which the current pulses overlap as is described in section 3.2.2, ensuring a positive torque output throughout a complete revolution of the motor, even if a fault has occurred on one phase. The low speed simulation has been performed for a supply frequency of 800 Hz.

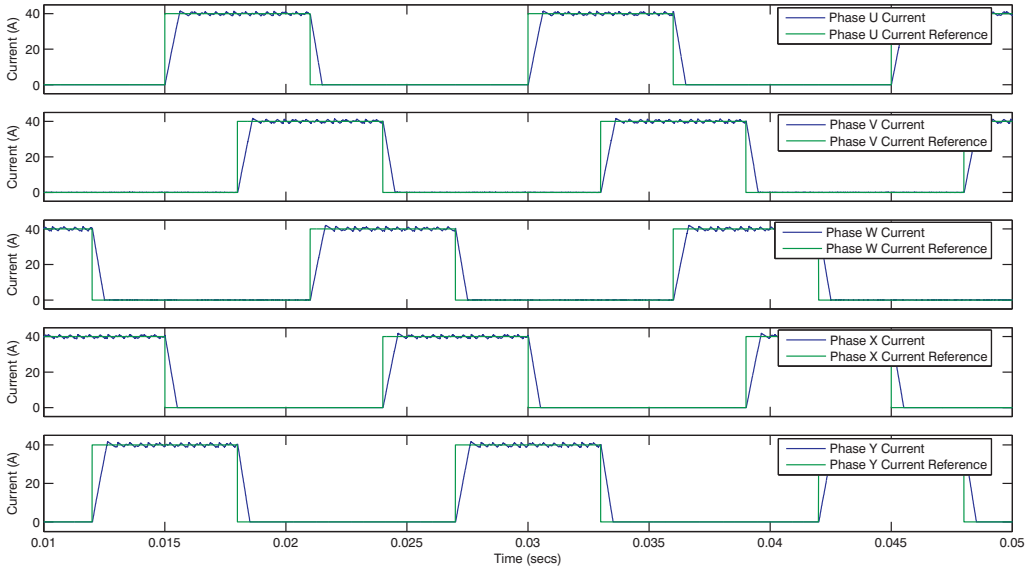

Figure 4.59: SATOW PMDC Motor (2000 rpm), DB Control, Three Phase Output Currents.

Presented in figure 4.60 is the output current, along with the error signal and hysteresis bands, applied output voltage, and output voltage level used. One can see that a relatively wide band of approximately 2 amps is used here. Based on a comparison of the hysteresis bands used in figures 4.18 and 4.19, for the single and double band schemes respectively, it is likely that using the single band scheme would require a band 7 times larger than the inner band used with the double band technique in order to achieve a similar switching frequency. In this case this would imply a band width of approximately 14 amps, which is not appropriate for a system in which the maximum demand current is 40A.

Figure 4.61 presents the 5 phase output currents for the high speed of 12,000 rpm. These

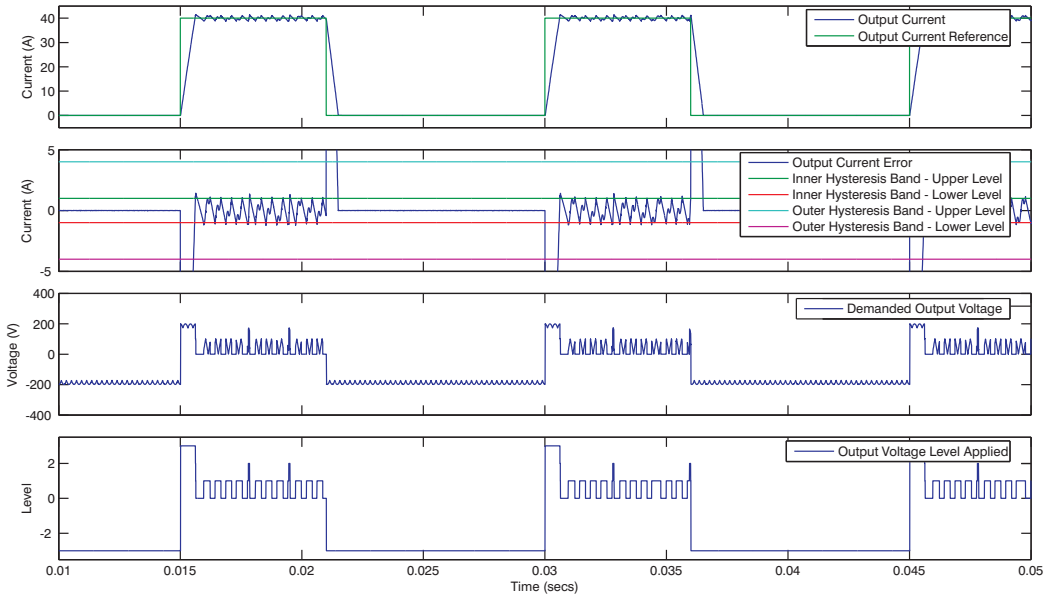

Figure 4.60: SATOW PMDC Motor (2000 rpm), DB Control, Phase U a, Output Current with Reference. b, Output Current Error with Hysteresis Bands. c, Demanded Output Voltage. d, Applied Output Voltage Level.

simulations were performed with an input frequency of 400 Hz. At this speed the phase back EMF is much greater, and the effect of this can be seen by considering figure 4.62. Once the current reaches the demand value, and the hysteresis control becomes active, one can see that the applied output voltage switches between only the highest levels, levels 2 and 3, in order to combat the high back EMF.

Interestingly, one can also see the effect of the trapezoidal nature of the back EMF generated in this motor. The current demand first steps up whilst the back EMF is oriented to increase the current. This is such that a sufficiently large current is flowing at the point where the back EMF changes sign, and positive torque can be produced. This point is clear on the current waveform at approximately t=5.1e-3, as the rate of increase of current drops significantly, whilst level 3 voltage is still applied, due to the back EMF now opposing the applied voltage. The voltage level is not stepped down until approximately t=5.5e-3, as the hysteretic control activates. The current demand is then set to zero at approximately t=6e-3, and the current drops rapidly, as both the back EMF and the applied voltage cause

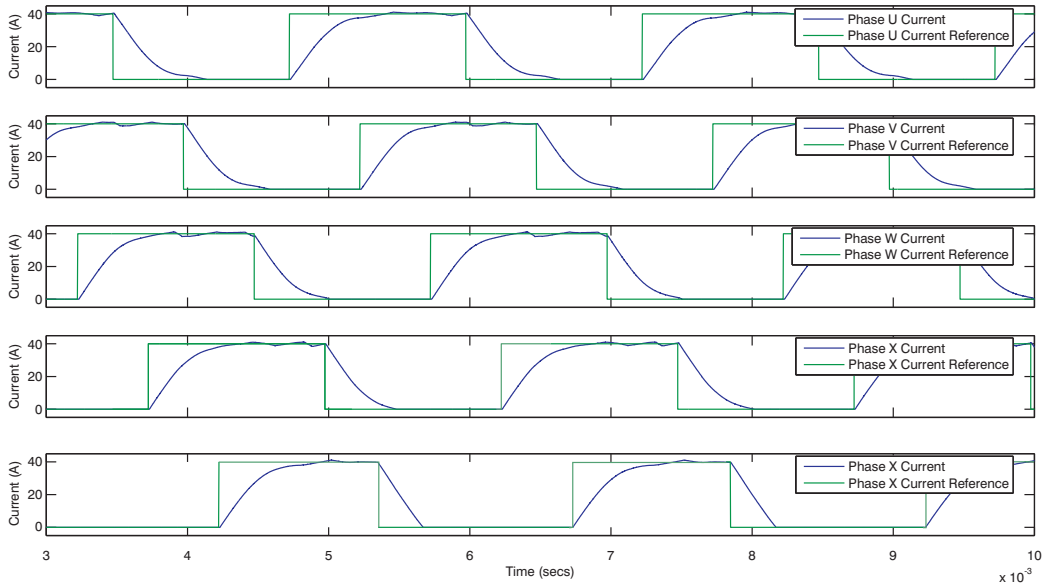

Figure 4.61: SATOW PMDC Motor (12,000 rpm), DB Control, Three Phase Output Currents.

it to fall. However, at approximately t=6.25e-3, a significant change in the rate of decrease of current can be seen. This is the point at which the back EMF again changes sign, and again opposes the applied voltage.

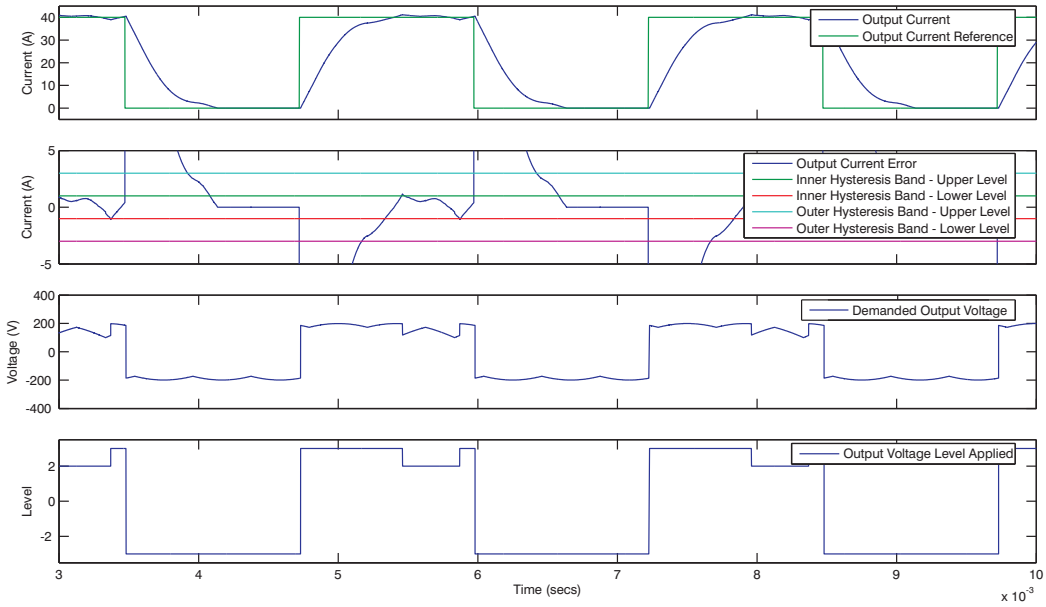

Figure 4.62: SATOW PMDC Motor (12,000 rpm), DB Control, Phase U a, Output Current with Reference. b, Output Current Error with Hysteresis Bands. c, Demanded Output Voltage. d, Applied Output Voltage Level.

4.8 Summary

This chapter has presented the Simulink simulations performed for the operation of the SSMC with both a switched reluctance motor and a trapezoidal PMDC machine, using implementations of both the single and double band control schemes. Firstly a simple, magnetically linear model of the switched reluctance motor was developed, based on the linear machine equation. Although this model assumes that no saturation of the steel within the motor occurs, it was shown to be a reliable tool when simulating the electrical motor behaviour under two specific conditions.

The single and double band control schemes were then implemented within Simulink, and truth tables developed which would later be used when implementing the control schemes in the practical converter. A series of simulations were performed, first testing the operation of both the single and double band schemes with a combination inductive and resistive load. This verified the operation of the two control scheme and it was noted that due to the

availability of lower voltages in the double band scheme, tighter hysteresis bands could be used. Also, the input current was distributed over a greater proportion of the input voltage sine wave.

Simulations were then performed using the switched reluctance motor model at the two speeds for which it was verified. The main points noted from these results were the greater range of switching frequencies produced as the motor inductance varies, and the way in which the back EMF of the motor inherently restricts the current at higher speeds, reducing the number controller actions and restricting the distribution of current between input phases.

Fourier analyses were performed on the input currents drawn, for both control schemes at the two speeds. The most significant point illustrated here was the reduced harmonic content produced by the double band control scheme at both speeds, due to the tighter hysteresis band that could be used.

A small selection of results were then presented for simulation of the single sided matrix converter driving the trapezoidal PMDC motor, which had been designed as part of the SATOW project. It was shown that the double band control scheme makes use of the SSMC with low phase inductance motors such as this possible, due to the lower voltages that can be applied to the motor phases in order to control the current.

Chapter 5

Prototype Drive - Construction and Control Implementation

5.1 Converter Hardware

The Prototype Single Sided Matrix Converter was designed in a modular form, allowing for easy expansion of phase numbers. A block diagram showing the structure of the 3-phase SSMC and controller can be seen in figure 5.1, while figure 5.2 shows a photo of the complete 5-phase SSMC. More Photos can be seen in appendix E.

The control of the SSMC is performed by the FPGA card. It receives input voltage and output current information via its on-board analogue to digital converters, and processes this information using a custom FPGA program. The input voltage signals are supplied by a voltage measurement PCB, whilst the output current measurements come directly from the output phase power circuit PCB's.

The FPGA controller program generates the gate signals for the IGBT's which make up the matrix converter power circuit. These signals are derived from the input voltage and output current data. The gate drive signals generated by this program are then fed via a short lead

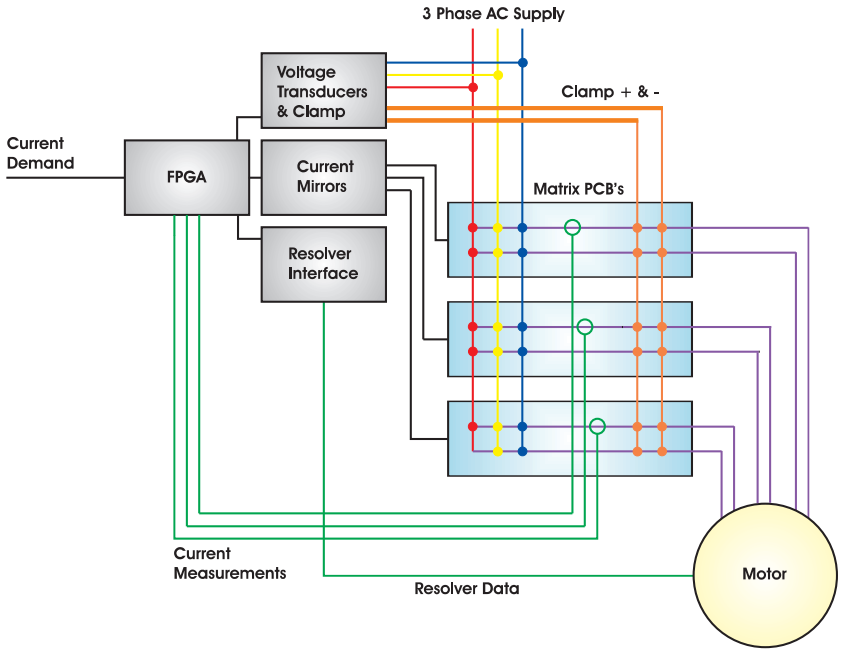

Figure 5.1: Block Diagram Showing the Structure of the 3-Phase SSMC

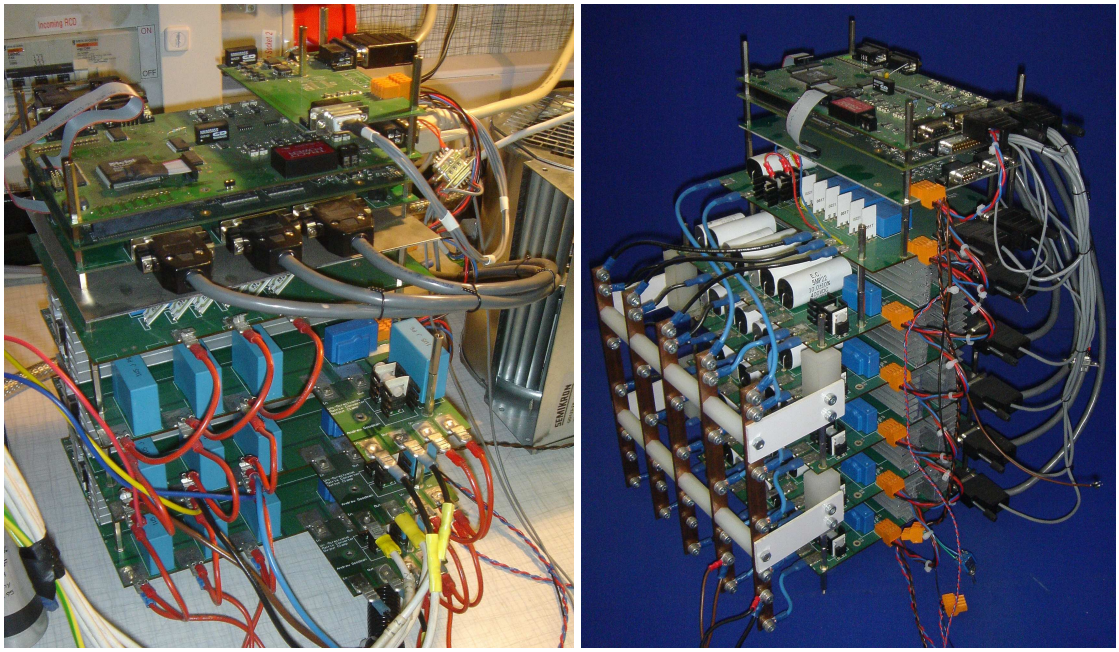

Figure 5.2: Single Sided Matrix Converters. a,3-Phase. b,5-Phase

to a current mirrors PCB. This board takes the gate drive signals in digital voltage form, and converts them to currents, to be fed to the matrix converter gate drive circuits. There is then a matrix PCB for each output phase of the converter.

Each of the elements of the matrix converter will be explained in greater detail in the following sections.

5.1.1 FPGA Controller PCB

The FPGA card used to control the SSMC was originally designed by Lee Empringham from the PEMC group of Nottingham University for the TIMES [49] project. The TIMES project required a controller for a conventional Matrix Converter. A Texas Instrument C6711 floating point DSP and the DSP Starter Kit (DSK) were used, and combined with the developed FPGA card to provide full control and reliable operation of a conventional matrix converter. Whilst fulfilling this role very effectively, the FPGA card has proved to be a very flexible and versatile card in many other applications.

In this application, a completely new program was developed for the FPGA, allowing the SSMC to be controlled without the need for a DSP (although the interface with the DSP was still used whilst developing the FPGA program, and as a data capture utility).

The FPGA chip used is an Actel A500k ProAsic device. This is a non-volatile, easily reprogrammable chip, which combines the benefits of an ASIC (Application Specific Integrated Circuit) with those of a reprogrammable device. It has fully configurable I/O (although many pin functions were fixed, based on the card with which the FPGA was used) and is available in a number of packages and sizes, with varying amounts of embedded RAM and numbers of gates. It has dedicated internal clock routing to minimize clock skew and ensure signal integrity and is available with a comprehensive software suite, used for the full chip software design process. Further detail on the software design can be found in section 5.2. As this research project neared completion, the A500k FPGA chip was announced as being obsolete by Actel, however the same control program could be

developed for the newer devices available.

In addition to the FPGA, the card contains a number of analogue to digital (A/D) converters, digital to analogue converters (D/A), hardware comparators for over-current protection and digital I/O capabilities for trip information output, trip source inputs and event triggering. A photograph of the FPGA card is shown in figure 5.3.

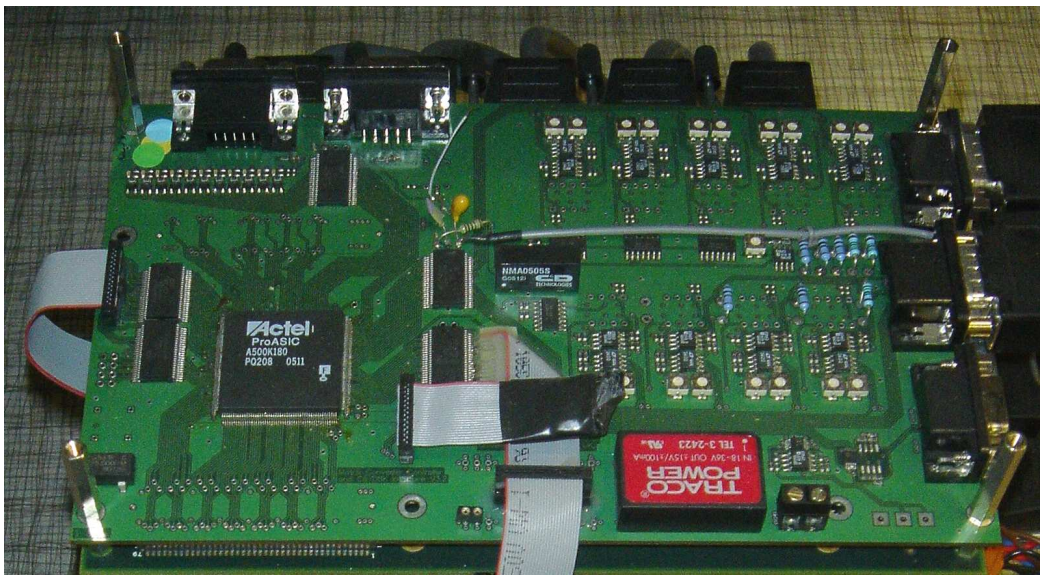

Figure 5.3: FPGA Controller PCB.

There are a total of nine A/D converter chips available on the card. Some have differential inputs and each can be used with a Burden resistor, used to measure the voltage drop across the resistor due to a flow of current. This is necessary as the outputs from the voltage and current transducers are in the form of current. Each A/D chip is also preceded by an Operational Amplifier (Op-amp) chip, which is used to scale the signal to be measured, such that the full input range of the A/D chip is used. In this application the A/D channels are used as in table 5.1. The output current signals for phases X and Y were added at a later stage, as the 5-phase SSMC was developed.

The three hardware comparators have been configured to observe three of the analogue current signals supplied to the A/D's, and generate a trip signal if the currents are above a predefined level. This was set up as a high speed current trip to disable the matrix converter

A/D Channel	Use
1	Current U
2	Current V
3	Current W
4	Voltage A
5	Voltage B
6	Voltage C
7	Current X
8	Current Y
9	

Table 5.1: A/D Channel Assignments

if potentially damaging high currents are seen to be flowing.

The four D/A channels on the card have not been used in this application.

Many of the FPGA pins are used to facilitate the interface with the DSP. This allows full access to the address and data buses of the DSP, and in this application proved very useful as a debugging device, as many of the internal signals within the FPGA could be sampled and stored in the DSP memory, albeit at a sampling frequency lower than the clock frequency of the FPGA. This obviously implies that the very high frequency logic signals could not be sampled accurately, however many of the lower frequency signals related to the general operation of the current controller could be sampled, and allowed for a moderate degree of verification of the controller operation.

Many of the remaining multi-purpose buffered digital inputs to the FPGA were used for functions such as trip inputs, digital interfacing with a resolver decoding chip and output of the gate drive signals to the power IGBT's.

5.1.2 Resolver Interface PCB

Rotor position data is acquired using a resolver, mounted on the rotor shaft. A pair of IC chips are used with the resolver, and mounted on the resolver interface PCB. This can be

seen in figure 5.4.

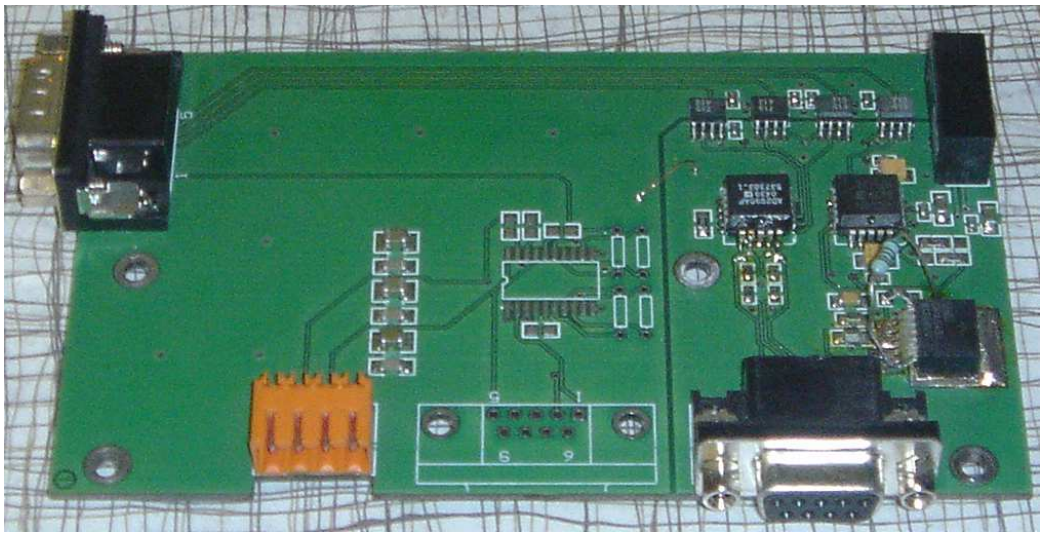

Figure 5.4: Resolver Interface PCB.

The first of these is an oscillator, and provides the sinusoidal excitation waveforms for the primary winding of the resolver. The second is a resolver to digital converter, connected to the two secondary windings of the resolver. The chip converts the analogue waveforms output by the resolver into a number of digital forms. In this application, the absolute serial binary output is used. This produces a 12 bit absolute representation of the rotor position. A three wire serial link is then used to transfer the binary data to the FPGA.

5.1.3 Current Mirrors PCB

The current mirrors PCB is used to generate current signals based on the gate drive signals. These are supplied in voltage form by the FPGA, via buffer chips. The current mirrors PCB can be seen in figure 5.5

As matrix converters produce a large amount of high frequency electro-magnetic noise, it was important to ensure that operation critical signals such as the gate drive signals were highly noise immune. The gate drive signals have to be transferred from the controller

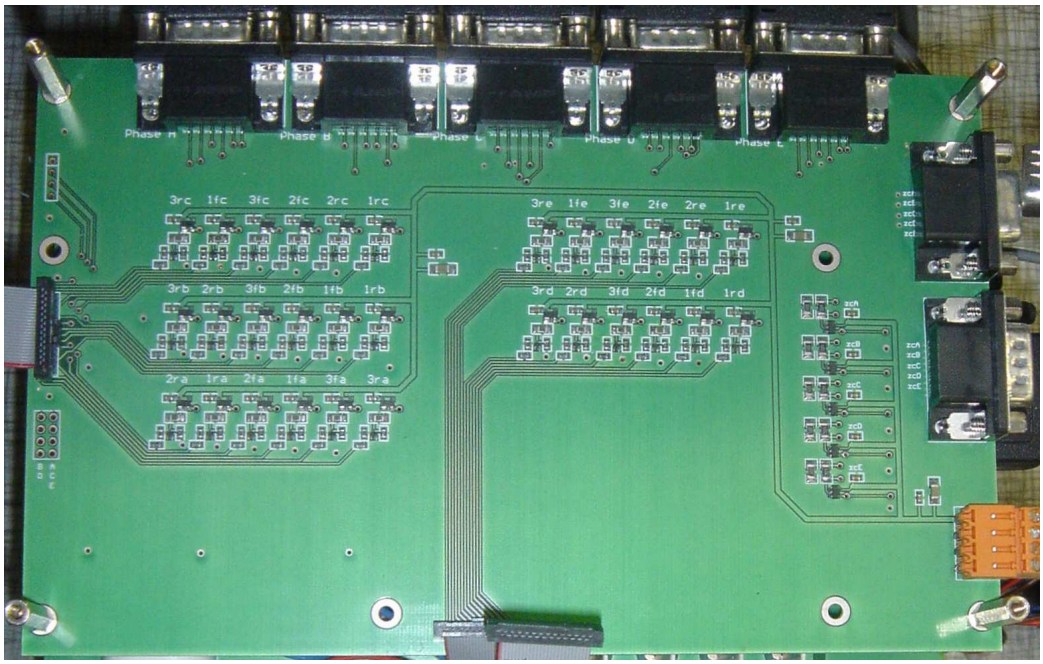

Figure 5.5: Current Mirrors PCB.

card, down to each of the matrix power PCB's, which in this application were arranged in a vertical tower with the controller card at the top.

The most noise immune way to transfer such digital signals would be to use optical fibres, with transmitters and receivers for each gate signal. However the optical transmitters and receivers are costly, so for this prototype the signals were transferred as currents. To add to the noise immunity of the signals, they were transmitted using twisted pair, shielded cables. Figure 5.6 shows the configuration of this transmission circuit, which was designed by Joseph Vassallo [50] as part of his PhD studies.

The circuit uses a MOSFET as a buffer, which is capable of supplying the current required to drive the input side of the current mirror. There is then a matched pair of BJT's which form the active part of the current mirror. The output current is then fed to the matrix power PCB via one wire of a twisted pair, through the current setting resistor on the matrix PCB, and then back along the second wire in the twisted pair. The circuit is then terminated back on the current mirrors PCB, with a connection to ground (Dgnd1). The ground side of the

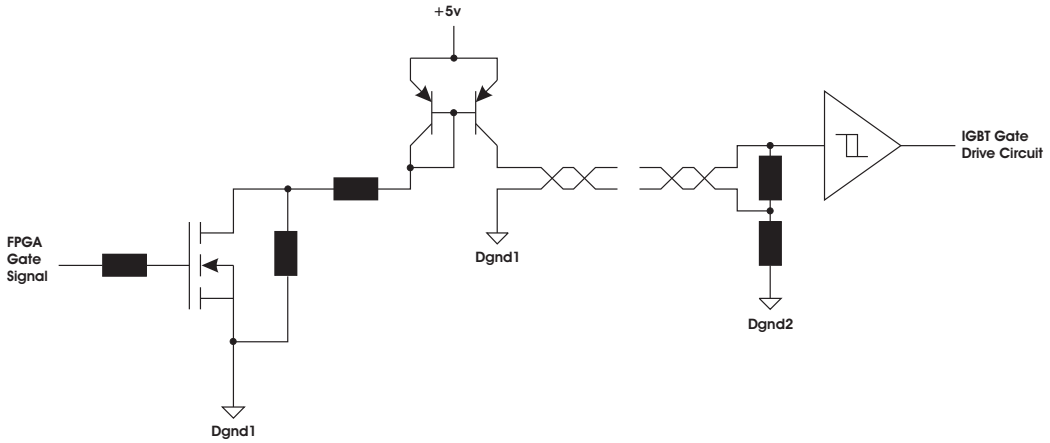

Figure 5.6: Gate Drive Signal Transmission Circuit, employing Current Mirrors.

twisted pair is also connected to the ground of the matrix power PCB (Dgnd2) via a low value resistor, to link the two grounds whilst minimising earth loops.

The use of a twisted pair here reduced the loop area, minimising the inductive coupling with sources of magnetic noise. The six pairs of wires to each matrix PCB were also shielded, reducing the susceptibility to interference by electric fields via capacitive coupling.

5.1.4 Voltage Transducers and Clamp PCB

The operation of the SSMC requires measurement of the input voltages. As this prototype SSMC was designed in an expandable form, with a separate matrix PCB for each output phase, it was logical to house the input voltage transducers and input voltage clamp on a separate PCB. This is shown in figure 5.7.

The voltages measured are the three line to line voltages. It would have been possible to measure just two of the line to line voltages, and reconstruct the third, however this would have introduced additional computational demands, and may not have been accurate, especially if significant distortion and imbalance were present, or induced on the voltage supply.

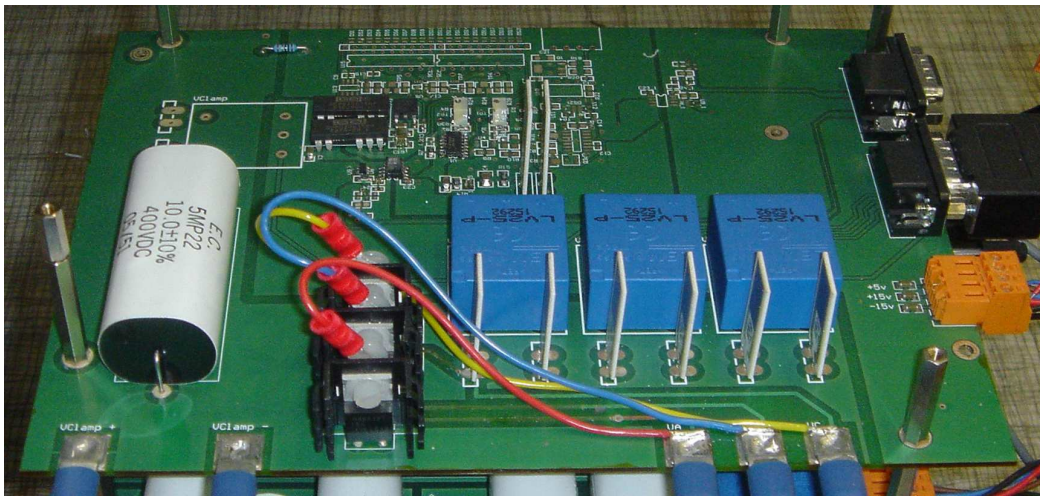

Figure 5.7: Voltage Transducers and Clamp PCB.

The input voltage clamp uses a very high speed diode bridge to rectify the supply voltage into a small capacitor bank, as was given in the SSMC topology in figure 3.1. Once the clamp is charged, any voltage spikes occurring on the supply, which would be potentially damaging to the converter power components are rectified into the clamp. In this way they are never seen by the power electronic devices of the converter.

The input clamp circuit also shares its capacitor bank with the output clamp, which performs a similar function on the output side of the SSMC. Further details on the output clamp can be found in section 5.1.5.1. In this configuration the input clamp acts as a pre-charge circuit for the output clamp. This means that the large current spike drawn when charging the clamp does not flow through the SSMC power devices.

5.1.4.1 Clamp Voltage Monitoring Circuit

The clamp voltage monitoring circuit is used with the five phase SSMC. The trip in the 3-phase version is implemented within the FPGA and uses a voltage transducer.

The clamp voltage monitoring circuit floats at the lower rail voltage of the clamp capacitor.

An isolated floating power supply chip is used to supply the circuit. A potential divider circuit is used to scale down the upper rail voltage of the clamp. The output of the potential divider is used as one input of a comparator chip. The second input is a reference voltage, which represents the maximum voltage level that the clamp capacitor should be allowed to reach. If the scaled down clamp voltage becomes larger than the reference voltage, the output of the comparator switches. This output is fed to a digital input of the FPGA, via an opto-isolator chip.

5.1.5 Matrix Power PCB

The matrix power PCB houses the uni-directional matrix converter switches and interconnecting power planes. This forms the basis of the hardware of the SSMC, and was a custom design for this project. It is shown in figures 5.8 and 5.9, in both unpopulated and populated states respectively. High resolution photos of the unpopulated matrix PCB can also be found in appendix F. The PCB contains the following features:

- Power switching devices
- Laminated power planes
- Gate drive circuit
- Output Clamp
- Output current measurement

The matrix PCB structure can be separated into three main areas, each of which required different design considerations.

- High Current, High Voltage Conduction Areas
- Gate Drive Circuits at floating voltages
- Low voltage control and measurement signal areas

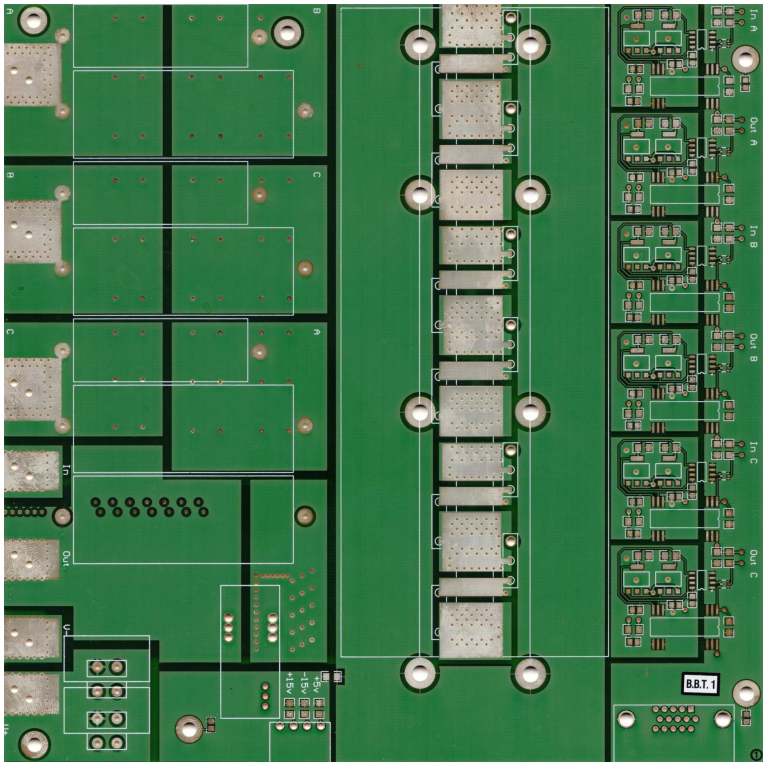

Figure 5.8: Matrix Power PCB - Unpopulated

5.1.5.1 High Voltage/High Current Areas

When designing the circuit layout for the high voltage, high current areas of the matrix converter, it was important to minimise any stray inductance close to the power electronics. Any inductance between the power electronic switches, input filter capacitors and clamp diodes would lead to significant voltage spikes being generated at each commutation due to the high turn off speed of the IGBT's used. The inductance of a short length of wire could generate spikes of tens or even hundreds of volts which could easily create collector to emitter voltages greater than the device ratings.

To ensure the stray inductance within the power circuit was minimised, laminated power planes were used for these interconnections. The laminated power planes were formed in this case using layers of a six layer PCB. The major function of each layer is as shown in table 5.2. The 6 Matrix PCB layers can be seen in appendix F, with labels indicating the

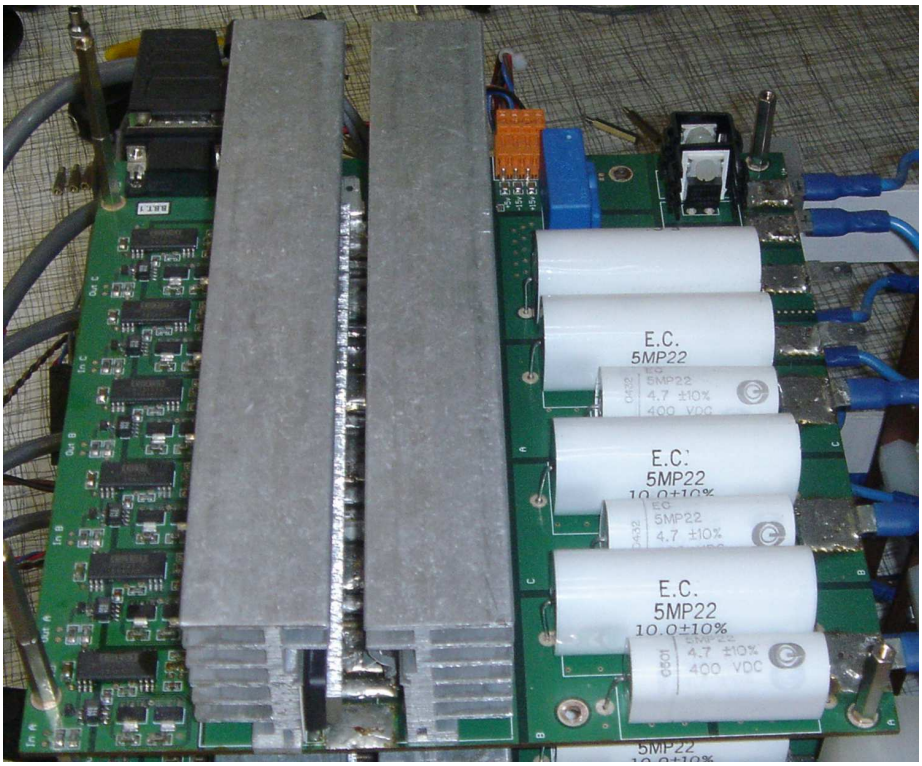

Figure 5.9: Matrix Power PCB - Populated

function of various areas.

Also connected using the laminated power planes were the output current measurement transducer and the output clamp circuit. The current transducer was connected such that the current flow out of the matrix PCB was first directed through the transducer. The output voltage clamp was connected in parallel with the output, and used very high speed diodes, arranged in a diode bridge rectifier configuration to rectify any large voltage spikes, as shown in figure 3.1.

The second, and more significant job of the output clamp is in providing a safe output side current path in the event of commutation failure, or an emergency shut-down of the drive, where all IGBT gate drive signals may be grounded. In this case the inductive energy stored in the motor is dumped into the clamp capacitor, via the rectification diodes. The clamp used in the experimental rig used a large electrolytic capacitor for ease of testing and

Layer	Use
1	Device/Layer Interconnections
2	Input Phase A
3	Input Phase B
4	Input Phase C
5	Output +
6	Output -

Table 5.2: Matrix PCB Layer Usage

development.

Sizing of the clamp capacitors is based on calculation of the inductive energy stored within the motor phases, using equation 5.1.

$$W_{Load} = \frac{1}{2} L(i_a^2 + i_b^2 + i_c^2 + ... + i_x^2) \tag{5.1}$$

where:

W_{Load} = Energy in Inductive Load (J)
L = Inductance of Load (H)
i = Load Phase Current Flowing (A)

This is then equated to equation 5.2, governing energy stored in a capacitor.

$$W_{Load} = \frac{1}{2} C_{Clamp}(V_{MAX}^2 - V_{INI}^2) \tag{5.2}$$

where:

W_{Load} = Energy in Inductive Load (J)
C_{Clamp} = Clamp Capacitance (C)
V_{MAX} = Maximum Allowable Clamp Voltage (V)

V_{INI} = Initial Clamp Voltage (V)

The motor used during the testing stages of the SSMC is described in section 6.1. Using the values given in table 5.3, and assuming that the maximum current is flowing in 2 motor phases (one of which will have the unaligned inductance, and one of which could have the fully aligned inductance), the required clamp capacitance can be calculated to be 599uF. However, a pair of 2200uF capacitors were available, and were connected in series, giving 1100uF of clamp capacitance.

Layer	Use
Maximum Phase Current	40A
Minimum Phase Inductance	12mH
Maximum Phase Inductance	60mH
Voltage Limit of Devices Used	600V
Maximum Allowable Clamp Voltage	500V
Initial Clamp Voltage	240V

Table 5.3: Values Required to Calculate Clamp Capacitance

A bleed resistor was also connected across the clamp capacitance in order that any rise in voltage due to energy dissipated into the clamp due to incorrect switch timing or voltage spikes can be removed. The resistor value and power rating are calculated based on the maximum voltage that the clamp should see, which is given in table 5.3 as 500V. A pair of 68kohm, 12W resistors were available, which were connected across each of the series capacitors, equalising the voltage distribution between them. Using Ohms law (equation 5.3), and the fact that each of the series clamp resistors will see a maximum of 250V, the worst case current flowing through the resistor can be calculated as 3.67mA.

$$V = IR \tag{5.3}$$

The power dissipated in the resistor for this worst case can then be calculated using equation 5.4, which for this case comes out as 0.92W. This is very safely within the power limits of the resistor.

$$P = I^2 R \tag{5.4}$$

Finally, the voltage to which the capacitance will discharge after a certain time can be calculated using equation 5.5.

$$V_t = V_I e^{\frac{-t}{RC}} \tag{5.5}$$

where:

V_t = Voltage at time t (V)
V_I = Initial Voltage (V)
R = Bleed Resistor Value (ohms)
C = Capacitance (F)

As an example here, assuming the clamp reaches its maximum voltage of 500V, each capacitor will have 250V across it. Using the 68Kohm resistors, the clamp voltage will have reached 167V after 60s, and 50.3V after 240s.

Ideally an active clamp [41] would be added, such that these electrolytic capacitors could be removed. This uses a chopper IGBT and lower value, high power resistor connected in series across the clamp capacitance, and is controlled such that when the clamp voltage rises, the power is dissipated at a high rate (but for a brief period), through the low value resistance. This implies that the clamp energy can be dissipated faster, and therefore a lower value of clamp capacitance is necessary.

5.1.5.1.1 High Voltage Implications The high voltage differences present within the Matrix PCB require adequate separation between layers, and planes within layers, such that breakdown of the insulation does not occur. The FR4 insulating material used within the PCBs has a dielectric strength of approximately 20kV/mm, implying that 20kV can be

applied across 1mm of material without any breakdown in the insulating properties of the FR4. The 6 layer PCBs used have a minimum FR4 thickness of 0.21mm between layers, giving a safe operating voltage of 4.2kV between PCB layers.

When designing the spacing between planes on individual layers, the spaces were treated as air. In reality this space would be filled with the glue used to fix the layers together. The glue would have a greater dielectric strength than air, however its value was not known, so assuming air (which has a low dielectric strength) would provide the safest design. The dielectric strength of air is approximately 3kV/mm. However, as required board area was not a significant concern for the prototype, compared with reliability, a minimum separation between plane areas of 2.5mm was allowed.

The edges of the PCBs were also coated with insulating varnish to maximise the insulation between layers at the edge of the PCB. This was necessary as the vertical separation between some layers was only 0.21mm. As the dielectric breakdown voltage for air is only approximately 3kV/mm, this gives a breakdown voltage of approximately 630v between layers at the PCB edge. This clearly does not allow a significant safety margin when 415V AC mains is applied across layers. This was an oversight when the PCB was designed. Ideally the planes would terminate several millimetres short of the PCB edge, such that the separation between planes is the FR4 thickness plus the distance between the edge of the layer and the edge of the PCB.

5.1.5.1.2 High Current Implications The high current requirement had implications regarding the cross sectional area of copper required within the copper PCB layers. The copper thickness was fixed for this prototype by the PCB manufacturer, so the width of the planes became the variable, affecting the temperature rise of the PCB for a given amount of current. Also, where current needed to flow between layers, enough appropriately sized and spaced vias were required.

In order to design the matrix PCB, an approximate calculation was preformed to determine the required current output capability. This was based on the requirements of the Switched Reluctance motor, and the initial specification decided upon for this. This was for a

15kW motor to be supplied from 415V rms phase-phase AC mains, via the SSMC. As the arrangement of the SSMC is analogous to a diode bridge rectifier, the average voltage available to control the load currents under full load conditions, is approximately 560 volts DC. This is the rms of the rectified 415V supply. From this the total current into the machine can be approximated as 27A for a 15kW output. As there are 3 phases in the SR motor, this implies an average of 9A per phase. The phase currents are supplied to the motor in pulses, covering approximately a third of each revolution, therefore each pulse must average approximately 27A. Both of these values are important for designing the power section of the matrix PCB; average current ratings are used to specify the cross sectional copper area on the PCB, and both the average and peak values are important when selecting IGBT's and current transducers. This is clearly a very approximate method for specifying required currents for a given power output, however as actual power output was not considered a particularly important factor for the purposes of the research, it was deemed to be a sufficient method.

It was later decided that the same PCB design for the converter would be used to supply the PMDC motor for the SATOW project. The initial specifications for the converter changed as the design for the motor was developed to meet the load requirements, and the current requirements became higher than those of the Switched Reluctance motor. As discussed in section 3.2.2, each phase of the SSMC for the SATOW project would be required to conduct for pulses covering 2/5^{ths} of each revolution. In order for the motor to produce the required maximum power output, these pulses would need an amplitude of 40A. This would only be required for a short period, of approximately 1 minute, so the heating effect would be reduced, however it is now clear that extra cooling may be necessary to ensure safe operation of the matrix PCB's of the SSMC, at the full load conditions of the SATOW motor [45], as at this point the PCB design had been finalised to meet the requirements of the Switched Reluctance motor.

5.1.5.1.2.1 Copper Area Required Both the width of copper plane on the PCB layers, and the number of vias connecting between layers are important variables in the design process of PCB's, when considering the current handling capability.

The method used to determine the width of copper required for a known copper thickness and acceptable temperature increase of the PCB, in order to carry the required current uses equations 5.6 and 5.7.

$$W = \frac{A}{T \times a} \tag{5.6}$$

where:

W = Required Track Width (mils)
A = Required Cross Sectional Area of Copper ($mils^2$)
T = PCB Copper Thickness (oz)
a = 1.378 (mils/oz)

and:

$$A = \left[\frac{I}{(k \times (\Delta t)^b)}\right]^{\frac{1}{c}} \tag{5.7}$$

where:

A = Required Cross Sectional Area of Copper ($mils^2$)
I = Current Conducting Requirement (A)
Δt = Acceptable Temperature Increase (^{o}C)

	Internal Layers	External Layers
k	0.024	0.048
b	0.44	0.44
c	0.725	0.725

Table 5.4: IPC-2221 Constants

The Values in table 5.4 are the result of curve fitting to the IPC-2221 (2003)[51] curves. The IPC (Association Connecting Electronics Industries) has produced standard IPC-2221,

and state that "the standard establishes the generic requirements for the design of organic printed boards and other forms of component mounting or interconnecting structures". IPC-2221 is the IPC's 'Generic Standard on Printed Board Design', which covers many aspects of the qualities and use of printed circuit boards and the materials commonly used to manufacture them.

Using the above method, tables 5.5 and 5.6 were produced. These show the width of copper plane required to carry the SSMC currents for the available 6 layer PCBs, when supplying both types of motor. These PCBs have 35 micron plating thickness on all layers. The values in the tables are for internal layers, as these are the layers which require the greater conductor width, as they have much reduced cooling capacity. The pulsed current rating is the amount of current required in each pulse, while the continuous current rating is the average current seen to flow through the PCB, based on the type of motor being driven, and the required pulse periods. The second rating is the figure used to calculate the required copper widths for the 6 layer PCBs. These figures were used as guidance when designing the matrix PCB.

Current Rating(pulsed) [A]	5.0	10.0	15.0	20.0	25.0	30.0
Current Rating(continuous) [A]	1.7	3.3	5.0	6.7	8.3	10.0
Required Trace Width [mm]	7.4	19.2	33.6	50.0	68.0	87.4

Table 5.5: Required PCB copper widths for SR Motor SSMC (using internal layer IPC values)

Current Rating(pulsed) [A]	10.0	20.0	30.0	40.0
Current Rating(continuous) [A]	4.0	8.0	12.0	16.0
Required Trace Width [mm]	24.7	64.2	112.4	167.1

Table 5.6: Required PCB copper widths for SATOW Trapezoidal PMDC Motor SSMC (using internal layer IPC values)

In order to calculate the minimum number of vias required to conduct the current between layers, the calculations described in equations 5.6 and 5.7 were used. They were however calculated for external layers, as all vias have an external face. All vias also have the same

35 micron plating thickness as all layers. This produced the copper width values in tables 5.7 and 5.8 . Dividing the required trace width by the 1.57mm via circumference, for the 0.5mm diameter vias, gives the approximate number of vias required, as can also be seen in the tables.

Current Rating(pulsed) [A]	5.0	10.0	15.0	20.0	25.0	30.0
Current Rating(continuous) [A]	1.7	3.3	5.0	6.7	8.3	10.0
Required Trace Width [mm]	2.8	7.4	12.9	19.2	26.1	33.6
Required number of Vias	2	5	8	12	17	21

Table 5.7: Required number of PCB vias for SR Motor SSMC (using external layer IPC values)

Current Rating(pulsed) [A]	10.0	20.0	30.0	40.0
Current Rating(continuous) [A]	4.0	8.0	12.0	16.0
Required Trace Width [mm]	9.5	24.7	43.2	64.2
Required number of Vias	6	16	27	41

Table 5.8: Required number of PCB vias for SATOW PMDC Trapezoidal Motor SSMC (using external layer IPC values)

Again these numbers were taken into account when designing the matrix PCBs. These values were however less significant than the copper width values, as many of the vias were also loaded with solder, producing a far larger conductor cross sectional area.

5.1.5.2 Gate Drive Circuit

The gate drive circuit takes the gate signal provided by the FPGA as its input, and supplies the gate of the respective IGBT with a voltage either significantly higher or lower than the emitter voltage. This causes the IGBT to become either forward or reverse biased, and conduct or block the flow of current. Because the emitter voltage levels float with either the supply or output voltage, Texas Instruments DCP020515DU floating power supplies were used for the gate drive circuit. These use the emitter voltage of the IGBT as the zero volt reference on the output side, and provide +/-15V from the +5V supply at the input.

The first stage of the gate drive circuit is a resistor, connected between the two wires of the twisted pair which carries the gate drive signal. This converts the current fed from the current mirrors into a detectable voltage, as was seen in figure 5.6. The high end of this resistor is connected to the input pin of an open collector schmitt triggered inverting logic gate. The schmitt trigger is included as a precaution, so as to minimise the effects of any noise spikes which may be generated on the gate drive signal in particularly high noise environments. The output of the inverting gate is connected to the input of a gate drive opto-isolator chip. This transmits the gate signal optically, and provides galvanic isolation between the gate drive circuit, and the input signal ground. The gate drive circuit from this point is given in figure 5.10.

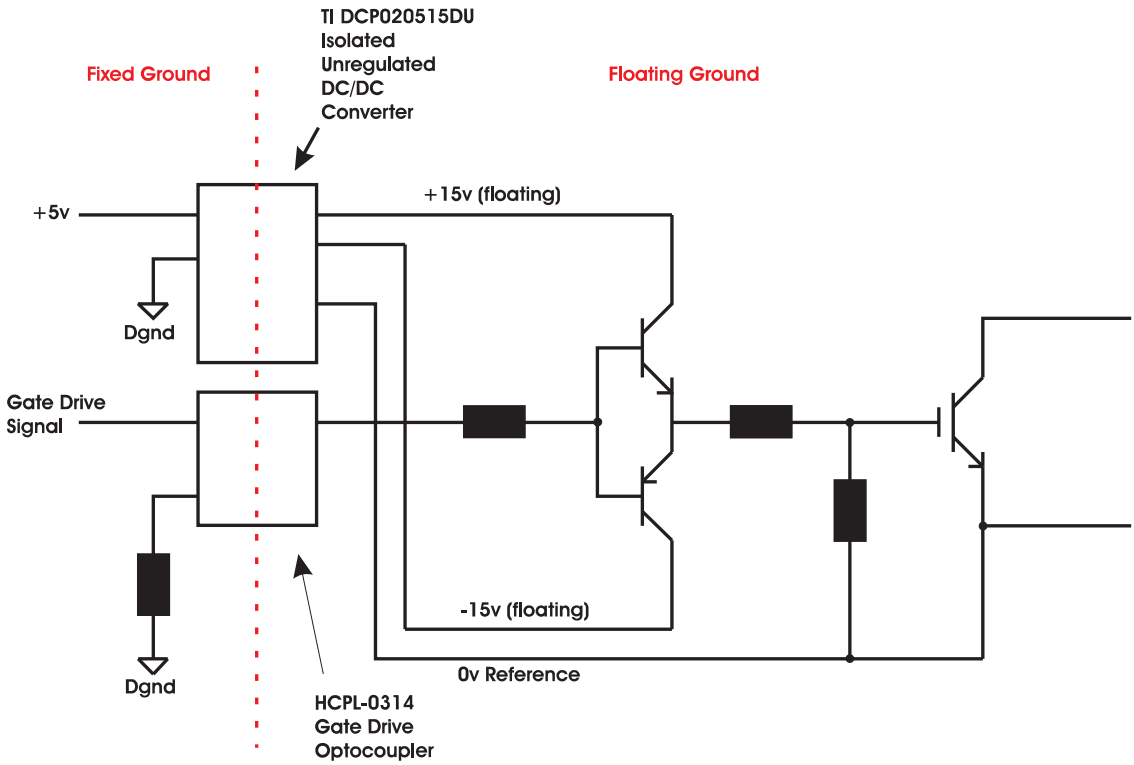

Figure 5.10: IGBT Gate Drive Circuit

The output stage of the opto-isolator is a push-pull transistor pair suitable for supplying the IGBT gate directly, however the current rating was not sufficient. Therefore a second push pull transistor pair was formed using discrete transistors. The output of this pair

was fed to the IGBT gate, via the gate drive resistor. The gate drive resistor was selected such that commutation between phases would occur in as short a time as possible, taking into account the IGBT properties. Commutating too quickly would create large voltage spikes, due to the small parasitic inductance still present within the circuit. Initially, basic calculations were performed to find a suitable gate drive resistance. Tests were then carried out to optimise the value.

Clearly, the different sections of the gate drive circuit were operating within +/-15V of each other, so large track separations were not required. A border zone around each gate drive circuit was however required, as the full supply phase to phase voltages could be present between individual gate drive circuits.

5.1.5.3 Low Voltage Control and Measurement Signals

The Matrix Power PCB carries both low and high voltages. To ensure that the low voltage signals were as noise immune as possible, and protected from interference generated by the large voltage transitions present in the high voltage areas, large ground planes were used. Also, many of the signals were distributed throughout the board using the internal layers of the PCB.

The low voltage signals consist of the gate drive signals , and the output current measurement signal. These are transmitted to and from the Matrix PCB as currents. Noise immunity of the current measurement signal is especially important, as it is an analogue signal. For this reason, the current measurement signals are individually shielded.

5.1.5.4 Mechanical Considerations

In addition to the electrical considerations when designing the PCB, certain mechanical requirements needed to be met. The power IGBTs and diodes used required sufficient cooling, provided by a heatsink. Two heatsinks were used on each PCB, each of which was attached directly to the PCB using screws, through holes which were incorporated into the

PCB design. This ensured that none of the mounting stresses were carried by the IGBT legs. A plane was also provided below the heatsink, which linked to the screw holes and provided a simple solution to grounding the heatsinks.

Mounting holes were also incorporated into the PCB which allowed pillars to be used to stack the individual output phase matrix PCBs rigidly, as a single unit.

5.2 FPGA Controller Design

An FPGA was used to control the SSMC. This monitors the input voltages and output currents of the matrix converter, and using the control algorithm implemented within the FPGA program, determines which switches of the matrix converter should be activated in order to control the output current at the required level.

The program used in the FPGA was developed specifically for this project, and implemented both the single band and double band hysteretic control techniques. Actel's Libero development suite was used to produce the program. Libero contains a number of programs, which perform the following functions:

- Program Development.
- Simulation.
- FPGA chip internal layout design.
- Production of final 'staple' file, used for programming.

The FPGA program is written using the VHDL programming language. The code for this may be input directly, or alternatively the 'ViewDraw' program included with Libero may be used to generate the VHDL. The ViewDraw program is generated graphically, using blocks to represent particular functions. Many of these blocks are generated using macros, produced by a further element of Libero, 'SmartGen', which generates customisable blocks

such as logic gates, registers and counters. Other blocks can be produced to represent VHDL code input directly by the programmer. The SSMC control program was developed in this way, using a combination of programming methods. The VHDL code for the final controller program, which was able to implement both the single and double band control techniques, was in excess of 220,000 lines. This demonstrates the value of such a graphical, partially automated programming technique, as entering such a length of code manually would be both time consuming, and its operation would be inherently difficult to visualise.

Throughout the programme development, simulations are performed using 'ModelSim'. A stimulus file is generated for a particular block, using 'WaveFormer'. The simulations may be carried out at three stages of development:

- Pre-Synthesis.
- Post-Synthesis.
- Post-Layout.

The pre-synthesis simulation simply tests the function of the block under ideal conditions, whilst the post-synthesis and post-layout simulations introduce the delays due to signal propagation times and clock skew. The time required to generate a stimulus file and thoroughly examine the program's responses for the complete control program would have been unrealistically high for this project. All individual program sections were however simulated to a high degree, as identifying any bugs at this stage would be far easier than once the complete program had been assembled, and was being implemented in the actual converter.

5.2.1 FPGA Design Considerations

When producing an FPGA program, one must remember that the end result is a synchronous logic circuit layout. This makes the programming technique somewhat different

to producing a program for either a computer or a Digital Signal Processor (DSP). The most important factor to bear in mind is that the programmer is responsible for ensuring the validity of data at every step of the synchronous program.

5.2.1.1 Data Validity

All numbers handled by the FPGA are represented in binary form. This implies that multiple 'lines' are used for each number. There is no dedicated routing resource within the FPGA chip, so these lines may take any available path through the FPGA between operational blocks. Although Libero attempts to minimise propagation delays it is likely that these paths will have varying propagation times. Also, operations on one line may take longer than operations on a second. For this reason, registers are used between operations, ensuring that a complete set of valid data is present at the input to the register, before being clocked through to the next operation, by the system clock.

5.2.1.2 Numerical Manipulation

Another very significant implication of producing an FPGA program is that the numerical manipulation capabilities of the FPGA are limited. Smartgen can be used to produce Adders, Subtractors and Multipliers, which reach the final value within a single clock cycle. Division on the FPGA is however a far more complex and time consuming operation, and there is no SmartGen macro available for producing such an operator. Division by any integer is possible, and a method was implemented during the development of the SSMC controller, but is based on an iterative method. The number of clock cycles required by the method tested was the number of bits of the input values, plus one. This is clearly not ideal for the very high bandwidth control loops, and division by such numbers was therefore avoided.

The alternative approach to performing actual division is bit-shifting. By shifting the characters of the binary representation of a number 'n' positions to the right, the number

is divided by 2^n. This is a highly efficient method for performing division, however the denominator has a limited number of values ie. 2^n. Where division by a constant is required, a combination of a multiplication, followed by a bit-shift can be used. This allows division by any integer in just two clock cycles. A combination of multiplication by a large non 2^n number, followed by a large bit-shift to reduce the number back within its original range also allowed for multiplication by very small scaling factors with multiple decimal places. This was necessary when correcting the values measured by the A/D converter chips, as the transducers used had a significant offset associated with them. Clearly the resolution of the number is decreased as the value is shifted back down, as the least significant bits are lost, however this did not cause a problem.

5.2.1.3 State Machines

A state machine is a device in which the output is a function of both the immediate inputs to the system, and a previous state. The operation of a state machine may be displayed as either a state diagram or state table. Table 5.9 and figure 5.11 show a state table and state diagram respectively for the same example system.

Present State		Input	Next State		Output
Q1	Q2	X	A	B	Y
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	0	1

Table 5.9: Typical State Table

In order to ensure that the previous state data is valid, registers are used at the input, clocking the data into the state machine at a fixed frequency. This applies to all inputs

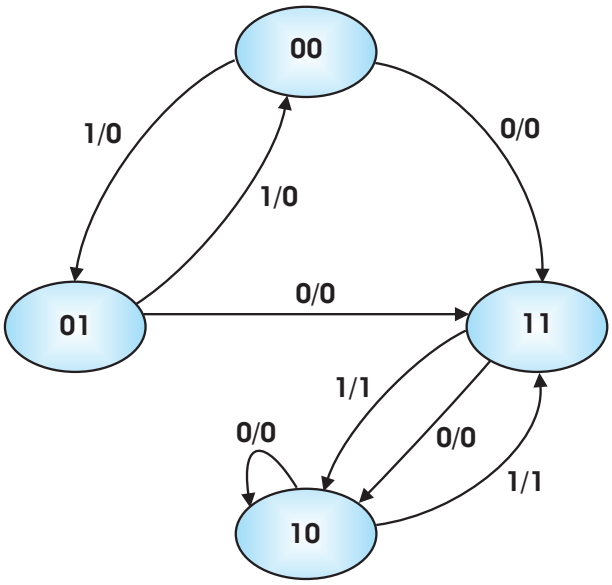

Figure 5.11: Typical State Diagram.

to that state machine, not just the previous state data.

Elements of the control operation for both the single band and double band control methods for the SSMC were represented using truth tables when first defining the operation of the control strategy, and when simulating the controller using the Simulink element of Matlab. From these 'truth', or 'state' tables, it was possible to generate VHDL code for the state machine, to be input directly into Libero.

5.2.2 Control Structure

An overview of the control structure for the SSMC can be seen in figure 5.12, while figure 5.13 gives a graphical overview of the top level of the FPGA program. An explanation of the operation of the FPGA program is then provided in the following sections, along with graphical representations of the program following one path down through the hierarchy of program blocks within the phase current controller, finally reaching a section of VHDL code representing a Mealy State Machine.

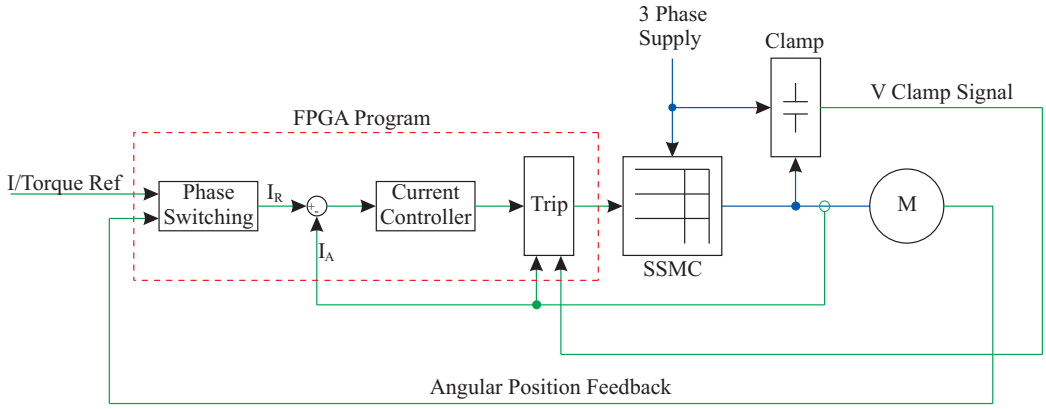

Figure 5.12: Control Structure.

5.2.2.1 Transducer Data Acquisition and Processing

The most significant inputs to the FPGA in terms of current control are the measured voltages and currents, and the rotor position data. These are supplied to the FPGA in serial form, by the analogue to digital converter chips, and the resolver to digital converter chip. A program block within the FPGA then converts the serial A/D data into parallel format. This block was originally produced by Lee Empringham, as part of the conventional Matrix Converter control program. A modified version was then used to convert the serial data from the resolver to digital converter chip. The remainder of the SSMC control program was developed entirely for this project.

Once converted to parallel data, scaling factors and offsets are applied to the A/D values. The offset correction is necessary as it accounts for the inherent offset associated with the current and voltage transducers. The scaling factors are applied, firstly to ensure that the transducer values are balanced, and secondly to scale the values such that each increment of the binary number represents a suitable increase of the measured value. The required scaling factor was calculated from measured data. The process for applying a typical scaling factor would be:

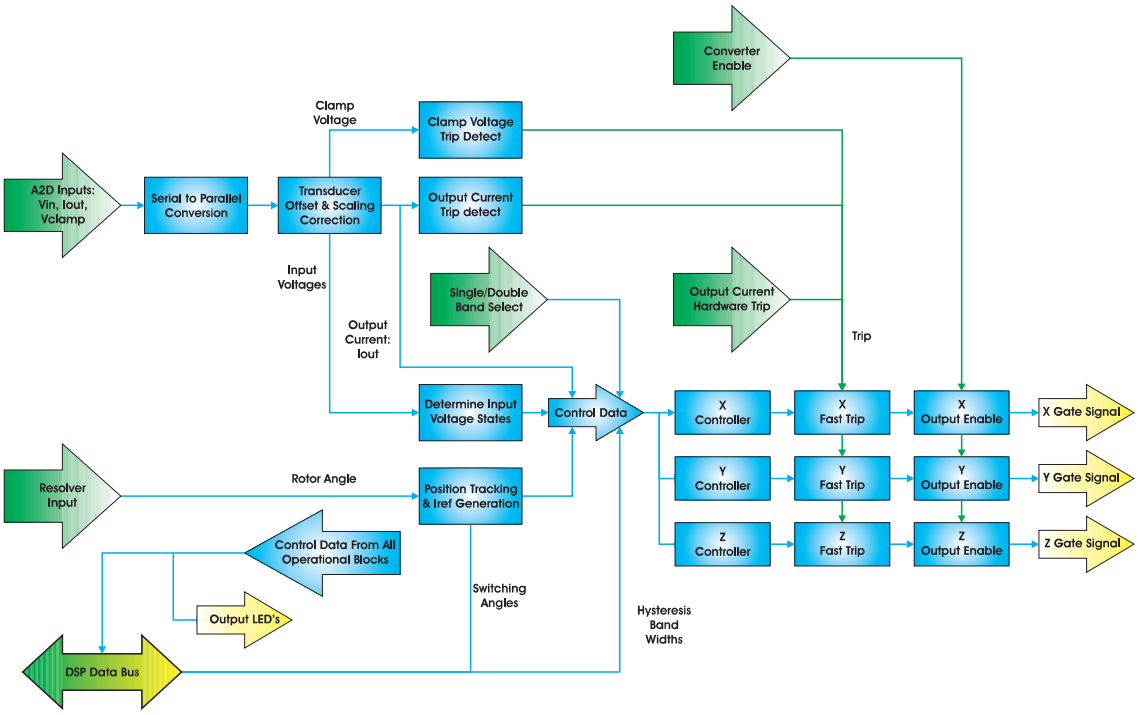

Figure 5.13: FPGA Program Structure - Top Level.

1. Required Scaling Factor of 0.9434 obtained from experimental tests.

2. Scaling Factor of 0.9434, multiplied by 1024, becomes 966. This value is stored in the scaling factors lookup table within the FPGA program.

3. Measured A/D value is multiplied 966.

4. Result is bit shifted 10 bits to the right, dividing by 1024. The bits representing the decimal places are dropped, but the integer part of the value has been correctly scaled by the required scaling factor of 0.9434.

The offset is then applied using a simple summing process.

5.2.2.2 Input Voltage State Determination

A simple analysis of the input voltages is then performed, as required by the control scheme. Comparisons of each phase voltage with respect to the others, and with respect to zero are performed, as in table 5.10. This creates 6 logic signals, defining which of the 12 possible states the input voltages are in, as given in figure 3.2

Signal Name	Comparison Performed	Equivalence
X	$BA > 0$	$B > A$
Y	$0 > AC$	$C > A$
Z	$CB > 0$	$C > B$
a	$AC > BA$	$A > 0$
b	$BA > CB$	$B > 0$
c	$CB > AC$	$C > 0$

Table 5.10: Input Voltage state signals

5.2.2.3 Resolver Data Processing, Filtering and Current Reference Creation

The resolver interface PCB is discussed in section 5.1.2. The communication with the interface chips was via a three line serial interface. The three lines are:

- Chip select (input)
- Clock (input)
- Data (output)

When data is to be read, the chip select line is taken low. Twelve clock pulses are then applied to the clock pin, before the chip enable is again taken high. The data bits are output from the chip on the Data pin, on the negative edges of each of the clock pulses.

The block produced by Lee Empringham for accessing the A/D converter chips was modified to produce the required interface with the Resolver interface chip, as it used a very similar serial interface. This converts the serial binary data into parallel data, for use within the SSMC control program. Because the SSMC controller does not operate at a fixed frequency, the resolver interface block is set up such that it continually interrogates the resolver interface chip at the highest possible frequency, providing the most up to date position data.

A filter block then follows. Although all communication leads are fully shielded, it is feasible that electromagnetic interference from the high frequency switching of the matrix converter could introduce noise onto either the analogue signals present around the resolver, or onto the digital communication lines used to connect the resolver interface chip to the FPGA input buffer. In order to ensure that any noise picked up on the leads does not affect the position tracking capabilities of the SSMC control program, it was decided that a selective filter should be implemented, which would reject bad values. This works on the basis that there should be a maximum difference between consecutive samples. If the difference between two samples is greater than a pre-determined value, the new sample is not allowed to pass into the control program. The following sample is then compared with the previously allowed sample, and if it is back within the range of the pre-determined value, it is allowed through.

The operation of the filter block was tested in a particularly electrically noisy environment, and its effect can be seen in figure 5.14.

This type of filter is clearly only able to remove bad values which are greater than a particular value. An averaging filter would be the alternative, and could further smooth out the data. It would however introduce a small error onto a large number of sampled values once a bad sample had occurred. It would also introduce a delay onto all sampled values, due to the averaging nature of the filter. This could generate significant positional inaccuracies at the maximum speed of 10,000 rpm at which the five phase PMDC motor is designed to operate.

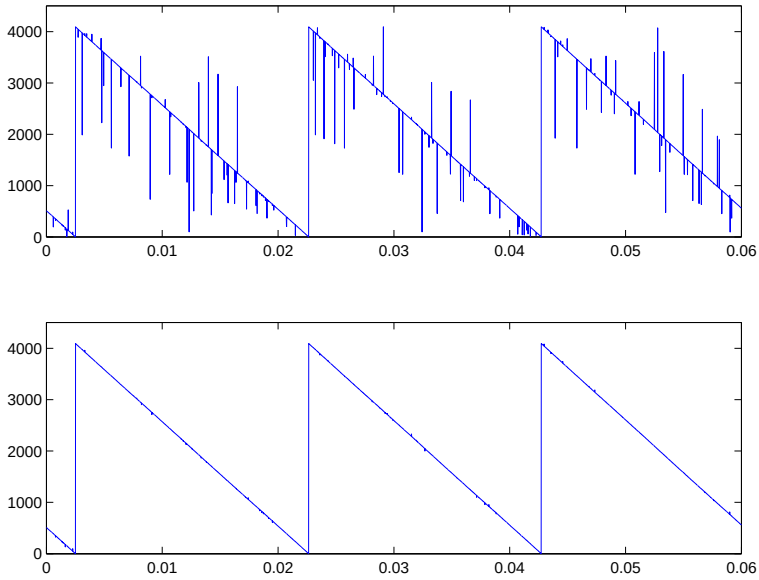

Figure 5.14: Sampled resolver data, before and after filtering.

Both the filtering of this signal and the shielding and data transmission between the resolver interface PCB and the FPGA controller PCB could be improved, however this had a satisfactory effect, and enabled the testing of the SSMC operation.

An offset is then applied to the filtered resolver data. The way this is achieved demonstrates one of the methods available when handling numerical data at a binary level within the FPGA. The offset is applied such that the zero position of the resolver can be synchronised with a particular rotor position. This simply requires the addition of the offset value to the resolver value, as the resolver interface chip outputs values from 0 to 4095, using the full range of values possible with twelve binary bits. If the full range were not already used, a correction would be required as the resolver value passed zero.

Table 5.11 demonstrates the application of an offset of 10 to the resolver value within the FPGA. The first column shows the sequence of sampled data. Columns 2 and 3 show the sampled data after the application of the offset, if 13 bits were being used. One can see that the corrected resolver value counts too high (greater than 4095), then steps down to 10 rather than zero before counting up again This would create positional errors with the

phase switching. However, when the most significant bit is removed as in columns 4 and 5, reducing the representation to 12 bits, the corrected value steps down to zero after reaching 4095 and counts up correctly. Obviously this is count direction independent, and will work if the motor and resolver are run in either direction.

Sampled	Offset allowing 13 bits		Offset allowing 12 bits	
Value	Decimal	Binary	Decimal	Binary
4080	4090	0111111111010	4090	111111111010
4081	4091	0111111111011	4091	111111111011
4082	4092	0111111111100	4092	111111111100
4083	4093	0111111111101	4093	111111111101
4084	4094	0111111111110	4094	111111111110
4085	4095	0111111111111	4095	111111111111
4086	4096	1000000000000	0	000000000000
4087	4097	1000000000001	1	000000000001
4088	4098	1000000000010	2	000000000010
4089	4099	1000000000011	3	000000000011
4090	4100	1000000000100	4	000000000100
4091	4101	1000000000101	5	000000000101
4092	4102	1000000000110	6	000000000110
4093	4103	1000000000111	7	000000000111
4094	4104	1000000001000	8	000000001000
4095	4105	1000000001001	9	000000001001
0	10	0000000001010	10	000000001010
1	11	0000000001011	11	000000001011
2	12	0000000001100	12	000000001100
3	13	0000000001101	13	000000001101
4	14	0000000001110	14	000000001110
5	15	0000000001111	15	000000001111

Table 5.11: Resolver Offset Application

5.2.2.4 Phase Current Controllers

The current control scheme is applied within the Phase Current Controller. Multiple copies of the Phase Current Controller are used within the FPGA program, each running in parallel, controlling an individual output phase of the SSMC, as was shown in figure 5.13. The inputs to the phase controller are:

- Input voltage states.
- Actual and reference currents.
- Current hysteresis band widths for both the single and double band controllers.
- Control scheme selection.

Within the Phase Current Controller are blocks containing the single and double band control schemes as shown in figure 5.15, which gives the graphical representation of the FPGA program within the Phase Current Controller program block. The two schemes run in parallel, with the output from just one being selectable via a multiplexer.

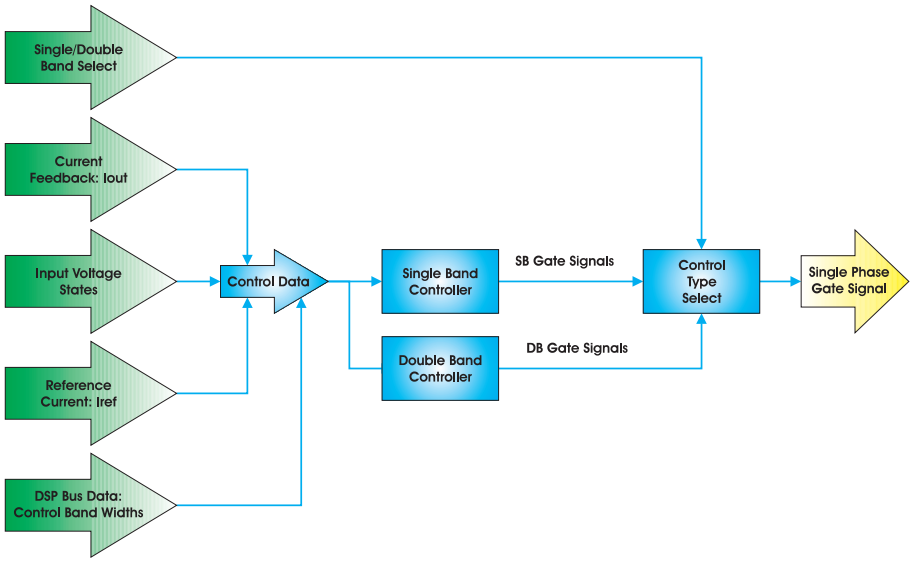

Figure 5.15: FPGA Program Structure - Phase Current Controller.

5.2.2.4.1 Single Band Current Controller The single band current controller is implemented in an identical form as used in the control simulations. One can gain a greater understanding of the way in which the specifics of the control schemes were implemented by referring back to chapter 4 and table B.1.

The first stage within the Single band controller is to subtract the actual phase current from the reference current, producing the error signal. The error is then processed by the hysteresis band block. This produces two logic signals, termed U1 and U2, which represent the error current relative to the hysteresis band, as shown in figure 5.16

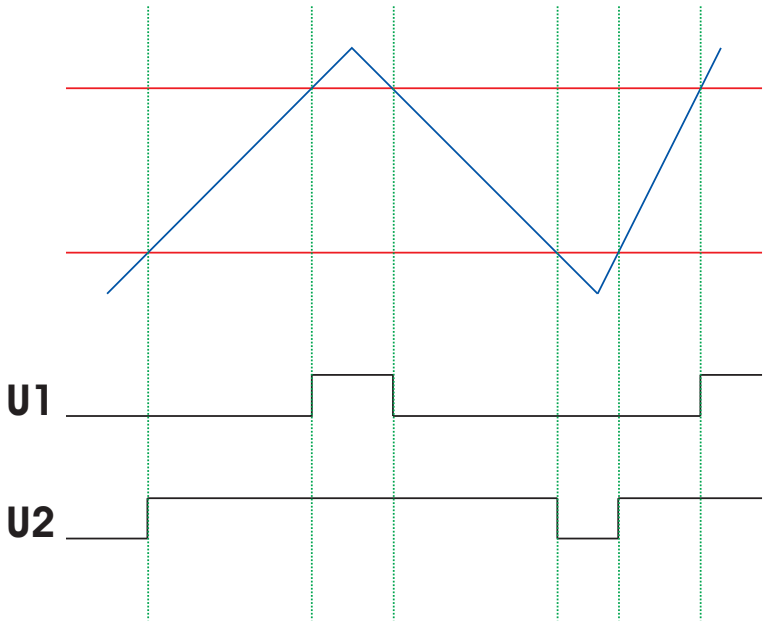

Figure 5.16: Logic Representation of Current Error With Respect to the Single Hysteresis Band.

The logic signals, U1 and U2 are taken as inputs to the Voltage Level Identifier block. This uses simple logic to determine whether the most positive or most negative of the input phases should be applied to the output, according to table 5.12.

U1	U2	Q1'	Q1
0	0	X	1
0	1	0	0
1	1	X	0
0	1	1	1

Table 5.12: Voltage Level Identifier Logic

Table 5.12 implies that when the current error is below the lower bound of the hysteresis

band, Q1 is set high, requesting the most positive available input voltage to be applied to the output. If the current error is within the hysteresis band, Q1 remains as it was previously set. When the current error becomes greater than the upper boundary of the hysteresis band, Q1 is set low, requesting the most negative voltage be applied.

Finally, Q1 is combined with the logic representation of the input voltage state, to determine the IGBT gating signals required to apply either the most positive or most negative of the input voltages. This logic arrangement is implemented using a Mealy State machine, input directly using VHDL. In this case the state machine is simply used to implement a truth table. It does not take account of previous states.

The gate drive signals then pass through a register, which uses a switching frequency limiting enable signal. The purpose of this is to restrict the switching frequency of the IGBT's. In order for the single band control scheme to operate optimally, this switching frequency limiter would not be used, and as soon as the control strategy requested a change to the state of the IGBT gate drives, it would occur. However, the relatively high supply voltage, low load inductance, and current rating of the IGBT's used in the prototypes implies that switching frequencies high enough to produce damagingly high amounts of energy dissipation within the IGBT would be likely. This would lead to very high IGBT temperatures, and thermal damage occurring. A crude form of pulse width limiter was therefore implemented within the FPGA to limit the switching frequency. Once a change of switch state has occurred, the enable signal to the frequency limiting register is taken low, and held low for approximately 0.1 ms. This implies that if a change in switch state is requested by the current control logic within this time, the new gate signals will not be passed out of the FPGA until the register enable signal has been taken high. This allows the frequency wild operation required for a hysteretic approach at lower frequencies, whilst protecting the IGBT's from excessively high switching frequencies whilst the drive is being tuned, and experiments carried out.

Finally, the gate drive signals pass through a block which adds a delay to the negative going edge of each signal. This ensures an overlap between supply phase conduction, when transferring the current from one input phase to another. The configuration of the SSMC

power circuit is such that a short circuit between input phases when multiple IGBT's are conducting is impossible, as the diode on the emitter side of the IGBT which is at the lower voltage would become reverse biased and block the flow of current. However, an open circuit when all IGBT's are reverse biased could potentially destroy the converter, as the current already flowing would create a very large potential difference across the device. The gate drive circuit used, inherently introduces a larger delay to the negative going gate drive edges than the positive going ones, however the larger, manually configurable overlap increases the drive reliability.

5.2.2.4.2 Double Band Current Controller The double band current controller is implemented in an identical form as used in the control simulations. One can gain a greater understanding of the way in which the specifics of the control schemes were implemented by referring back to chapter 4 and tables C.1, C.2 and C.3.

The Double Band control block is structured in a very similar way to the Single Band controller, and is shown in figure 5.17. Firstly the actual phase current is subtracted from the reference. The error is then processed by the hysteresis band state identifier block, to determine whether the error is below, within or above the hysteresis band. This block now performs the comparisons for both the inner and outer bands, providing four logic signals as its output, termed U1, U2, U3, U4. The relationship between the current error, the hysteresis bands, and the logic signals is as in figure 5.18.

The hysteresis band logic signals are again fed to an 'input voltage identifier'. This identifies which of the seven available supply voltage levels should be applied to the output phase. It takes account of the current error signal with respect to the double hysteresis bands, along with the direction of change of the current. The requested voltage level is encoded using three logic lines, and is output from the input voltage identifier block. The control operation of this block was developed as a state table, and is implemented using a Mealy State Machine, the VHDL code for which is given in appendix D. This is a true state machine as it takes account of the previous output state, as under normal operation, the scheme should step through the available voltage levels until a change in direction of

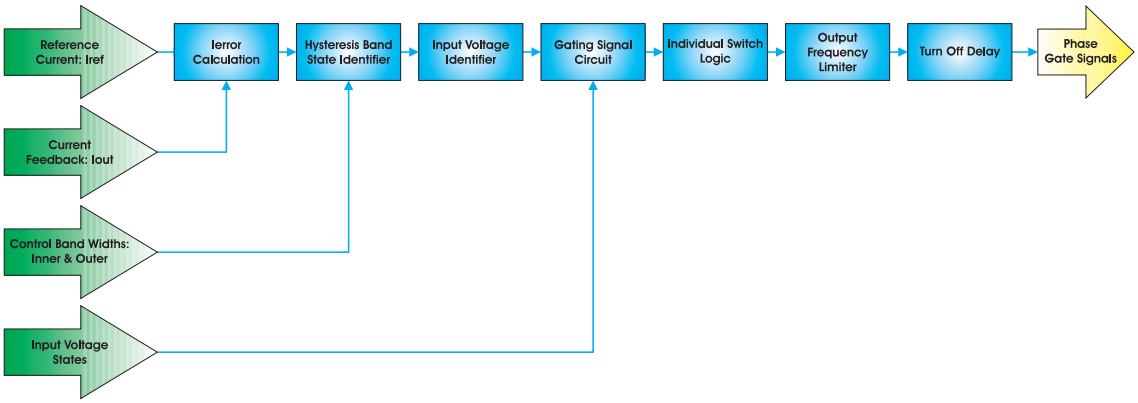

Figure 5.17: FPGA Program Structure - Double Band Hysteresis Current Controller.

change of current occurs.

Registers are used to clock the data into the input voltage identifier. The clock frequency used with these registers is carefully selected to ensure that the control scheme does not step through the voltage levels at too high a rate. If this were the case, the controller would step through the levels before the newly applied voltage had any effect on the current. The frequency used here is clearly dependant upon the supply voltage and phase inductance.

Following the voltage level identifier is the ‘gating signal circuit’. This takes as its inputs the three logic signals representing the required voltage level, along with the six signals representing the input voltage state. Again a Mealy State Machine is used to implement the logic of the control operation, although no previous state data is used. The outputs of the gating signal circuit are four logic signals representing the phase to phase voltage that should be applied, and the direction in which it should be applied.

A further Mealy State Machine termed the ‘individual switch logic’ block then follows, implementing a simple truth table, which converts the four signals representing the required line to line voltage into the IGBT gate drive signals.

The same switching frequency limiter and off transition delay blocks then follow as are used with the single band controller, as given in section 5.2.2.4.1.

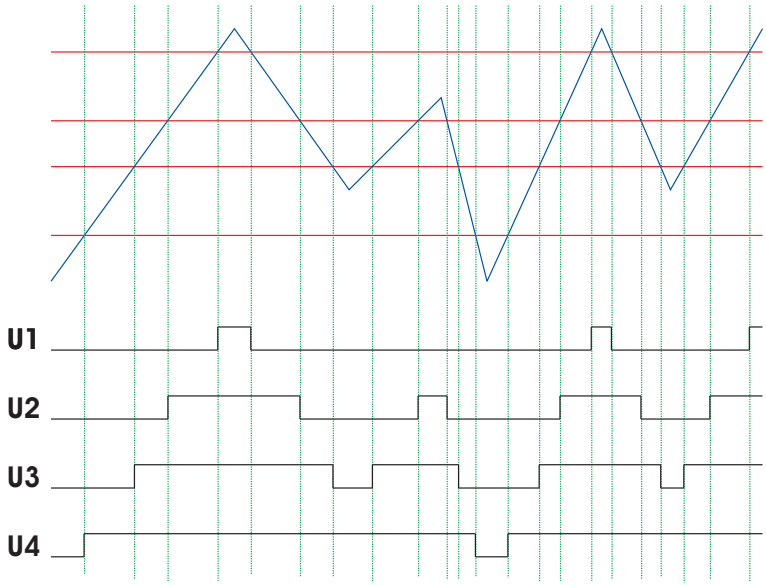

Figure 5.18: Logic Representation of Current Error With Respect to the Double Hysteresis Bands.

5.2.2.5 Trip Handling

Just two basic trip events have been implemented in the prototype SSMC controller.

- Over current trip on output current.
- Over voltage trip on clamp capacitor.

These were the two which were considered to be critical to the safe operation of the drive in the test environment.

The clamp over voltage monitoring is implemented slightly differently on the three and five phase versions of the SSMC. In the three phase version, a voltage transducer is used to obtain a measurement of the clamp voltage, which is then supplied to one of the spare A/Ds. The measured value is compared with a preset trip value within the FPGA, and the trip event is triggered if the clamp voltage is too high. The trip level is set such that if

activated and the drive has to shut down, the peak energy stored within the motor inductance can be dumped into the clamp without its voltage exceeding the predetermined safe level.

In the five phase version of the SSMC, the Clamp Voltage Monitoring Circuit is used, as described in section 5.1.4.1. The logic signal produced by this circuit is input to the FPGA via one of the digital input lines.

The over current trip is implemented in two ways. The first is using hardware comparators in an analogue circuit included on the FPGA board. This is described in section 5.1.1. The logic signal generated by the hardware comparators is fed into the FPGA via one of the digital inputs. This second method uses software comparators, operating on the binary data collected from the A/D converter chips. The software comparators were necessary when implementing the five phase SSMC, as only three of the output current measurements are connected to hardware comparators. In the five phase converter, all five currents are monitored by the software comparators, with a single trip signal being generated if one of the five phase currents rises above a predetermined level.

The trip signals from the three sources are combined using 'or' gates, producing a single trip drive signal. This is supplied to a high speed trip block, which intercepts the gate drive signals after the current controller blocks. Inside the high speed trip block is a multiplexer, which takes the trip signal as its selection input. The multiplexer is configured such that when the trip signal is low, the multiplexer allows through the gate drive signals generated by the current controller block. When the trip signal goes high, the multiplexer selects gate drive signals from a predefined trip table, disabling the operation of the converter in a safe way.

5.2.2.6 Data Extraction

As described in section 5.1.1, the FPGA PCB was originally designed to be integrated with a Texas instruments DSP, with access to the DSP's address and data bus being available in the FPGA chip. This allows for bi-directional data transfer between the DSP and FPGA. The controller for the SSMC was designed and implemented entirely within the FPGA

software, however the connection to the DSP was used, and allowed extraction of control data from the FPGA current controllers. It was only possible to sample the data at a relatively low rate, compared with the clock frequency of the FPGA and control program, so a complete low level diagnostic check of the SSMC controller was not possible using this method. It did however allow for the verification of the overall current band controller operation.

Along with the lines necessary for operation of the control program, an additional control data extraction bus was output from each control block. As the bus passed through the hierarchy of blocks, additional signals were attached to different bits of the bus, before the individual buses were attached to inputs of a 32 way, 32 bit multiplexer. The five lines of the DSP address bus were used as the selection lines of the multiplexer, with the output of the multiplexer being connected to a data bus interface block, designed by Lee Empringham. This allowed 1024 data bits to be sampled and captured by the DSP, at a sampling frequency of approximately 40kHz.

A Host program was then used on an accompanying PC, allowing communication with the DSP. Using the Host, data could be captured using the DSP as requested by the operator, and then uploaded to the host PC, before being analysed using Matlab.

The DSP program and PC Host program were modified versions of those developed for the TIMES [49] project.

5.3 Summary

This chapter has presented the practical implementation of the Single Sided Matrix Converter, using control provided by an FPGA. The converter hardware has been described, including the design of a six layer PCB used to provide the power planes necessary for reliable operation of the matrix converter.

The design procedures and methods used for implementation of the drive controller within

the FPGA were then presented, followed by a description of the two current control scheme blocks. Trips were included within the controller such that the drive was protected under fault conditions, and finally a description of the DSP and Host interface were given, which although not required for the controller operation, were invaluable as program development tools. These also allowed the extraction of large amounts of controller operation data, which is presented in chapter 6.

Chapter 6

Prototype Practical Results

A very wide range of data is available from each of the experimental Single Sided Matrix Converters, for many different operating conditions. Presented in this chapter are a selection of test results from both SSMCs, for different operating conditions, which aim to demonstrate the operation of both the single and double band control schemes, as well as explaining the effects of the motor on the shape of the currents drawn. The results don't necessarily show optimum or efficient operation of the motors, and are all taken without the implementation of a speed or torque control loop.

6.1 Basic Control Data Required for Both Control Schemes

The operation of both the single and double band control schemes is dependant upon a small amount of knowledge of the input voltage states. Figure 6.1 shows actual voltage transducer readings for the three input phase voltages, sampled by the FPGA and captured using the attached DSP, with the converter outputs disabled. One should note that the transducers are configured to measure line to line voltages. Along with the sampled voltages are the 6 logic signals derived from them. Just the lower three logic signals are used by the single

band scheme, whilst all six are used by the double band scheme.

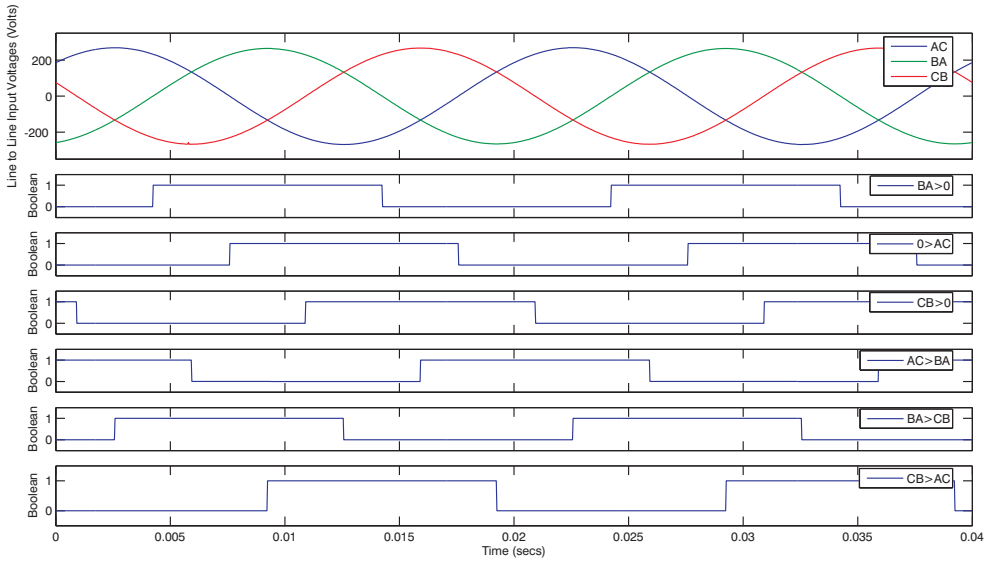

Figure 6.1: Supply Phase to Phase Voltages with Supply State Logic.

Presented in figure 6.2 is the raw sampled resolver data, along with the filtered data, before and after application of the offset value. As explained in section 5.2.2.3 it appears that the majority of this noise is of a digital nature, due to occasional bit shifting, and most likely occurs on the serial data link lead between the resolver interface chip, and the FPGA PCB. It is very likely that improvements could be made to remove the source of this noise. Figure 6.2 does however show the effectiveness of the filter developed within the FPGA as described in section 5.2.2.3.

Visible in figure 6.2b is the offset resolver position data. This corrects for the random orientation of both the resolver stator and rotor during construction, such that a value of zero corresponds with the condition of a rotor pole being fully aligned with a stator pole of phase U.

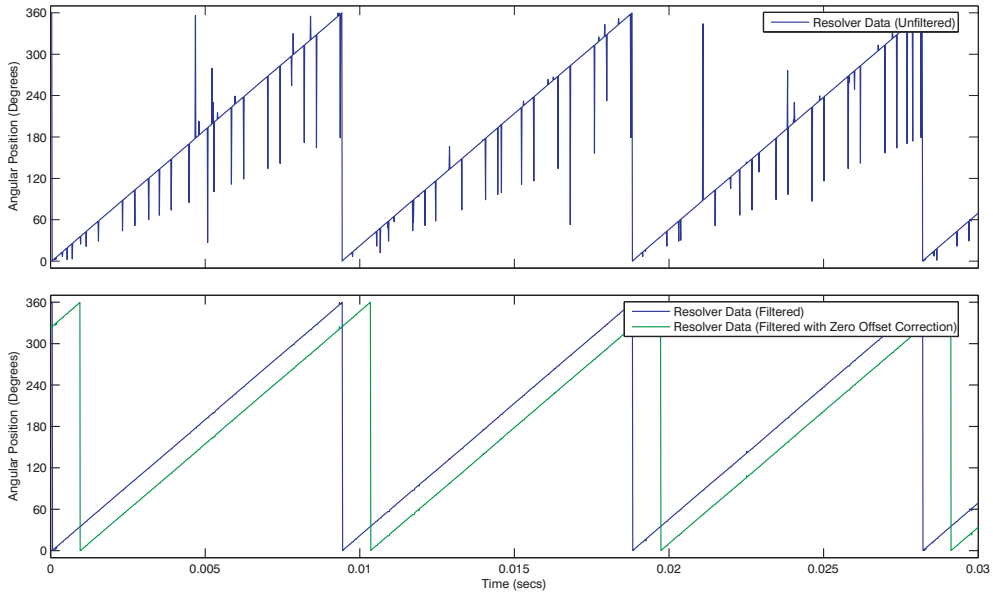

Figure 6.2: Resolver Data: a,Unfiltered. b,Filtered. c,Zero Offset Corrected.

6.2 Three Phase SSMC driven Switched Reluctance Motor

The majority of the results presented are taken from the 3 phase SSMC, driving a Switched Reluctance motor. The motor used at this stage is a 12/8 3 phase switched reluctance motor, with an approximate power output of 12kW. It has the characteristics as given in table 6.1. Note that with a 12/8 switched reluctance motor, each pole spans 15 mechanical degrees, compared with 30 for the 6/4 machine used in the simulations. This motor was kindly loaned to the Electrical & Electronic Engineering Department by Switched Reluctance Drives Ltd, a subsidiary of Emerson Electric Co of St Louis, Missouri, to enable the testing of the operation of the SSMC.

Phase Resistance (ohms)	0.72
Aligned Inductance (mH)	60
Unaligned Inductance (mH)	12

Table 6.1: Experimental Switched Reluctance Motor Characteristics - Final testing Motor

In order to show the operation of the current control schemes, it was necessary to supply the motor phases with a significantly high current. However, such a level of current is sufficient to accelerate the motor to a speed where the back EMF generated inherently limits the current level within the phase, to the point that the current does not reach the demand value, and the control scheme is not seen to operate. It is therefore important that results for both low speed and high speed operation are presented. In order to observe the operation of the current control scheme at low speed, a load was applied to the motor, using a DC commutator machine. The switched reluctance motor and loading rig can be seen in figure 6.3. Unfortunately the amplitude of this load is unknown, as although a load cell is fitted to the loading rig used in order to measure torque produced, the torque produced by the switched reluctance motor was outside of the range of the load cell. The results for two speeds as given in table 6.2, along with the phase excitation parameters used are presented in the following sections. Results are presented using both the single and double band control schemes.

Results are also presented for a 30 amp demand controlled with the double band method, in order to show operation of the converter at the maximum average current at which it was designed to operate. The parameters used are also given in table 6.2.

Current Limit (A)	Switching Angles (degrees)		Speed (rpm)
	Turn On	Turn Off	
24	16.8	0	290
30	27	10.5	4000
30	16.8	0	310

Table 6.2: Switched Reluctance Motor Experimental Data

A simple switching frequency limiter is used within the FPGA, as described in sections 5.2.2.4.1 and 5.2.2.4.2, in order to protect the IGBT's. In order to allow clear control data to be captured from the FPGA using the DSP, which only samples the FPGA at a low rate, the switching frequency of the converter for both the single band and double band control schemes is set lower than the 10 KHz at which the converter is designed to operate. When in single band control mode, the switching frequency limit is set to approximately 6.5 kHz, whilst in double band mode, the maximum switching frequency is set to approximately 3

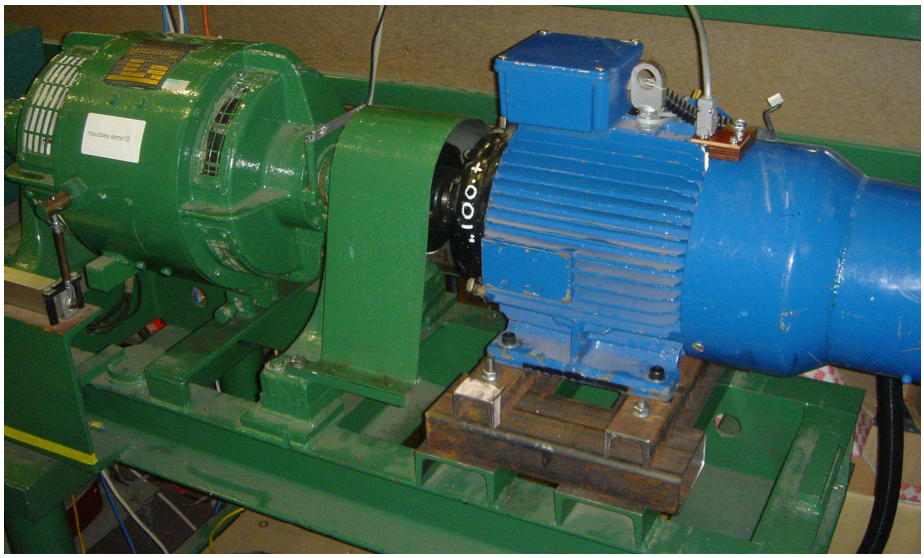

Figure 6.3: Switched Reluctance Motor & Loading Rig.

KHz. For both control modes, the data presented here has been acquired with the hysteresis bands set as narrow as is practical in order to see reasonable operation of the two control schemes. This difference in switching frequency does however have the effect of making the single band method appear capable of containing the current within a band as narrow as that used with the double band method.

The switched reluctance motor test results where acquired using a variable voltage, variable frequency power supply to power the SSMC, with the output voltage set to 110V rms line to line at 50 Hz. This is capable of supplying the currents required by the converter, without causing significant distortion to the voltage sin waves. However, as the SSMC draws large high frequency harmonics from the supply, 60μF of capacitance were connected between the supply phases at the converter terminals, as might be used in a final lineside filter. Without the use of these capacitors, the supply voltage is distorted such that spikes are produced, and the input clamp voltage rises to the trip level. This level has been set relatively low at 340V, so as to offer maximum protection to the power electronics, and avoid stress damage.

Ideally a Fourier analysis would be performed on the input currents, as a comparison with

those performed on the simulation results, in order to determine the types of harmonics present in the supply current. Unfortunately however, the use of the lineside capacitors makes a Fourier analysis misleading, as many of the higher frequency components drawn by the SSMC are supplied by the capacitors. They also completely mask the amplitude of the fundamental current drawn when using either of the control methods. For this reason Fourier analyses have not been performed on the supply current waveforms. This is something that should be carried out using a slightly modified circuit arrangement, in future work.

6.2.1 Single Band Current Control - Low Speed

Presented in figure 6.4 are the three phase output currents, along with the angular rotor position taken from the captured resolver data. The eight current pulses required by each phase during one revolution are clear.

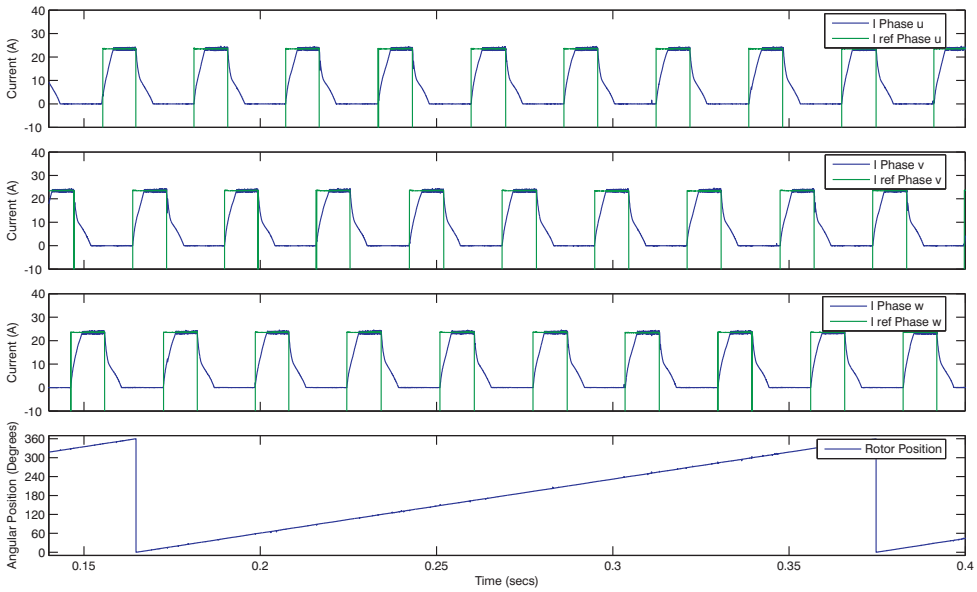

Figure 6.4: SB Controlled Output Phase Currents with Rotor Position.

Figure 6.5 presents the same data as 6.4 but over a shorter period. Also clear here is the

effect of the phase back EMF, which causes a slow decrease in current after each pulse.

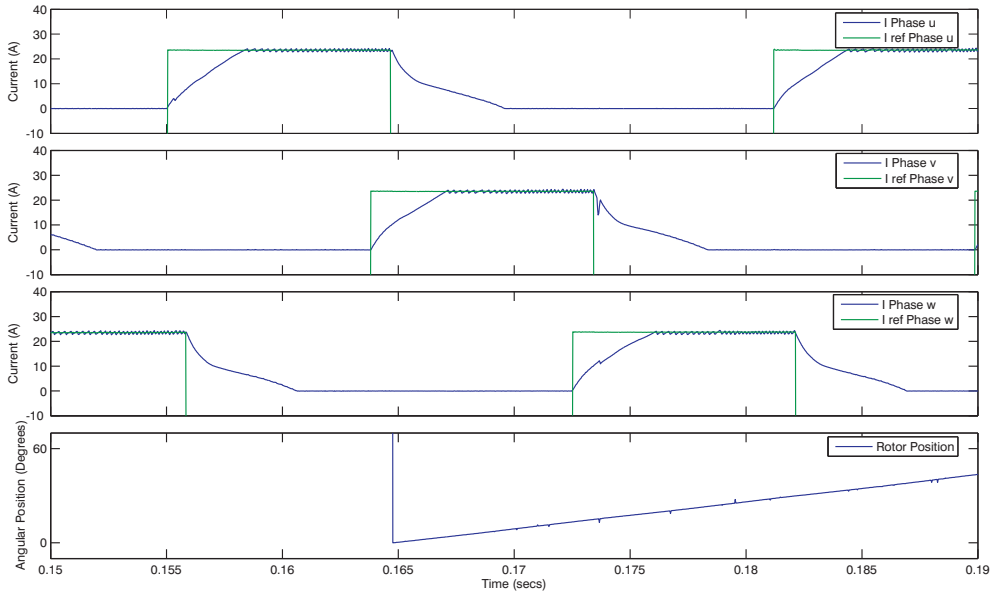

Figure 6.5: SB Controlled Output Phase Currents with Rotor Position (Zoomed in).

Presented in figure 6.6 is a single current pulse applied to phase U, along with the current error signal and the single hysteresis band. It is clear here that the single band control scheme correctly controls the current within the hysteresis band. An interesting point to note is the increase in switching frequency over the period of the pulse. This is a direct contrast to the decrease in switching frequency apparent in the simulations, shown specifically in figure 4.51. This very clearly shows the limitation of the linear model, which neglects the magnetic saturation of the steel that occurs when high currents are applied to the phases of the switched reluctance motor. By considering figure 4.5 which shows the flux linkage against current curves for both the minimum and maximum flux linkage conditions, one can see that as the rotor turns and the saturation of the steel increases, the maximum flux linkage condition tends towards a horizontal line, the incremental inductance actually decreases over the period where the poles come into alignment. Other than this however, the control behaves as predicted by the simulations.

Figure 6.7a gives the supply line to neutral voltages, and from these, the maximum and minimum available supply voltages have been reconstructed in figure 6.7b. A single phase

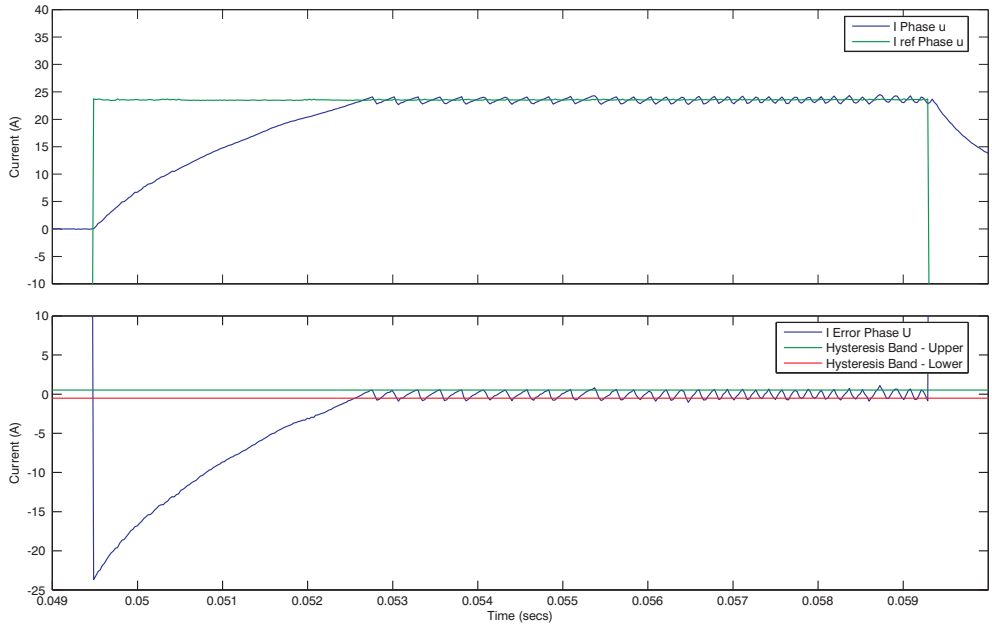

Figure 6.6: SB Control, Phase U: a,Current Output. b,Current Error with Hysteresis Bands.

output voltage of the SSMC can be seen in figure 6.7c, and can be compared with the current, again shown in figure 6.7d. One can clearly see the combined effect of the phase inductance, and the induced back EMF in the slow rate of rise and decay of current with the phase. Also very apparent here is the effect of the high harmonic content of the input currents on the supply phase voltages.

Presented in figure 6.8 is oscilloscope data acquired for an output phase pulse comparable with that shown in figure 6.7. These two sets of data were taken at the same time, during the same test run, however the data captures were not synchronised. Two interesting observations can be made here which cannot be made from the data available from the DSP. Firstly, the input current is shown in figure 6.8b. A significant 50 Hz component is visible, induced by the lineside capacitors connected at the SSMC terminals. As would be expected, this leads the supply voltage waveform. Large harmonics are however very clearly present throughout the cycle, as each of the output phases conducts.

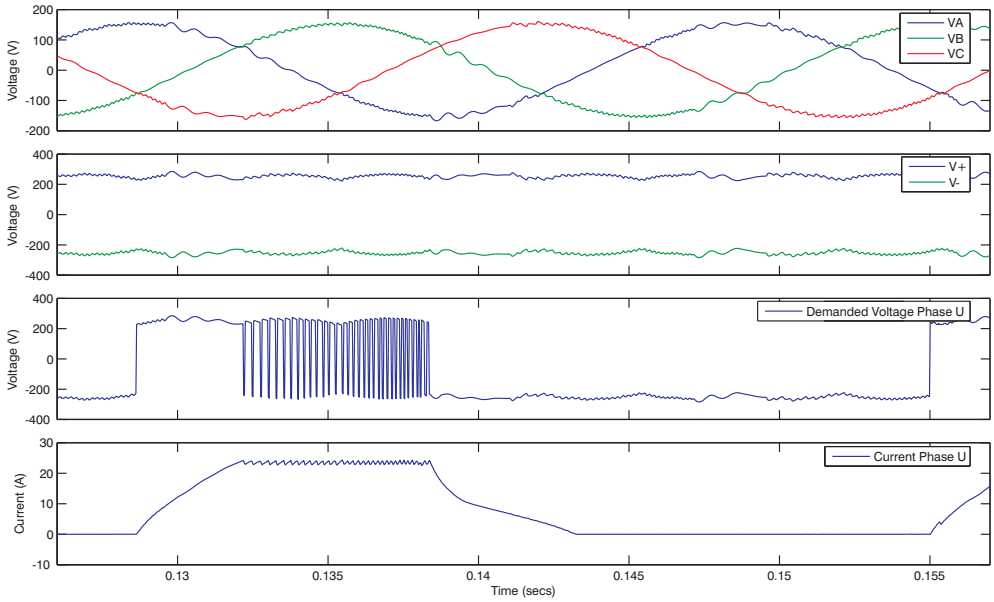

Figure 6.7: DSP Data: a,Supply Line to Neutral Voltage. b,Voltage Available at Converter Output. c,Voltage Demanded at Converter Output (Phase U). d,Current Output (Phase U).

The second observation to be made is concerning the output voltage waveforms. Comparing figure 6.8c with figure 6.7c, one can see two discrepancies between the output voltage applied by the control scheme, and the voltage measured across the terminals of the SSMC, when the current demand is zero. Firstly, the maximum negative voltage, V- in figure 6.7b is only seen across the output terminals of the SSMC when a positive current is flowing. Once the current reaches zero, the diodes of the two unidirectional switches though which the current was flowing become reverse biased, stopping the voltage applied by the IGBTs being seen across the output terminals. The moment any current tried to flow through the phase, the diodes would again become forward biased, and V- would be applied across the phase, forcing the current to zero. The second discrepancy seen is the spikes of voltage which occur from the moment that the current reaches zero, and continue until the next output pulse begins. This is due to capacitive coupling between the motor phases, and although they are of a significant amplitude, the negative voltage applied to the phase by the SSMC prevents them from inducing any current flow.

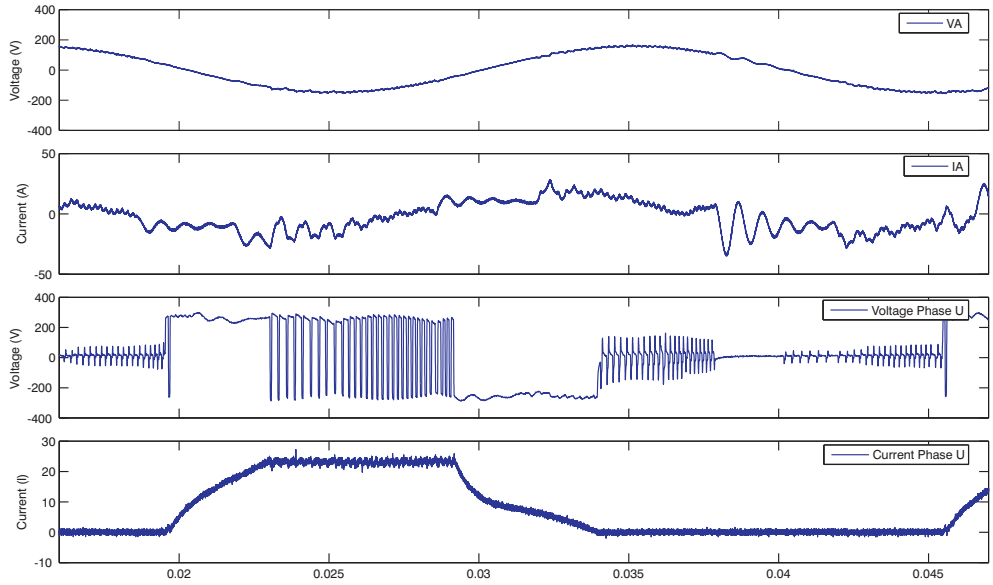

Figure 6.8: Scope Data: a,Supply Line to Neutral Voltage (Phase A). b, Supply Current (Phase A). c,Voltage Applied at Converter Output (Phase U). d,Current Output (Phase U).

6.2.2 Double Band Current Control - Low Speed

Presented here are results in an identical format to those presented for control by the single band scheme, allowing for comparisons to be made. Firstly, in figure 6.9 are the three output phase currents, along with the captured resolver data for a complete revolution of the rotor.

Figure 6.10 gives the three output phase currents over a shorter period. By comparing this with figure 6.5, one can see that both control schemes are equally capable of producing the current pulse, which has a very similar shape in both cases.

Figure 6.11 presents the current error signal, along with the voltage level applied. Whilst the low switching frequency limit imposed by the controller affects the quality of the output current waveform, it allows for a clear explanation and verification of the behaviour of the double band controller, as is given in the following bullet points.

- The current demand rises to 24A, the current error becomes negative, dropping

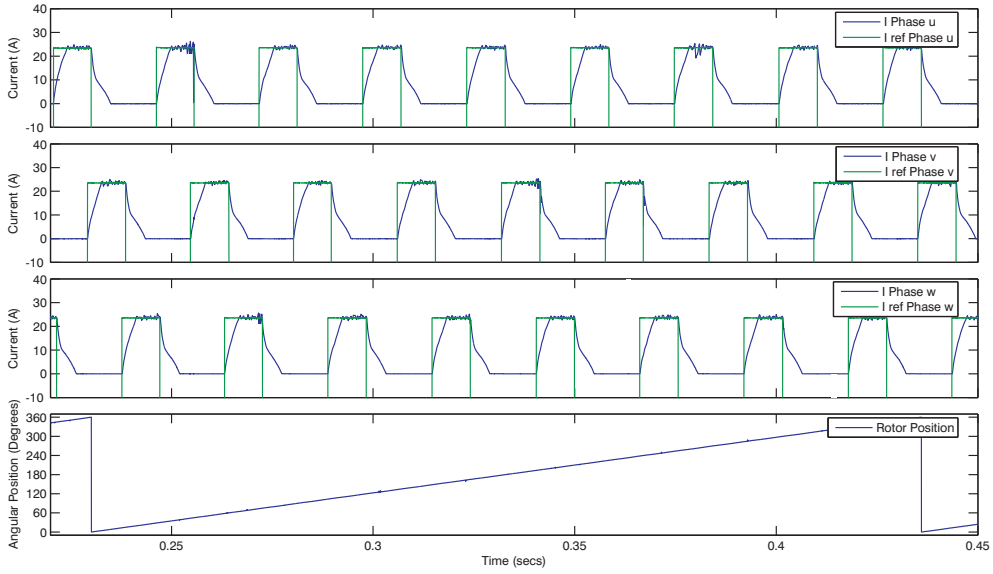

Figure 6.9: DB Controlled Output Phase Currents with Rotor Position.

outside the outer hysteresis band. The instant this occurs, level V+3 voltage is applied across the output.

- The current begins to increase. When the error reaches the upper level of the inner hysteresis band, the applied voltage level begins stepping down until a change in direction of current is observed. In this case, dropping to level V+2 is sufficient.

- The error reaches the lower level of the inner hysteresis band, and the applied voltage level steps up to level V+3.

- The error reaches the upper level of the inner hysteresis band, and the applied voltage level steps up to level V+2.

- The current begins to drop, but then starts to increase again. This is due to the non-constant voltage associated with each voltage level. Upon the error reaching the upper level of the inner band, the voltage level is again stepped down, until the current is seen to fall. Dropping to level V+1 is sufficient, but causes a fast drop in current.

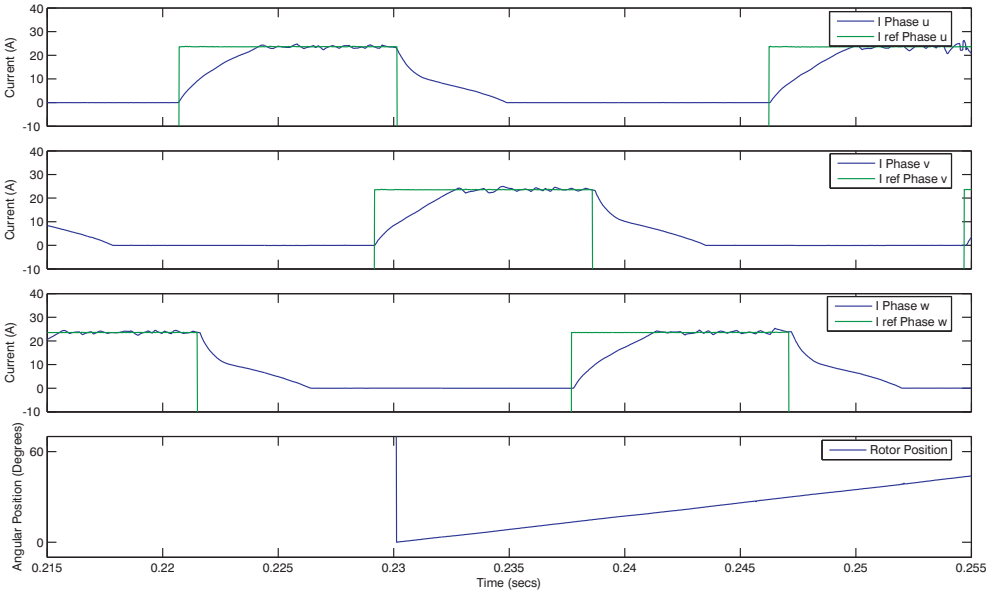

Figure 6.10: DB Controlled Output Phase Currents with Rotor Position (Zoomed in).

- The error reaches the lower level of the inner band, and level V+2 is applied. As the voltage associated with V+2 is now lower, it is seen to be applied for longer.
- Level V+2's voltage is now increasing, and a series of steps between V+1 and V+2 follow. The changing period of each being due to the changing voltages associated with the voltage levels.
- There comes a point where voltage level V+1's voltage is great enough to cause an increase in current. Note that level V+1's voltage is of a triangular nature, with a minimum voltage of zero. Once its amplitude becomes too great to cause a decrease in current, level V0 is applied for a couple of short pulses, when a drop in current is required.
- As level V+1's voltage begins to decrease again, its amplitude is such that its application to the load causes a decrease in current, and the levels are now stepped between V+1 and V+2.
- The end of the demand pulse is reached, and upon passing the upper level of the outer hysteresis band, voltage level V-3 is applied. This causes a fast decrease in current,

until the polarity of the back EMF is reversed, and opposes the applied voltage. The current continues to decrease until reaching zero amps, but decreases at a slower rate.

This explains the operation of the double band control, and verifies its correct operation.

If the switching frequency limit were increased to the 10kHz for which the converter was designed, it would be made clear that a tighter hysteresis band could be used with the double band controller than with the single band controller, as was shown in the simulations, producing a cleaner output current waveform.

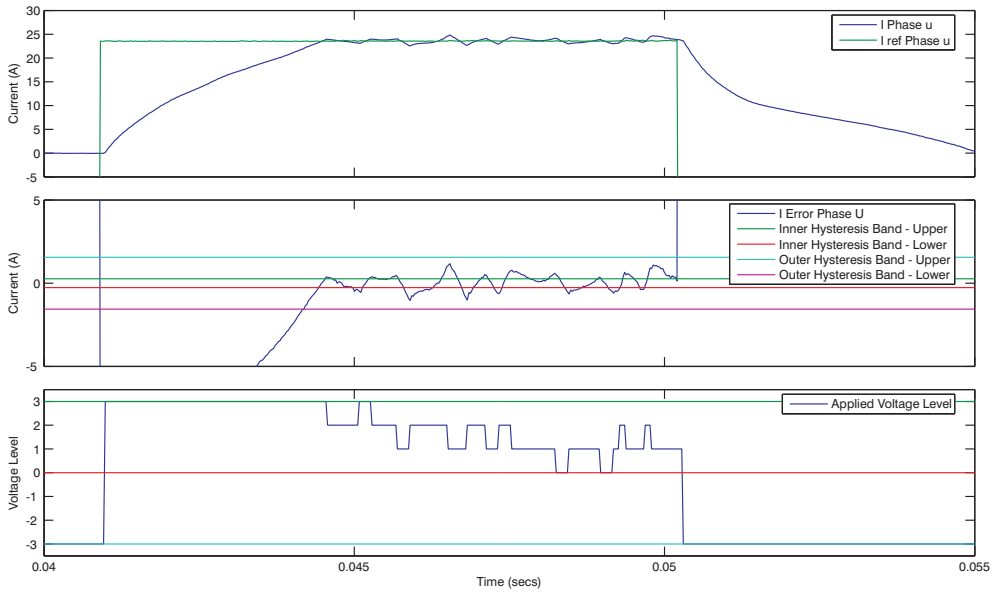

Figure 6.11: DB Control, Phase U: a,Current Output. b,Current Error with Hysteresis Bands. c,Applied Voltage Level.

Figures 6.12 and 6.13 present the comparison of DSP and oscilloscope data, for comparable current pulses. As with the single band method, it is clear that the large harmonics present in the supply current cause significant distortion of the supply voltage. The lower double band switching frequency limit used compared with that of the single band method worsens the supply current significantly however, implying that lower frequency components will be present in the supply current.

Also visible in figure 6.13c are the voltage spikes induced across the converter terminals, due to the capacitive coupling between phases of the motor. The spikes are however significantly smaller here compared with the single band method, as the double band method applies lower voltage changes across the phase winding.

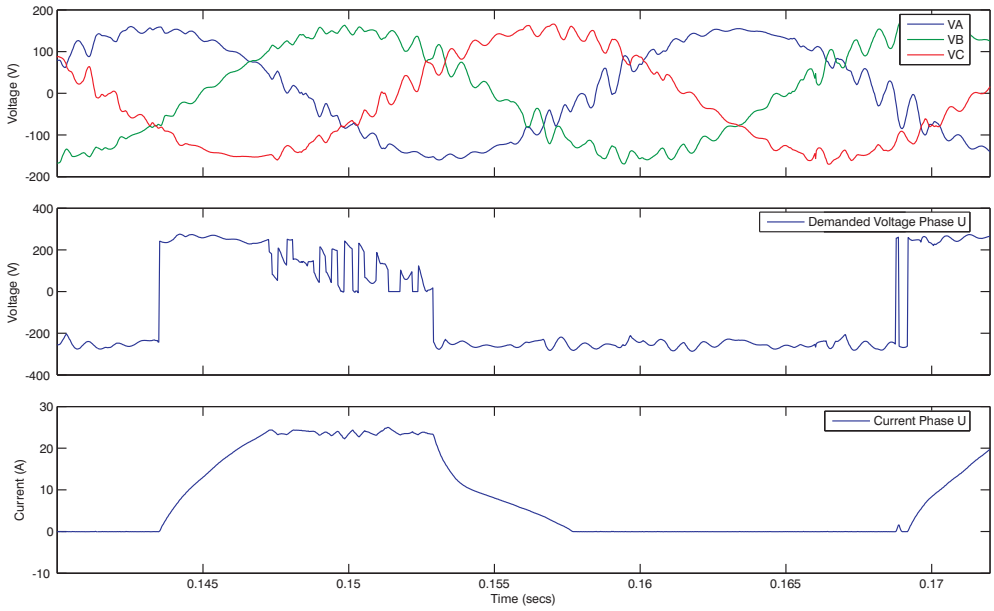

Figure 6.12: DSP Data: a,Supply Line to Neutral Voltages. b,Voltage Available at Converter Output. c,Voltage Demanded at Converter Output (Phase U). d,Current Output (Phase U).

Presented in figure 6.14 is single phase output voltage and current data for the double band scheme controlling a current of 30amps. Note that this is applied with the motor stationary. A single current pulse can be seen in figure 6.15. These figures show operation in the same way as described previously in this section, and are included simply to show operation of the converter at the current at which it was designed to be capable of operating.

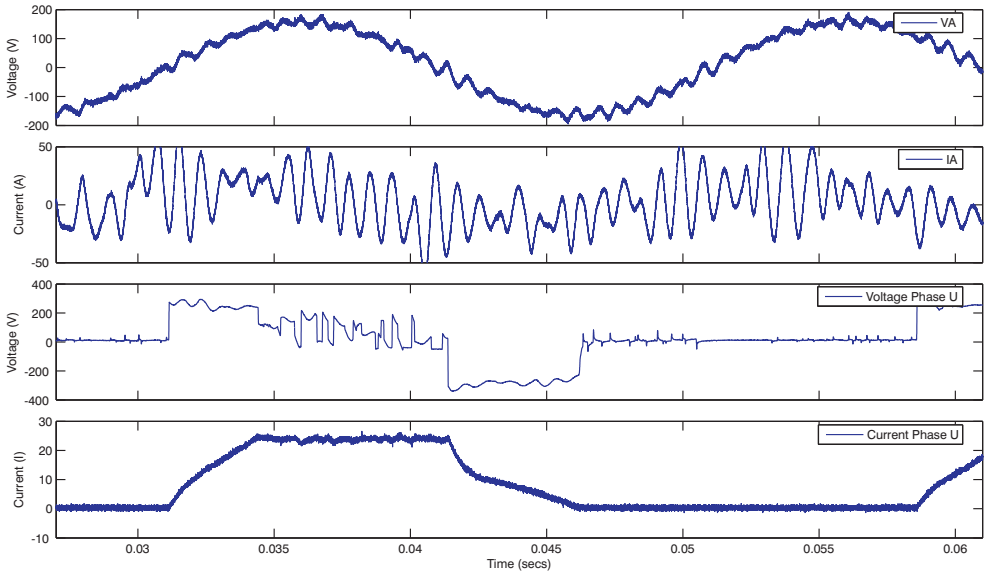

Figure 6.13: Scope Data: a,Supply Line to Neutral Voltage (Phase A). b, Supply Current (Phase A). c,Voltage Applied at Converter Output (Phase U). d,Current Output (Phase U).

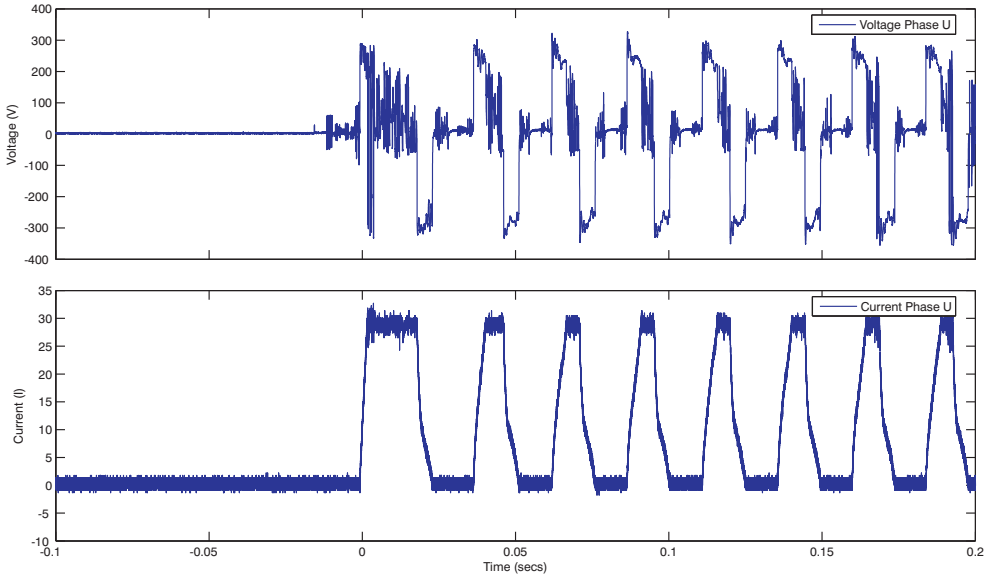

Figure 6.14: Scope Data - 30amp Output Pulse (Phase U): a,Voltage Applied at Converter Output. b,Current Output.

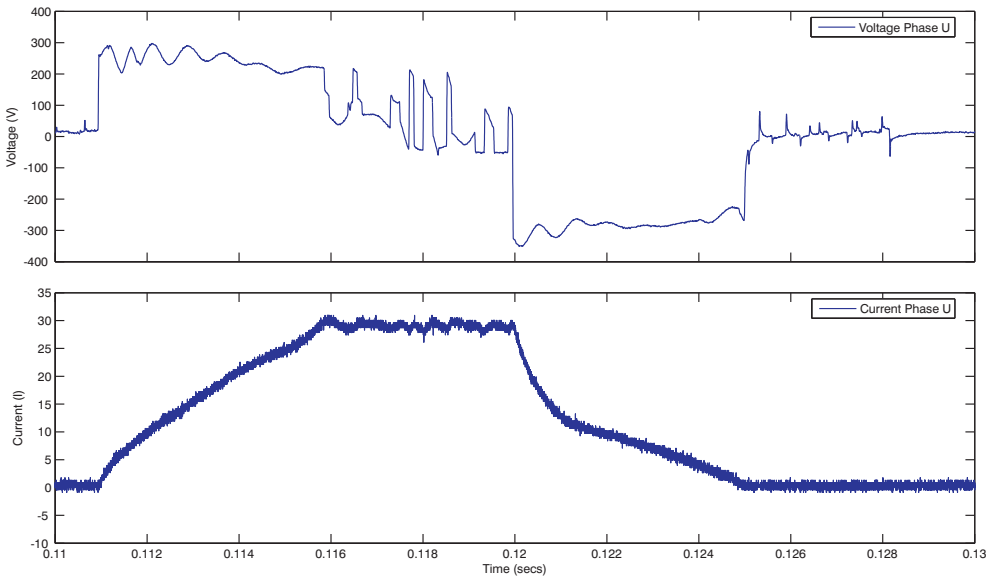

Figure 6.15: Scope Data - 30amp Output Pulse (Phase U): a,Voltage Applied at Converter Output. b,Current Output.

6.2.3 Single & Double Band Current Control - High Speed

Presented in figures 6.16 and 6.17 are single phase output voltage and current waveforms for the single band and double band control schemes respectively, driving the motor at approximately 4000 rpm, using the parameters given in table 6.2. These are typical high speed switched reluctance motor current waveforms, and it is clear in each case, no hysteretic switching occurs. The motor phase current is naturally limited by the back EMF induced by the higher speed. The varying peak current amplitudes are due to the variations in maximum voltage available from the three phase supply, as can be seen by observing each of the voltage waveforms.

The interesting observation to make here is that as no hysteretic switching occurs, and therefore no control over the output current shape, no control would ever be possible over the quality of the input currents. Figure 6.18 is as figure 6.16, however over a longer period, and includes a line to line input voltage and single phase current. There is unfortunately a large amount of sampling noise on the supply current waveform, however it is clear that the smaller current pulses drawn at high speed are mostly absorbed by the lineside capacitance used here.

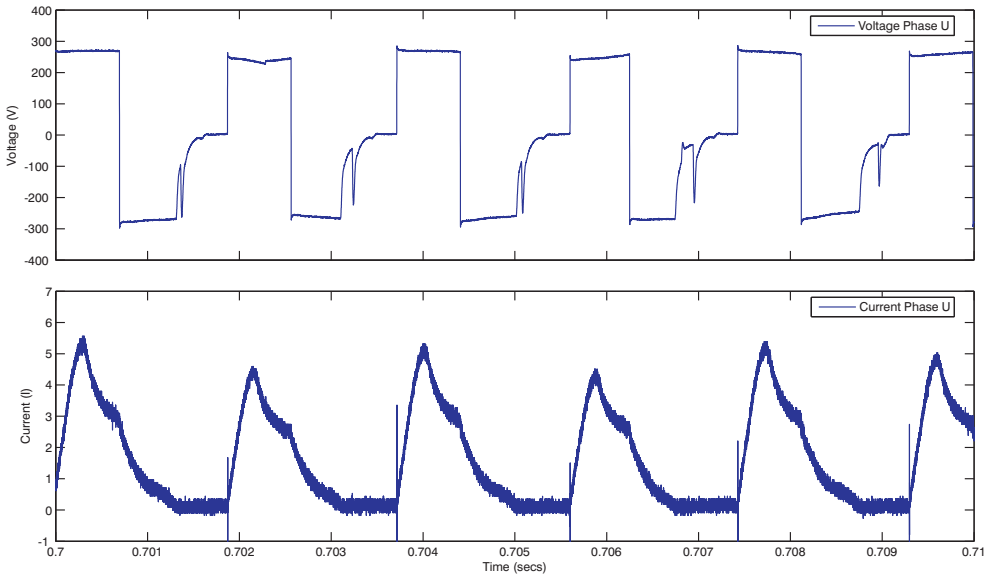

Figure 6.16: Scope Data - SB Control (Phase U): a,Voltage Applied at Converter Output. b,Current Output.

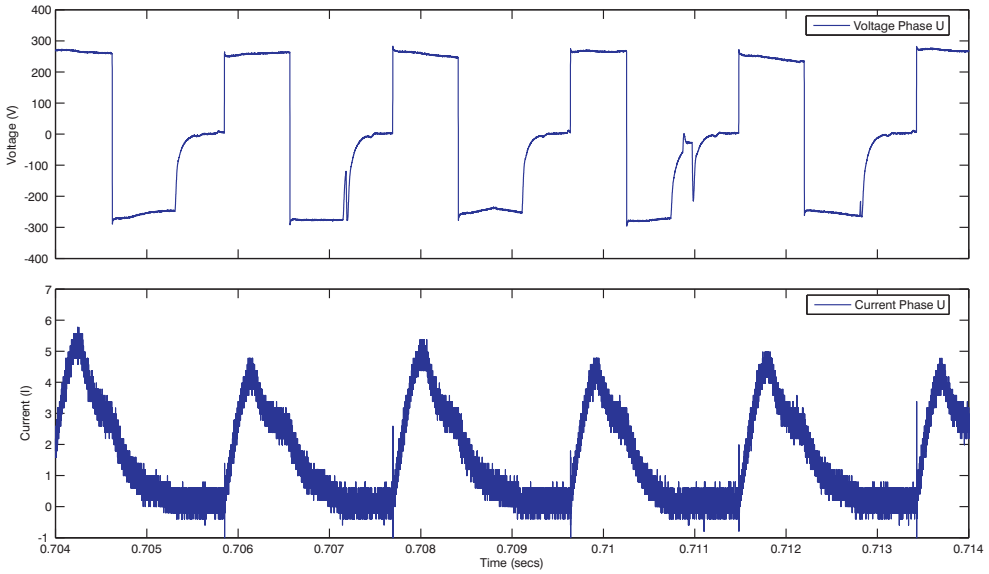

Figure 6.17: Scope Data - DB Control (Phase U): a,Voltage Applied at Converter Output. b,Current Output.

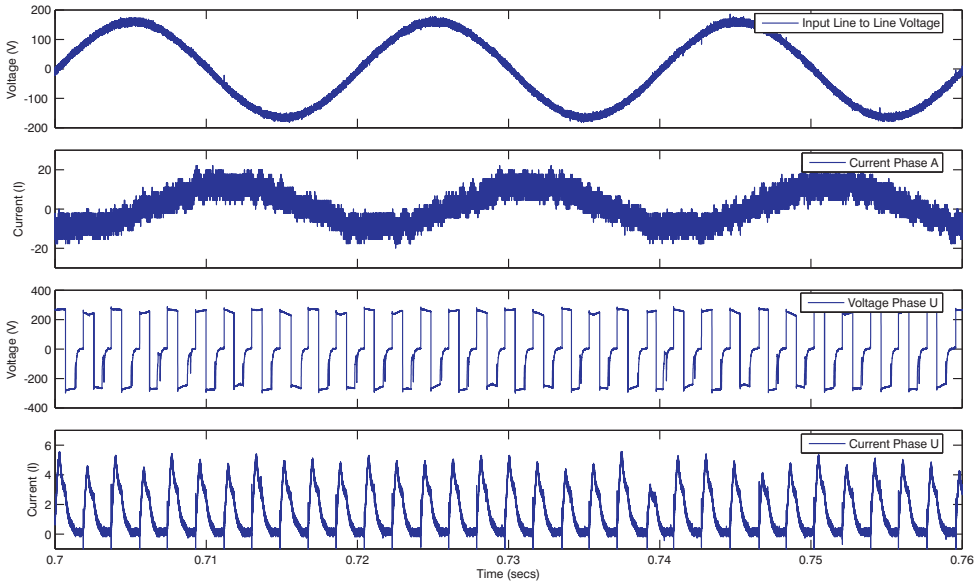

Figure 6.18: Scope Data - DB Control (Phase U): a,Voltage Applied at Converter Output. b,Current Output.

6.3 Five Phase SSMC driven Trapezoidal PMDC Motor (SATOW Project)

A small selection of results are presented for operation of the SATOW trapezoidal PMDC motor, driven from a five phase SSMC. Both single band and double band results are presented, and highlight the problems encountered with the low phase inductance of this motor.

The single band controlled five phase output currents are presented in figure 6.19, along with the resolver position signal. One can see here the way in which the phase pulses overlap as required.

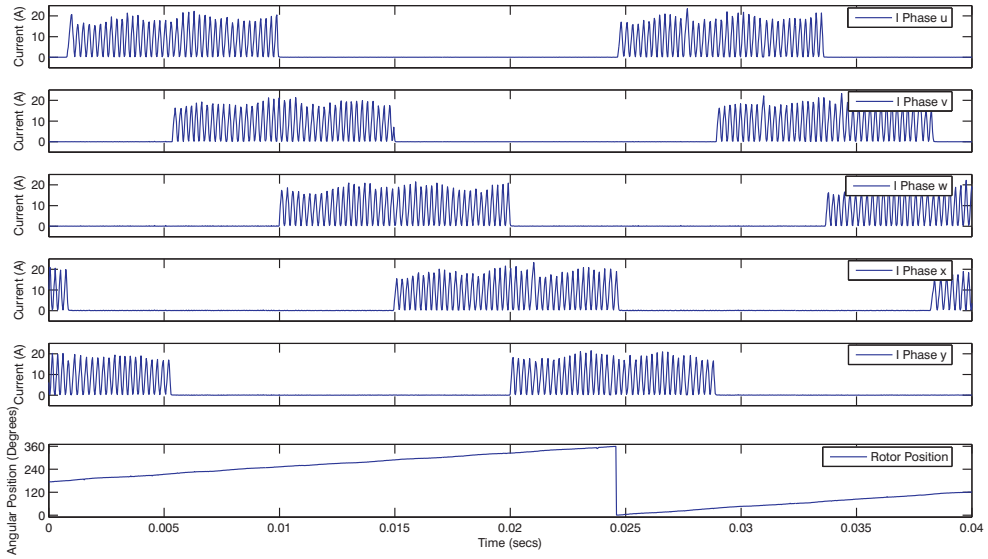

Figure 6.19: SB Controlled Output Phase Currents with Rotor Position.

Figure 6.20 presents the current error signal and hysteresis band, along with the applied output phase voltage. The very large current ripple can be seen, and the fact that the low phase inductance coupled with the limited switching frequency makes it impossible for the converter to control the error signal to be within the single hysteresis band. An increase in the switching frequency to the designed value would help here, however the ripple will still be substantial. Further work is required here.

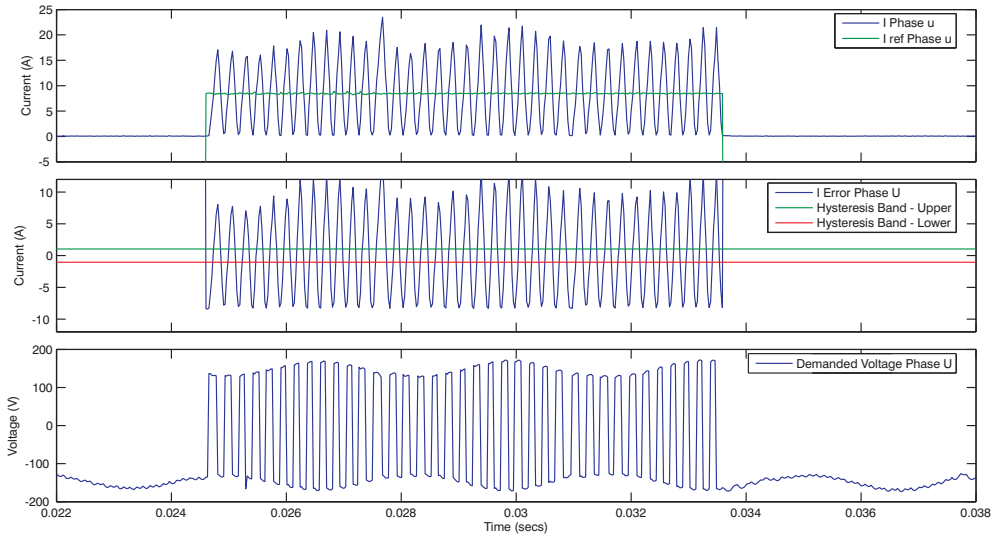

Figure 6.20: SB Control (Phase U): a,Current Output. b,Current Error with Hysteresis Bands. c,Voltage Demanded at Converter Output.

Figure 6.21 presents results obtained for operation of the double band control scheme. Again, the overlapping 5 phase output currents can be seen.

Presented in figure 6.22 are the error signal, along with the double hysteresis bands, and the applied output voltage, and voltage levels. One can see that the double band control scheme is more successful at controlling the current, and for 60-70% of the time maintains it within the outer band. The outer band is however set to approximately 16A which is larger than would be desired.

One can clearly see in figures 6.22c & d, the way in which the double band control steps through the available voltage levels when the error is maintained within the outer band, in this case stepping from level V-3 to V+2 on several occasions.

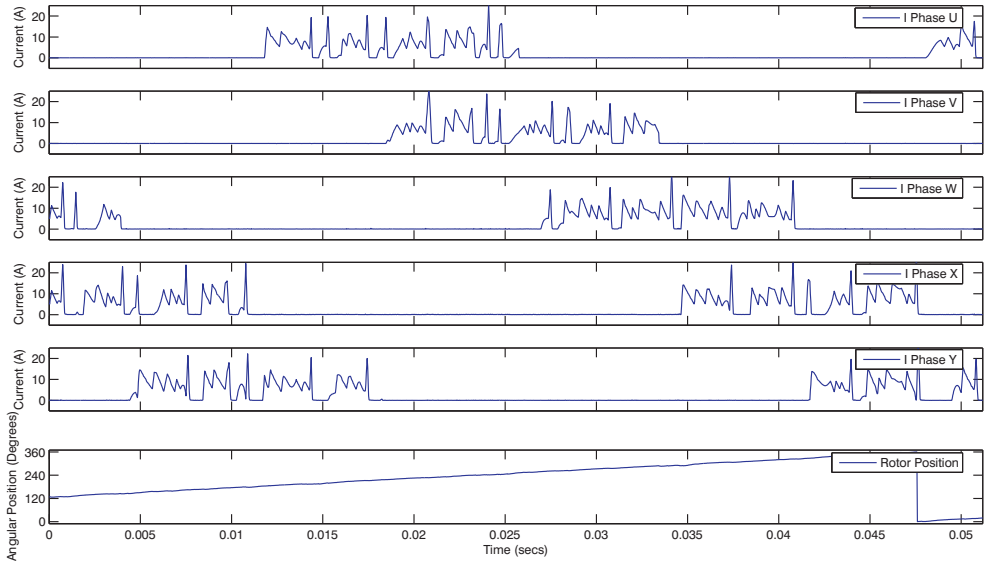

Figure 6.21: DB Controlled Output Phase Currents with Rotor Position.

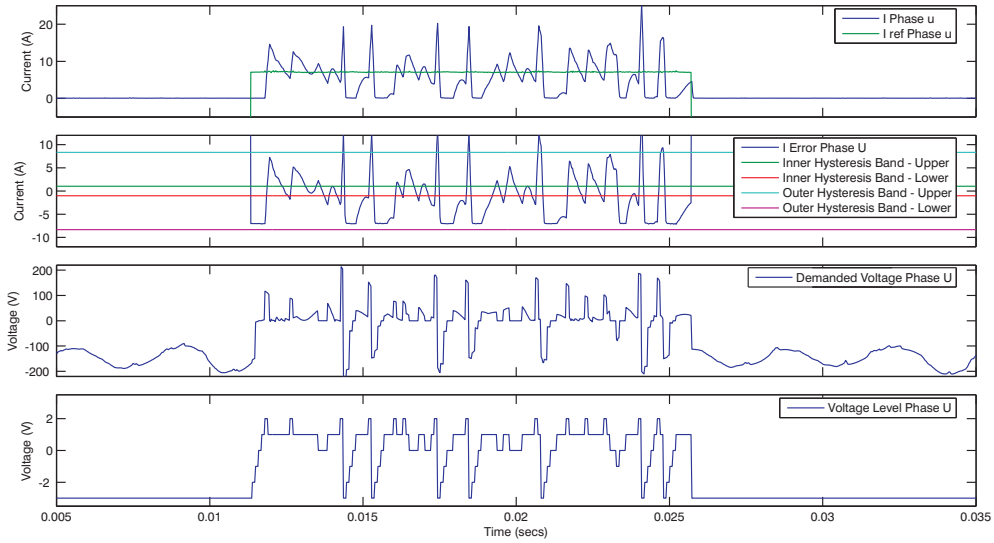

Figure 6.22: DB Control (Phase U): a,Current Output. b,Current Error with Hysteresis Bands. c,Voltage Demanded at Converter Output. d,Voltage Level Applied at Converter Output.

6.4 Summary

This chapter has presented results for operation of the practical single sided matrix converter, driving both the switched reluctance motor, and the trapezoidal PMDC machine. It has been shown that the converter and control schemes operate as proposed and in a reliable manner, and that commutation occurs safely when significant current pulses of 30A are drawn.

In the switched reluctance motor, the effects of back EMF and changing motor phase inductance on the currents drawn were clearly visible, as were the large input current harmonics at the reduced switching frequency limits for which the results were obtained. Unfortunately direct comparisons of input current quality for the two schemes could not be accurately made as the switching frequency limits used in the two cases were different. Also, the way in which the oscilloscope data had been acquired made Fourier analysis of the input currents inappropriate. The results were however promising in showing the ability of the converter in driving the switched reluctance motor.

The current waveforms for operation of the switched reluctance motor at high speed were shown to be the same for either control scheme, as the effect of back EMF inherently limits the phase currents far below the demand value. This has the implication that no development of the control scheme can be used to improve the input current waveforms for high speed operation, without reducing the power output of the motor, as the most positive supply voltage is always needed by each phase during a current pulse at high speed.

Finally a limited number of practical waveforms for the SSMC driven trapezoidal PMDC motor were presented. The lower phase inductance in this motor is clearly a problem when the single band control scheme is used. Better results were seen with the double band controller, although the hysteresis band width required was still excessively large. Much better results should however be seen when the switching frequency is increased to the design value.

The great value of the DSP and Host program were evident in making controller data

available for the purposes of FPGA software development and debugging, and in acquiring controller operation waveforms.

Chapter 7

Conclusion

This thesis has introduced in chapter 1 a novel form of AC input direct energy converter drive, termed a single sided matrix converter (SSMC). The objective was to develop a simple drive control strategy with failsafe commutation and which did not require the use of a digital signal processor (DSP). This approach was adopted to ensure that the drive could be used easily in aerospace actuation systems without requiring approval for a specific DSP. The work has been published in 3 IEEE conference papers listed in appendix A. The drive is only able to supply a pulsed current output and can supply a switched reluctance motor and a brushless DC machine.

The potential of the SSMC with brushless DC drives was recognised early in this PhD study, and a second student Xiaoyan Huang started work under the SATOW project on designing a special five phase brushless DC machine, to compliment this project.

Chapter 2 explained how the SSMC fits within a family of power electronic converters. An overview of the different conversions commonly performed was given, followed by a more in depth look at some of the active direct power converter topologies. An in depth review of matrix converter operation, and solutions to the implementation problems were provided. The space vector control method was covered, as this was a potential way in which the SSMC might be controlled.

A detailed explanation of the operation of the SSMC was given in chapter 3, including descriptions of the hysteretic control schemes proposed. The novel double band control scheme was introduced, which had the potential to reduce the switching frequency of the power devices and provide a more continuous line current. An evaluation of the suitability of both the switched reluctance and trapezoidal PMDC motors for use with the SSMC was also provided here, with an explanation of the expected effects of the motors on the output currents.

Simulation of the converter and drive system in chapter 4 showed that operation is effective for (inductive) switched reluctance and brushless DC machine loads. Several practical problems became clear, the first and most obvious being the non-sinusoidal input currents, which would require significant filtering. The Fourier analyses performed made it apparent that the double band control drew a lesser harmonic content from the supply than the single band control. Secondly, it became very clear that low load inductance combined with the restricted switching frequency would be a problem, as in the case of the trapezoidal PMDC motor designed under SATOW. Use of the double band control scheme, and its ability to apply smaller differential voltages across the load should improve the situation greatly.

In order to enable the effective control of the SSMC without the use of a DSP, an FPGA was employed. The programming of this chip and development of the converter was described in chapter 5. It was shown that both the single band and double band control schemes can be implemented using an FPGA, and that although time consuming to develop programs for, the FPGA provides an incredibly flexible and reliable platform on which to develop such control. Some of the methods used to enable the implementation of this type of controller on an FPGA were also discussed. The design procedure for the development of the matrix PCB was covered, indicating the factors to be taken into account when designing PCBs for large voltages and currents. The two SSMCs were assembled and communication lines and circuits tested at every stage, to ensure correct and safe operation of the completed converters.

Results for the operation of the SSMC with inductive, SR and trapezoidal PMDC machine loads are presented in chapter 6. It is shown that the drive has the following advantages:

- Tight control of pulsed output currents is possible where the load inductance is sufficiently high. This was seen with operation of the switched reluctance motor. The pulsed output requirement makes a fixed switching frequency converter less suitable, as the best attempt must be made to meet large instantaneous demand changes. This requires instantaneous commutation as is available here.

- Whilst only positive output currents can be generated, the pulse timing can be adjusted such that negative motor torque is produced, implying regenerative breaking and therefore bi-directional power flow through the converter. Although tests were not specifically performed to verify this, it is evident in the long tails of current seen to conduct after pole alignment in the SR motor.

- It has been shown that commutation between input phases occurs in a safe, reliable manner.

- If all gate drive signals are removed, the drive fails in a safe manner, dumping all energy stored in the inductive motor elements into the clamp, and protecting the converter IGBTs from over-voltage damage.

- The SSMC has been shown to be capable of driving two motors - both the switched reluctance motor and the trapezoidal PMDC machine.

- The novel double band control scheme has been shown to be advantageous in reducing switching frequencies, making the converter more suitable for use with lower inductance loads.

- The double band control scheme has been shown to distribute the current drawn from the supply throughout more of the supply voltage cycle, reducing the large current pulsations drawn during the lower amplitude parts of the input sine wave.

- The large number of IGBTs used makes failure of a single device less significant to the continued operation of the drive. Although not implemented here, the double band control scheme could be developed to detect device failure, and restrict the possible output phase vectors accordingly, ensuring continued operation of the drive [45].

- The drive presented offers complete isolation between phases, both at the converter and motor stages. this implies that a fault on one phase will have no effect on the operation or reliability of the remaining functional phases.

The practical results obtained also indicated the following negative side of the single sided matrix converter:

- No attempt is made to control the input current quality. As was clearly shown, the input currents are inherently non-sinusoidal and may need significant filtering if supply side harmonics are to be minimised.
- The IGBT switching frequency is not fixed, but must nonetheless be restricted in order to control switching losses and minimise heat produced. This implies that the supply voltage, load inductance and hysteresis band widths must be matched to ensure reasonable performance of the control schemes. If this is not the case, as was seen with the SATOW results, poor control of the output currents is a problem.
- At high speeds, no controller actions are seen with the SR motor, and maximum available supply voltage is required throughout the pulse duration in order to maintain the speed. There is therefore little scope in terms of control for improvement of the input current quality at high speed operation.
- A larger number of power devices are required to supply a three phase SR motor than would be required to supply a normal AC motor from a conventional matrix converter.

7.1 Further work

Although much has been achieved in terms of applying the proposed control schemes to a practical converter, there is scope for improvement and development of the drive as given in the following:

- Alternative control algorithms could be considered as a way of improving the supply currents drawn by the converter. One proposal is to restrict the voltage levels available at each commutation such that an improvement in input current quality can be made. This may be at the expense of the output current quality, but would likely offer an acceptable compromise.

- Consideration should be given to the design of a suitable input filter. Additional Fourier analyses of the actual input currents drawn should be performed and an investigation made into the feasibility of the filter required in order to improve the quality of the input currents to a suitable degree.

- The switching frequency limiter implemented to date restricts times between all commutations. A more intelligent version should be developed which recognises the phase commutations taking place and only restricts the time between commutations accordingly. Most importantly, the final commutation at the end of a current pulse, at the point where the most negative voltage should be applied, should be made exempt from the restrictions of the switching frequency limiter.

- An active clamp should be added to the SSMC in order to remove the only electrolytic capacitors used in the development version of the converter, making the drive entirely suitable for aerospace actuator applications.

Appendix A

Papers Published

Goodman A, Bradley K J, Wheeler P W ,"Evaluation of the Single Sided Matrix Converter Driven Switched Reluctance Motor", *IEEE Industry Applications, Thirty Ninth IAS Annual Meeting*, Seattle, October 2004.

Huang X, Bradley K J, Goodman A, Gerada C, Wheeler W, Clare J, Whitley C , "Fault-Tolerant Brushless DC Motor Drive for Electro-Hydrostatic Actuation System in Aerospace Application", *IEEE Industry Applications, Forty-First IAS Annual Meeting*, Tampa, October 2006.

Huang X, Bradley K J, Goodman A, Gerada C, Wheeler W, Clare J, Whitley C , "Fault-Tolerant Analysis of Multi-Phase Single Sided Matrix Converter for Brushless DC Drives", *IEEE International Symposium on Industrial Electronics*, Vigo, June 2007.

Appendix B

Single Band Controller Logic

Table B.1: Single Band Controller - Gating Signal Logic.

Inputs									Outputs					
A1	B1	C1	A2	B2	C2	Q1	Q2		SAa	SAb	SBa	SBb	SCa	SCb
1	0	0	0	1	0	1	0		1	0	0	0	1	0
1	0	0	0	0	1	1	0		1	0	0	0	0	1
0	1	0	0	0	1	1	0		0	1	0	0	0	1
0	1	0	1	0	0	1	0		0	1	0	1	0	0
0	0	1	1	0	0	1	0		0	0	1	1	0	0
0	0	1	0	1	0	1	0		0	0	1	0	1	0
1	0	0	0	1	0	0	1		0	1	0	1	0	0
1	0	0	0	0	1	0	1		0	0	1	1	0	0
0	1	0	0	0	1	0	1		0	0	1	0	1	0
0	1	0	1	0	0	0	1		1	0	0	0	1	0
0	0	1	1	0	0	0	1		1	0	0	0	0	1
0	0	1	0	1	0	0	1		0	1	0	0	0	1

Appendix C

Double Band Controller Logic

Table C.1: Double Band Controller - Voltage Level Identifier Logic.

Inputs										Outputs		
U1	U2	U3	U4	D		V1'	V2'	V3'		V1	V2	V3
0	0	0	0	0		0	0	0		0	0	0
0	0	0	0	0		0	0	1		0	0	0
0	0	0	0	0		0	1	0		0	0	0
0	0	0	0	0		0	1	1		0	0	0
0	0	0	0	0		1	0	0		0	0	0
0	0	0	0	0		1	0	1		0	0	0
0	0	0	0	0		1	1	0		0	0	0
0	0	0	0	0		1	1	1		0	0	0
0	0	0	0	1		0	0	0		0	0	0
0	0	0	0	1		0	0	1		0	0	0
0	0	0	0	1		0	1	0		0	0	0
0	0	0	0	1		0	1	1		0	0	0
0	0	0	0	1		1	0	0		0	0	0
0	0	0	0	1		1	0	1		0	0	0
0	0	0	0	1		1	1	0		0	0	0
0	0	0	0	1		1	1	1		0	0	0
0	0	0	1	0		0	0	0		0	0	0
0	0	0	1	0		0	0	1		0	0	0
0	0	0	1	0		0	1	0		0	1	1

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Table C.1 – Continued

U1	U2	U3	U4	D		V1'	V2'	V3'		V1	V2	V3
0	0	0	1	0		0	1	1		0	0	1
0	0	0	1	0		1	0	0		1	1	0
0	0	0	1	0		1	0	1		1	0	0
0	0	0	1	0		1	1	0		0	1	0
0	0	0	1	0		1	1	1		0	1	0
0	0	0	1	1		0	0	0		0	0	0
0	0	0	1	1		0	0	1		0	0	1
0	0	0	1	1		0	1	0		0	1	0
0	0	0	1	1		0	1	1		0	1	1
0	0	0	1	1		1	0	0		1	0	0
0	0	0	1	1		1	0	1		1	0	1
0	0	0	1	1		1	1	0		1	1	0
0	0	0	1	1		1	1	1		0	1	0
0	0	1	0	0		0	0	0		0	1	0
0	0	1	0	0		0	0	1		0	1	0
0	0	1	0	0		0	1	0		0	1	0
0	0	1	0	0		0	1	1		0	1	0
0	0	1	0	0		1	0	0		0	1	0
0	0	1	0	0		1	0	1		0	1	0
0	0	1	0	0		1	1	0		0	1	0
0	0	1	0	0		1	1	1		0	1	0
0	0	1	0	1		0	0	0		0	1	0
0	0	1	0	1		0	0	1		0	1	0
0	0	1	0	1		0	1	0		0	1	0
0	0	1	0	1		0	1	1		0	1	0
0	0	1	0	1		1	0	0		0	1	0
0	0	1	0	1		1	0	1		0	1	0
0	0	1	0	1		1	1	0		0	1	0
0	0	1	0	1		1	1	1		0	1	0
0	0	1	1	0		0	0	0		0	0	0
0	0	1	1	0		0	0	1		0	0	1
0	0	1	1	0		0	1	0		0	1	0
0	0	1	1	0		0	1	1		0	1	1
0	0	1	1	0		1	0	0		1	0	0
0	0	1	1	0		1	0	1		1	0	1
0	0	1	1	0		1	1	0		1	1	0
0	0	1	1	0		1	1	1		0	1	0
0	0	1	1	1		0	0	0		0	0	0
0	0	1	1	1		0	0	1		0	0	1
0	0	1	1	1		0	1	0		0	1	0

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Table C.1 – Continued

U1	U2	U3	U4	D		V1'	V2'	V3'		V1	V2	V3
0	0	1	1	1		0	1	1		0	1	1
0	0	1	1	1		1	0	0		1	0	0
0	0	1	1	1		1	0	1		1	0	1
0	0	1	1	1		1	1	0		1	1	0
0	0	1	1	1		1	1	1		0	1	0
0	1	0	0	0		0	0	0		0	1	0
0	1	0	0	0		0	0	1		0	1	0
0	1	0	0	0		0	1	0		0	1	0
0	1	0	0	0		0	1	1		0	1	0
0	1	0	0	0		1	0	0		0	1	0
0	1	0	0	0		1	0	1		0	1	0
0	1	0	0	0		1	1	0		0	1	0
0	1	0	0	0		1	1	1		0	1	0
0	1	0	0	1		0	0	0		0	1	0
0	1	0	0	1		0	0	1		0	1	0
0	1	0	0	1		0	1	0		0	1	0
0	1	0	0	1		0	1	1		0	1	0
0	1	0	0	1		1	0	0		0	1	0
0	1	0	0	1		1	0	1		0	1	0
0	1	0	0	1		1	1	0		0	1	0
0	1	0	0	1		1	1	1		0	1	0
0	1	0	1	0		0	0	0		0	1	0
0	1	0	1	0		0	0	1		0	1	0
0	1	0	1	0		0	1	0		0	1	0
0	1	0	1	0		0	1	1		0	1	0
0	1	0	1	0		1	0	0		0	1	0
0	1	0	1	0		1	0	1		0	1	0
0	1	0	1	0		1	1	0		0	1	0
0	1	0	1	0		1	1	1		0	1	0
0	1	0	1	1		0	0	0		0	1	0
0	1	0	1	1		0	0	1		0	1	0
0	1	0	1	1		0	1	0		0	1	0
0	1	0	1	1		0	1	1		0	1	0
0	1	0	1	1		1	0	0		0	1	0
0	1	0	1	1		1	0	1		0	1	0
0	1	0	1	1		1	1	0		0	1	0
0	1	0	1	1		1	1	1		0	1	0
0	1	1	0	0		0	0	0		0	1	0
0	1	1	0	0		0	0	1		0	1	0
0	1	1	0	0		0	1	0		0	1	0

Continued on Next Page...

Table C.1 – Continued

U1	U2	U3	U4	D		V1'	V2'	V3'		V1	V2	V3
0	1	1	0	0		0	1	1		0	1	0
0	1	1	0	0		1	0	0		0	1	0
0	1	1	0	0		1	0	1		0	1	0
0	1	1	0	0		1	1	0		0	1	0
0	1	1	0	0		1	1	1		0	1	0
0	1	1	0	1		0	0	0		0	1	0
0	1	1	0	1		0	0	1		0	1	0
0	1	1	0	1		0	1	0		0	1	0
0	1	1	0	1		0	1	1		0	1	0
0	1	1	0	1		1	0	0		0	1	0
0	1	1	0	1		1	0	1		0	1	0
0	1	1	0	1		1	1	0		0	1	0
0	1	1	0	1		1	1	1		0	1	0
0	1	1	1	0		0	0	0		0	0	0
0	1	1	1	0		0	0	1		0	0	1
0	1	1	1	0		0	1	0		0	1	0
0	1	1	1	0		0	1	1		0	1	1
0	1	1	1	0		1	0	0		1	0	0
0	1	1	1	0		1	0	1		1	0	1
0	1	1	1	0		1	1	0		1	1	0
0	1	1	1	0		1	1	1		0	1	0
0	1	1	1	1		0	0	0		0	0	1
0	1	1	1	1		0	0	1		0	1	1
0	1	1	1	1		0	1	0		1	1	0
0	1	1	1	1		0	1	1		0	1	0
0	1	1	1	1		1	0	0		1	0	1
0	1	1	1	1		1	0	1		1	0	1
0	1	1	1	1		1	1	0		1	0	0
0	1	1	1	1		1	1	1		0	1	0
1	0	0	0	0		0	0	0		0	1	0
1	0	0	0	0		0	0	1		0	1	0
1	0	0	0	0		0	1	0		0	1	0
1	0	0	0	0		0	1	1		0	1	0
1	0	0	0	0		1	0	0		0	1	0
1	0	0	0	0		1	0	1		0	1	0
1	0	0	0	0		1	1	0		0	1	0
1	0	0	0	0		1	1	1		0	1	0
1	0	0	0	1		0	0	0		0	1	0
1	0	0	0	1		0	0	1		0	1	0
1	0	0	0	1		0	1	0		0	1	0

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Table C.1 – Continued

U1	U2	U3	U4	D		V1'	V2'	V3'		V1	V2	V3
1	0	0	0	1		0	1	1		0	1	0
1	0	0	0	1		1	0	0		0	1	0
1	0	0	0	1		1	0	1		0	1	0
1	0	0	0	1		1	1	0		0	1	0
1	0	0	0	1		1	1	1		0	1	0
1	0	0	1	0		0	0	0		0	1	0
1	0	0	1	0		0	0	1		0	1	0
1	0	0	1	0		0	1	0		0	1	0
1	0	0	1	0		0	1	1		0	1	0
1	0	0	1	0		1	0	0		0	1	0
1	0	0	1	0		1	0	1		0	1	0
1	0	0	1	0		1	1	0		0	1	0
1	0	0	1	0		1	1	1		0	1	0
1	0	0	1	1		0	0	0		0	1	0
1	0	0	1	1		0	0	1		0	1	0
1	0	0	1	1		0	1	0		0	1	0
1	0	0	1	1		0	1	1		0	1	0
1	0	0	1	1		1	0	0		0	1	0
1	0	0	1	1		1	0	1		0	1	0
1	0	0	1	1		1	1	0		0	1	0
1	0	0	1	1		1	1	1		0	1	0
1	0	1	0	0		0	0	0		0	1	0
1	0	1	0	0		0	0	1		0	1	0
1	0	1	0	0		0	1	0		0	1	0
1	0	1	0	0		0	1	1		0	1	0
1	0	1	0	0		1	0	0		0	1	0
1	0	1	0	0		1	0	1		0	1	0
1	0	1	0	0		1	1	0		0	1	0
1	0	1	0	0		1	1	1		0	1	0
1	0	1	0	1		0	0	0		0	1	0
1	0	1	0	1		0	0	1		0	1	0
1	0	1	0	1		0	1	0		0	1	0
1	0	1	0	1		0	1	1		0	1	0
1	0	1	0	1		1	0	0		0	1	0
1	0	1	0	1		1	0	1		0	1	0
1	0	1	0	1		1	1	0		0	1	0
1	0	1	0	1		1	1	1		0	1	0
1	0	1	1	0		0	0	0		0	1	0
1	0	1	1	0		0	0	1		0	1	0
1	0	1	1	0		0	1	0		0	1	0

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Table C.1 – Continued

U1	U2	U3	U4	D		V1'	V2'	V3'		V1	V2	V3
1	0	1	1	0		0	1	1		0	1	0
1	0	1	1	0		1	0	0		0	1	0
1	0	1	1	0		1	0	1		0	1	0
1	0	1	1	0		1	1	0		0	1	0
1	0	1	1	0		1	1	1		0	1	0
1	0	1	1	1		0	0	0		0	1	0
1	0	1	1	1		0	0	1		0	1	0
1	0	1	1	1		0	1	0		0	1	0
1	0	1	1	1		0	1	1		0	1	0
1	0	1	1	1		1	0	0		0	1	0
1	0	1	1	1		1	0	1		0	1	0
1	0	1	1	1		1	1	0		0	1	0
1	0	1	1	1		1	1	1		0	1	0
1	1	0	0	0		0	0	0		0	1	0
1	1	0	0	0		0	0	1		0	1	0
1	1	0	0	0		0	1	0		0	1	0
1	1	0	0	0		0	1	1		0	1	0
1	1	0	0	0		1	0	0		0	1	0
1	1	0	0	0		1	0	1		0	1	0
1	1	0	0	0		1	1	0		0	1	0
1	1	0	0	0		1	1	1		0	1	0
1	1	0	0	1		0	0	0		0	1	0
1	1	0	0	1		0	0	1		0	1	0
1	1	0	0	1		0	1	0		0	1	0
1	1	0	0	1		0	1	1		0	1	0
1	1	0	0	1		1	0	0		0	1	0
1	1	0	0	1		1	0	1		0	1	0
1	1	0	0	1		1	1	0		0	1	0
1	1	0	0	1		1	1	1		0	1	0
1	1	0	1	0		0	0	0		0	1	0
1	1	0	1	0		0	0	1		0	1	0
1	1	0	1	0		0	1	0		0	1	0
1	1	0	1	0		0	1	1		0	1	0
1	1	0	1	0		1	0	0		0	1	0
1	1	0	1	0		1	0	1		0	1	0
1	1	0	1	0		1	1	0		0	1	0
1	1	0	1	0		1	1	1		0	1	0
1	1	0	1	1		0	0	0		0	1	0
1	1	0	1	1		0	0	1		0	1	0
1	1	0	1	1		0	1	0		0	1	0

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Table C.1 – Continued

U1	U2	U3	U4	D		V1'	V2'	V3'		V1	V2	V3
1	1	0	1	1		0	1	1		0	1	0
1	1	0	1	1		1	0	0		0	1	0
1	1	0	1	1		1	0	1		0	1	0
1	1	0	1	1		1	1	0		0	1	0
1	1	0	1	1		1	1	1		0	1	0
1	1	1	0	0		0	0	0		0	1	0
1	1	1	0	0		0	0	1		0	1	0
1	1	1	0	0		0	1	0		0	1	0
1	1	1	0	0		0	1	1		0	1	0
1	1	1	0	0		1	0	0		0	1	0
1	1	1	0	0		1	0	1		0	1	0
1	1	1	0	0		1	1	0		0	1	0
1	1	1	0	0		1	1	1		0	1	0
1	1	1	0	1		0	0	0		0	1	0
1	1	1	0	1		0	0	1		0	1	0
1	1	1	0	1		0	1	0		0	1	0
1	1	1	0	1		0	1	1		0	1	0
1	1	1	0	1		1	0	0		0	1	0
1	1	1	0	1		1	0	1		0	1	0
1	1	1	0	1		1	1	0		0	1	0
1	1	1	0	1		1	1	1		0	1	0
1	1	1	1	0		0	0	0		1	0	1
1	1	1	1	0		0	0	1		1	0	1
1	1	1	1	0		0	1	0		1	0	1
1	1	1	1	0		0	1	1		1	0	1
1	1	1	1	0		1	0	0		1	0	1
1	1	1	1	0		1	0	1		1	0	1
1	1	1	1	0		1	1	0		1	0	1
1	1	1	1	0		1	1	1		0	1	0
1	1	1	1	1		0	0	0		1	0	1
1	1	1	1	1		0	0	1		1	0	1
1	1	1	1	1		0	1	0		1	0	1
1	1	1	1	1		0	1	1		1	0	1
1	1	1	1	1		1	0	0		1	0	1
1	1	1	1	1		1	0	1		1	0	1
1	1	1	1	1		1	1	0		1	0	1
1	1	1	1	1		1	1	1		0	1	0

Table C.2: Double Band Controller - Gating Signal Logic.

Inputs										Outputs			
X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
0	0	0	0	0	0	0	0	0		0	0	0	0
0	0	0	0	0	0	0	0	1		0	0	0	0
0	0	0	0	0	0	0	1	0		0	0	0	0
0	0	0	0	0	0	0	1	1		0	0	0	0
0	0	0	0	0	0	1	0	0		0	0	0	0
0	0	0	0	0	0	1	0	1		0	0	0	0
0	0	0	0	0	0	1	1	0		0	0	0	0
0	0	0	0	0	0	1	1	1		0	0	0	0
0	0	0	0	0	1	0	0	0		0	0	0	0
0	0	0	0	0	1	0	0	1		0	0	0	0
0	0	0	0	0	1	0	1	0		0	0	0	0
0	0	0	0	0	1	0	1	1		0	0	0	0
0	0	0	0	0	1	1	0	0		0	0	0	0
0	0	0	0	0	1	1	0	1		0	0	0	0
0	0	0	0	0	1	1	1	0		0	0	0	0
0	0	0	0	0	1	1	1	1		0	0	0	0
0	0	0	0	1	0	0	0	0		0	0	0	0
0	0	0	0	1	0	0	0	1		0	0	0	0
0	0	0	0	1	0	0	1	0		0	0	0	0
0	0	0	0	1	0	0	1	1		0	0	0	0
0	0	0	0	1	0	1	0	0		0	0	0	0
0	0	0	0	1	0	1	0	1		0	0	0	0
0	0	0	0	1	0	1	1	0		0	0	0	0
0	0	0	0	1	0	1	1	1		0	0	0	0
0	0	0	0	1	1	0	0	0		0	0	0	0
0	0	0	0	1	1	0	0	1		0	0	0	0
0	0	0	0	1	1	0	1	0		0	0	0	0
0	0	0	0	1	1	0	1	1		0	0	0	0
0	0	0	0	1	1	1	0	0		0	0	0	0
0	0	0	0	1	1	1	0	1		0	0	0	0
0	0	0	0	1	1	1	1	0		0	0	0	0
0	0	0	0	1	1	1	1	1		0	0	0	0
0	0	0	1	0	0	0	0	0		0	1	0	1
0	0	0	1	0	0	0	0	1		0	1	1	0
0	0	0	1	0	0	0	1	0		0	1	0	0
0	0	0	1	0	0	0	1	1		0	0	1	1
0	0	0	1	0	0	1	0	0		1	1	1	0

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
0	0	0	1	0	0	1	0	1		1	1	0	1
0	0	0	1	0	0	1	1	0		1	0	1	1
0	0	0	1	0	0	1	1	1		0	0	0	0
0	0	0	1	0	1	0	0	0		0	0	0	0
0	0	0	1	0	1	0	0	1		0	0	0	0
0	0	0	1	0	1	0	1	0		0	0	0	0
0	0	0	1	0	1	0	1	1		0	0	0	0
0	0	0	1	0	1	1	0	0		0	0	0	0
0	0	0	1	0	1	1	0	1		0	0	0	0
0	0	0	1	0	1	1	1	0		0	0	0	0
0	0	0	1	0	1	1	1	1		0	0	0	0
0	0	0	1	1	0	0	0	0		0	1	0	1
0	0	0	1	1	0	0	0	1		0	0	1	1
0	0	0	1	1	0	0	1	0		0	1	0	0
0	0	0	1	1	0	0	1	1		0	1	1	0
0	0	0	1	1	0	1	0	0		1	0	1	1
0	0	0	1	1	0	1	0	1		1	1	0	1
0	0	0	1	1	0	1	1	0		1	1	1	0
0	0	0	1	1	0	1	1	1		0	0	0	0
0	0	0	1	1	1	0	0	0		0	0	0	0
0	0	0	1	1	1	0	0	1		0	0	0	0
0	0	0	1	1	1	0	1	0		0	0	0	0
0	0	0	1	1	1	0	1	1		0	0	0	0
0	0	0	1	1	1	1	0	0		0	0	0	0
0	0	0	1	1	1	1	0	1		0	0	0	0
0	0	0	1	1	1	1	1	0		0	0	0	0
0	0	0	1	1	1	1	1	1		0	0	0	0
0	0	1	0	0	0	0	0	0		0	0	0	0
0	0	1	0	0	0	0	0	1		0	0	0	0
0	0	1	0	0	0	0	1	0		0	0	0	0
0	0	1	0	0	0	0	1	1		0	0	0	0
0	0	1	0	0	0	1	0	0		0	0	0	0
0	0	1	0	0	0	1	0	1		0	0	0	0
0	0	1	0	0	0	1	1	0		0	0	0	0
0	0	1	0	0	0	1	1	1		0	0	0	0
0	0	1	0	0	1	0	0	0		0	0	0	0
0	0	1	0	0	1	0	0	1		0	0	0	0
0	0	1	0	0	1	0	1	0		0	0	0	0
0	0	1	0	0	1	0	1	1		0	0	0	0

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
0	0	1	0	0	1	1	0	0		0	0	0	0
0	0	1	0	0	1	1	0	1		0	0	0	0
0	0	1	0	0	1	1	1	0		0	0	0	0
0	0	1	0	0	1	1	1	1		0	0	0	0
0	0	1	0	1	0	0	0	0		0	0	0	0
0	0	1	0	1	0	0	0	1		0	0	0	0
0	0	1	0	1	0	0	1	0		0	0	0	0
0	0	1	0	1	0	0	1	1		0	0	0	0
0	0	1	0	1	0	1	0	0		0	0	0	0
0	0	1	0	1	0	1	0	1		0	0	0	0
0	0	1	0	1	0	1	1	0		0	0	0	0
0	0	1	0	1	0	1	1	1		0	0	0	0
0	0	1	0	1	1	0	0	0		0	0	0	0
0	0	1	0	1	1	0	0	1		0	0	0	0
0	0	1	0	1	1	0	1	0		0	0	0	0
0	0	1	0	1	1	0	1	1		0	0	0	0
0	0	1	0	1	1	1	0	0		0	0	0	0
0	0	1	0	1	1	1	0	1		0	0	0	0
0	0	1	0	1	1	1	1	0		0	0	0	0
0	0	1	0	1	1	1	1	1		0	0	0	0
0	0	1	1	0	0	0	0	0		0	1	1	0
0	0	1	1	0	0	0	0	1		0	1	0	1
0	0	1	1	0	0	0	1	0		0	1	0	0
0	0	1	1	0	0	0	1	1		1	0	1	1
0	0	1	1	0	0	1	0	0		1	1	0	1
0	0	1	1	0	0	1	0	1		1	1	1	0
0	0	1	1	0	0	1	1	0		0	0	1	1
0	0	1	1	0	0	1	1	1		0	0	0	0
0	0	1	1	0	1	0	0	0		0	1	1	0
0	0	1	1	0	1	0	0	1		1	0	1	1
0	0	1	1	0	1	0	1	0		0	1	0	0
0	0	1	1	0	1	0	1	1		0	1	0	1
0	0	1	1	0	1	1	0	0		0	0	1	1
0	0	1	1	0	1	1	0	1		1	1	1	0
0	0	1	1	0	1	1	1	0		1	1	0	1
0	0	1	1	0	1	1	1	1		0	0	0	0
0	0	1	1	1	0	0	0	0		0	0	0	0
0	0	1	1	1	0	0	0	1		0	0	0	0
0	0	1	1	1	0	0	1	0		0	0	0	0

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
0	0	1	1	1	0	0	1	1		0	0	0	0
0	0	1	1	1	0	1	0	0		0	0	0	0
0	0	1	1	1	0	1	0	1		0	0	0	0
0	0	1	1	1	0	1	1	0		0	0	0	0
0	0	1	1	1	0	1	1	1		0	0	0	0
0	0	1	1	1	1	0	0	0		0	0	0	0
0	0	1	1	1	1	0	0	1		0	0	0	0
0	0	1	1	1	1	0	1	0		0	0	0	0
0	0	1	1	1	1	0	1	1		0	0	0	0
0	0	1	1	1	1	1	0	0		0	0	0	0
0	0	1	1	1	1	1	0	1		0	0	0	0
0	0	1	1	1	1	1	1	0		0	0	0	0
0	0	1	1	1	1	1	1	1		0	0	0	0
0	1	0	0	0	0	0	0	0		0	0	0	0
0	1	0	0	0	0	0	0	1		0	0	0	0
0	1	0	0	0	0	0	1	0		0	0	0	0
0	1	0	0	0	0	0	1	1		0	0	0	0
0	1	0	0	0	0	1	0	0		0	0	0	0
0	1	0	0	0	0	1	0	1		0	0	0	0
0	1	0	0	0	0	1	1	0		0	0	0	0
0	1	0	0	0	0	1	1	1		0	0	0	0
0	1	0	0	0	1	0	0	0		0	0	0	0
0	1	0	0	0	1	0	0	1		0	0	0	0
0	1	0	0	0	1	0	1	0		0	0	0	0
0	1	0	0	0	1	0	1	1		0	0	0	0
0	1	0	0	0	1	1	0	0		0	0	0	0
0	1	0	0	0	1	1	0	1		0	0	0	0
0	1	0	0	0	1	1	1	0		0	0	0	0
0	1	0	0	0	1	1	1	1		0	0	0	0
0	1	0	0	1	0	0	0	0		0	0	0	0
0	1	0	0	1	0	0	0	1		0	0	0	0
0	1	0	0	1	0	0	1	0		0	0	0	0
0	1	0	0	1	0	0	1	1		0	0	0	0
0	1	0	0	1	0	1	0	0		0	0	0	0
0	1	0	0	1	0	1	0	1		0	0	0	0
0	1	0	0	1	0	1	1	0		0	0	0	0
0	1	0	0	1	0	1	1	1		0	0	0	0
0	1	0	0	1	1	0	0	0		0	0	0	0
0	1	0	0	1	1	0	0	1		0	0	0	0

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
0	1	0	0	1	1	0	1	0		0	0	0	0
0	1	0	0	1	1	0	1	1		0	0	0	0
0	1	0	0	1	1	1	0	0		0	0	0	0
0	1	0	0	1	1	1	0	1		0	0	0	0
0	1	0	0	1	1	1	1	0		0	0	0	0
0	1	0	0	1	1	1	1	1		0	0	0	0
0	1	0	1	0	0	0	0	0		0	0	0	0
0	1	0	1	0	0	0	0	1		0	0	0	0
0	1	0	1	0	0	0	1	0		0	0	0	0
0	1	0	1	0	0	0	1	1		0	0	0	0
0	1	0	1	0	0	1	0	0		0	0	0	0
0	1	0	1	0	0	1	0	1		0	0	0	0
0	1	0	1	0	0	1	1	0		0	0	0	0
0	1	0	1	0	0	1	1	1		0	0	0	0
0	1	0	1	0	1	0	0	0		0	0	0	0
0	1	0	1	0	1	0	0	1		0	0	0	0
0	1	0	1	0	1	0	1	0		0	0	0	0
0	1	0	1	0	1	0	1	1		0	0	0	0
0	1	0	1	0	1	1	0	0		0	0	0	0
0	1	0	1	0	1	1	0	1		0	0	0	0
0	1	0	1	0	1	1	1	0		0	0	0	0
0	1	0	1	0	1	1	1	1		0	0	0	0
0	1	0	1	1	0	0	0	0		0	0	0	0
0	1	0	1	1	0	0	0	1		0	0	0	0
0	1	0	1	1	0	0	1	0		0	0	0	0
0	1	0	1	1	0	0	1	1		0	0	0	0
0	1	0	1	1	0	1	0	0		0	0	0	0
0	1	0	1	1	0	1	0	1		0	0	0	0
0	1	0	1	1	0	1	1	0		0	0	0	0
0	1	0	1	1	0	1	1	1		0	0	0	0
0	1	0	1	1	1	0	0	0		0	0	0	0
0	1	0	1	1	1	0	0	1		0	0	0	0
0	1	0	1	1	1	0	1	0		0	0	0	0
0	1	0	1	1	1	0	1	1		0	0	0	0
0	1	0	1	1	1	1	0	0		0	0	0	0
0	1	0	1	1	1	1	0	1		0	0	0	0
0	1	0	1	1	1	1	1	0		0	0	0	0
0	1	0	1	1	1	1	1	1		0	0	0	0
0	1	1	0	0	0	0	0	0		0	0	0	0

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
0	1	1	0	0	0	0	0	1		0	0	0	0
0	1	1	0	0	0	0	1	0		0	0	0	0
0	1	1	0	0	0	0	1	1		0	0	0	0
0	1	1	0	0	0	1	0	0		0	0	0	0
0	1	1	0	0	0	1	0	1		0	0	0	0
0	1	1	0	0	0	1	1	0		0	0	0	0
0	1	1	0	0	0	1	1	1		0	0	0	0
0	1	1	0	0	1	0	0	0		1	0	1	1
0	1	1	0	0	1	0	0	1		1	1	0	1
0	1	1	0	0	1	0	1	0		0	1	0	0
0	1	1	0	0	1	0	1	1		0	1	1	0
0	1	1	0	0	1	1	0	0		0	1	0	1
0	1	1	0	0	1	1	0	1		0	0	1	1
0	1	1	0	0	1	1	1	0		1	1	1	0
0	1	1	0	0	1	1	1	1		0	0	0	0
0	1	1	0	1	0	0	0	0		0	0	0	0
0	1	1	0	1	0	0	0	1		0	0	0	0
0	1	1	0	1	0	0	1	0		0	0	0	0
0	1	1	0	1	0	0	1	1		0	0	0	0
0	1	1	0	1	0	1	0	0		0	0	0	0
0	1	1	0	1	0	1	0	1		0	0	0	0
0	1	1	0	1	0	1	1	0		0	0	0	0
0	1	1	0	1	0	1	1	1		0	0	0	0
0	1	1	0	1	1	0	0	0		0	0	0	0
0	1	1	0	1	1	0	0	1		0	0	0	0
0	1	1	0	1	1	0	1	0		0	0	0	0
0	1	1	0	1	1	0	1	1		0	0	0	0
0	1	1	0	1	1	1	0	0		0	0	0	0
0	1	1	0	1	1	1	0	1		0	0	0	0
0	1	1	0	1	1	1	1	0		0	0	0	0
0	1	1	0	1	1	1	1	1		0	0	0	0
0	1	1	1	0	0	0	0	0		0	0	0	0
0	1	1	1	0	0	0	0	1		0	0	0	0
0	1	1	1	0	0	0	1	0		0	0	0	0
0	1	1	1	0	0	0	1	1		0	0	0	0
0	1	1	1	0	0	1	0	0		0	0	0	0
0	1	1	1	0	0	1	0	1		0	0	0	0
0	1	1	1	0	0	1	1	0		0	0	0	0
0	1	1	1	0	0	1	1	1		0	0	0	0

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
0	1	1	1	0	1	0	0	0		1	0	1	1
0	1	1	1	0	1	0	0	1		0	1	1	0
0	1	1	1	0	1	0	1	0		0	1	0	0
0	1	1	1	0	1	0	1	1		1	1	0	1
0	1	1	1	0	1	1	0	0		1	1	1	0
0	1	1	1	0	1	1	0	1		0	0	1	1
0	1	1	1	0	1	1	1	0		0	1	0	1
0	1	1	1	0	1	1	1	1		0	0	0	0
0	1	1	1	1	0	0	0	0		0	0	0	0
0	1	1	1	1	0	0	0	1		0	0	0	0
0	1	1	1	1	0	0	1	0		0	0	0	0
0	1	1	1	1	0	0	1	1		0	0	0	0
0	1	1	1	1	0	1	0	0		0	0	0	0
0	1	1	1	1	0	1	0	1		0	0	0	0
0	1	1	1	1	0	1	1	0		0	0	0	0
0	1	1	1	1	0	1	1	1		0	0	0	0
0	1	1	1	1	1	0	0	0		0	0	0	0
0	1	1	1	1	1	0	0	1		0	0	0	0
0	1	1	1	1	1	0	1	0		0	0	0	0
0	1	1	1	1	1	0	1	1		0	0	0	0
0	1	1	1	1	1	1	0	0		0	0	0	0
0	1	1	1	1	1	1	0	1		0	0	0	0
0	1	1	1	1	1	1	1	0		0	0	0	0
0	1	1	1	1	1	1	1	1		0	0	0	0
1	0	0	0	0	0	0	0	0		0	0	0	0
1	0	0	0	0	0	0	0	1		0	0	0	0
1	0	0	0	0	0	0	1	0		0	0	0	0
1	0	0	0	0	0	0	1	1		0	0	0	0
1	0	0	0	0	0	1	0	0		0	0	0	0
1	0	0	0	0	0	1	0	1		0	0	0	0
1	0	0	0	0	0	1	1	0		0	0	0	0
1	0	0	0	0	0	1	1	1		0	0	0	0
1	0	0	0	0	1	0	0	0		0	0	0	0
1	0	0	0	0	1	0	0	1		0	0	0	0
1	0	0	0	0	1	0	1	0		0	0	0	0
1	0	0	0	0	1	0	1	1		0	0	0	0
1	0	0	0	0	1	1	0	0		0	0	0	0
1	0	0	0	0	1	1	0	1		0	0	0	0
1	0	0	0	0	1	1	1	0		0	0	0	0

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
1	0	0	0	0	1	1	1	1		0	0	0	0
1	0	0	0	1	0	0	0	0		0	0	1	1
1	0	0	0	1	0	0	0	1		1	1	1	0
1	0	0	0	1	0	0	1	0		0	1	0	0
1	0	0	0	1	0	0	1	1		0	1	0	1
1	0	0	0	1	0	1	0	0		0	1	1	0
1	0	0	0	1	0	1	0	1		1	0	1	1
1	0	0	0	1	0	1	1	0		1	1	0	1
1	0	0	0	1	0	1	1	1		0	0	0	0
1	0	0	0	1	1	0	0	0		0	0	0	0
1	0	0	0	1	1	0	0	1		0	0	0	0
1	0	0	0	1	1	0	1	0		0	0	0	0
1	0	0	0	1	1	0	1	1		0	0	0	0
1	0	0	0	1	1	1	0	0		0	0	0	0
1	0	0	0	1	1	1	0	1		0	0	0	0
1	0	0	0	1	1	1	1	0		0	0	0	0
1	0	0	0	1	1	1	1	1		0	0	0	0
1	0	0	1	0	0	0	0	0		0	0	0	0
1	0	0	1	0	0	0	0	1		0	0	0	0
1	0	0	1	0	0	0	1	0		0	0	0	0
1	0	0	1	0	0	0	1	1		0	0	0	0
1	0	0	1	0	0	1	0	0		0	0	0	0
1	0	0	1	0	0	1	0	1		0	0	0	0
1	0	0	1	0	0	1	1	0		0	0	0	0
1	0	0	1	0	0	1	1	1		0	0	0	0
1	0	0	1	0	1	0	0	0		0	0	0	0
1	0	0	1	0	1	0	0	1		0	0	0	0
1	0	0	1	0	1	0	1	0		0	0	0	0
1	0	0	1	0	1	0	1	1		0	0	0	0
1	0	0	1	0	1	1	0	0		0	0	0	0
1	0	0	1	0	1	1	0	1		0	0	0	0
1	0	0	1	0	1	1	1	0		0	0	0	0
1	0	0	1	0	1	1	1	1		0	0	0	0
1	0	0	1	1	0	0	0	0		0	0	1	1
1	0	0	1	1	0	0	0	1		0	1	0	1
1	0	0	1	1	0	0	1	0		0	1	0	0
1	0	0	1	1	0	0	1	1		1	1	1	0
1	0	0	1	1	0	1	0	0		1	1	0	1
1	0	0	1	1	0	1	0	1		1	0	1	1

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
1	0	0	1	1	0	1	1	0		0	1	1	0
1	0	0	1	1	0	1	1	1		0	0	0	0
1	0	0	1	1	1	0	0	0		0	0	0	0
1	0	0	1	1	1	0	0	1		0	0	0	0
1	0	0	1	1	1	0	1	0		0	0	0	0
1	0	0	1	1	1	0	1	1		0	0	0	0
1	0	0	1	1	1	1	0	0		0	0	0	0
1	0	0	1	1	1	1	0	1		0	0	0	0
1	0	0	1	1	1	1	1	0		0	0	0	0
1	0	0	1	1	1	1	1	1		0	0	0	0
1	0	1	0	0	0	0	0	0		0	0	0	0
1	0	1	0	0	0	0	0	1		0	0	0	0
1	0	1	0	0	0	0	1	0		0	0	0	0
1	0	1	0	0	0	0	1	1		0	0	0	0
1	0	1	0	0	0	1	0	0		0	0	0	0
1	0	1	0	0	0	1	0	1		0	0	0	0
1	0	1	0	0	0	1	1	0		0	0	0	0
1	0	1	0	0	0	1	1	1		0	0	0	0
1	0	1	0	0	1	0	0	0		0	0	0	0
1	0	1	0	0	1	0	0	1		0	0	0	0
1	0	1	0	0	1	0	1	0		0	0	0	0
1	0	1	0	0	1	0	1	1		0	0	0	0
1	0	1	0	0	1	1	0	0		0	0	0	0
1	0	1	0	0	1	1	0	1		0	0	0	0
1	0	1	0	0	1	1	1	0		0	0	0	0
1	0	1	0	0	1	1	1	1		0	0	0	0
1	0	1	0	1	0	0	0	0		0	0	0	0
1	0	1	0	1	0	0	0	1		0	0	0	0
1	0	1	0	1	0	0	1	0		0	0	0	0
1	0	1	0	1	0	0	1	1		0	0	0	0
1	0	1	0	1	0	1	0	0		0	0	0	0
1	0	1	0	1	0	1	0	1		0	0	0	0
1	0	1	0	1	0	1	1	0		0	0	0	0
1	0	1	0	1	0	1	1	1		0	0	0	0
1	0	1	0	1	1	0	0	0		0	0	0	0
1	0	1	0	1	1	0	0	1		0	0	0	0
1	0	1	0	1	1	0	1	0		0	0	0	0
1	0	1	0	1	1	0	1	1		0	0	0	0
1	0	1	0	1	1	1	0	0		0	0	0	0

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
1	0	1	0	1	1	1	0	1		0	0	0	0
1	0	1	0	1	1	1	1	0		0	0	0	0
1	0	1	0	1	1	1	1	1		0	0	0	0
1	0	1	1	0	0	0	0	0		0	0	0	0
1	0	1	1	0	0	0	0	1		0	0	0	0
1	0	1	1	0	0	0	1	0		0	0	0	0
1	0	1	1	0	0	0	1	1		0	0	0	0
1	0	1	1	0	0	1	0	0		0	0	0	0
1	0	1	1	0	0	1	0	1		0	0	0	0
1	0	1	1	0	0	1	1	0		0	0	0	0
1	0	1	1	0	0	1	1	1		0	0	0	0
1	0	1	1	0	1	0	0	0		0	0	0	0
1	0	1	1	0	1	0	0	1		0	0	0	0
1	0	1	1	0	1	0	1	0		0	0	0	0
1	0	1	1	0	1	0	1	1		0	0	0	0
1	0	1	1	0	1	1	0	0		0	0	0	0
1	0	1	1	0	1	1	0	1		0	0	0	0
1	0	1	1	0	1	1	1	0		0	0	0	0
1	0	1	1	0	1	1	1	1		0	0	0	0
1	0	1	1	1	0	0	0	0		0	0	0	0
1	0	1	1	1	0	0	0	1		0	0	0	0
1	0	1	1	1	0	0	1	0		0	0	0	0
1	0	1	1	1	0	0	1	1		0	0	0	0
1	0	1	1	1	0	1	0	0		0	0	0	0
1	0	1	1	1	0	1	0	1		0	0	0	0
1	0	1	1	1	0	1	1	0		0	0	0	0
1	0	1	1	1	0	1	1	1		0	0	0	0
1	0	1	1	1	1	0	0	0		0	0	0	0
1	0	1	1	1	1	0	0	1		0	0	0	0
1	0	1	1	1	1	0	1	0		0	0	0	0
1	0	1	1	1	1	0	1	1		0	0	0	0
1	0	1	1	1	1	1	0	0		0	0	0	0
1	0	1	1	1	1	1	0	1		0	0	0	0
1	0	1	1	1	1	1	1	0		0	0	0	0
1	0	1	1	1	1	1	1	1		0	0	0	0
1	0	1	1	1	1	0	0	0		0	0	0	0
1	0	1	1	1	1	0	0	1		0	0	0	0
1	0	1	1	1	1	0	1	0		0	0	0	0
1	0	1	1	1	1	0	1	1		0	0	0	0
1	0	1	1	1	1	1	0	0		0	0	0	0
1	0	1	1	1	1	1	0	1		0	0	0	0
1	0	1	1	1	1	1	1	0		0	0	0	0
1	0	1	1	1	1	1	1	1		0	0	0	0
1	1	0	0	0	0	0	0	0		0	0	0	0
1	1	0	0	0	0	0	0	1		0	0	0	0
1	1	0	0	0	0	0	1	0		0	0	0	0
1	1	0	0	0	0	0	1	1		0	0	0	0

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Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
1	1	0	0	0	0	1	0	0		0	0	0	0
1	1	0	0	0	0	1	0	1		0	0	0	0
1	1	0	0	0	0	1	1	0		0	0	0	0
1	1	0	0	0	0	1	1	1		0	0	0	0
1	1	0	0	0	1	0	0	0		0	0	0	0
1	1	0	0	0	1	0	0	1		0	0	0	0
1	1	0	0	0	1	0	1	0		0	0	0	0
1	1	0	0	0	1	0	1	1		0	0	0	0
1	1	0	0	0	1	1	0	0		0	0	0	0
1	1	0	0	0	1	1	0	1		0	0	0	0
1	1	0	0	0	1	1	1	0		0	0	0	0
1	1	0	0	0	1	1	1	1		0	0	0	0
1	1	0	0	1	0	0	0	0		1	1	1	0
1	1	0	0	1	0	0	0	1		0	0	1	1
1	1	0	0	1	0	0	1	0		0	1	0	0
1	1	0	0	1	0	0	1	1		1	1	0	1
1	1	0	0	1	0	1	0	0		1	0	1	1
1	1	0	0	1	0	1	0	1		0	1	1	0
1	1	0	0	1	0	1	1	0		0	1	0	1
1	1	0	0	1	0	1	1	1		0	0	0	0
1	1	0	0	1	1	0	0	0		1	1	1	0
1	1	0	0	1	1	0	0	1		1	1	0	1
1	1	0	0	1	1	0	1	0		0	1	0	0
1	1	0	0	1	1	0	1	1		0	0	1	1
1	1	0	0	1	1	1	0	0		0	1	0	1
1	1	0	0	1	1	1	0	1		0	1	1	0
1	1	0	0	1	1	1	1	0		1	0	1	1
1	1	0	0	1	1	1	1	1		0	0	0	0
1	1	0	1	0	0	0	0	0		0	0	0	0
1	1	0	1	0	0	0	0	1		0	0	0	0
1	1	0	1	0	0	0	1	0		0	0	0	0
1	1	0	1	0	0	0	1	1		0	0	0	0
1	1	0	1	0	0	1	0	0		0	0	0	0
1	1	0	1	0	0	1	0	1		0	0	0	0
1	1	0	1	0	0	1	1	0		0	0	0	0
1	1	0	1	0	0	1	1	1		0	0	0	0
1	1	0	1	0	1	0	0	0		0	0	0	0
1	1	0	1	0	1	0	0	1		0	0	0	0
1	1	0	1	0	1	0	1	0		0	0	0	0

Continued on Next Page...

Table C.2 – Continued

X B>A	Y C>A	Z C>B	A>0	B>0	C>0	V1	V2	V3		U	A	B	C
1	1	0	1	0	1	0	1	1		0	0	0	0
1	1	0	1	0	1	1	0	0		0	0	0	0
1	1	0	1	0	1	1	0	1		0	0	0	0
1	1	0	1	0	1	1	1	0		0	0	0	0
1	1	0	1	0	1	1	1	1		0	0	0	0
1	1	0	1	1	0	0	0	0		0	0	0	0
1	1	0	1	1	0	0	0	1		0	0	0	0
1	1	0	1	1	0	0	1	0		0	0	0	0

Table C.3: Double Band Controller - Switch Logic.

Inputs					Outputs					
U	A	B	C		SAa	SAb	SBa	SBb	SCa	SCb
0	0	0	0		0	0	0	0	0	0
0	0	0	1		0	0	0	0	1	1
0	0	1	0		0	0	1	1	0	0
0	0	1	1		0	0	1	0	0	1
0	1	0	0		1	1	0	0	0	0
0	1	0	1		1	0	0	0	0	1
0	1	1	0		1	0	0	1	0	0
0	1	1	1		0	0	0	0	0	0
1	0	0	0		0	0	0	0	0	0
1	0	0	1		0	0	0	0	1	1
1	0	1	0		0	0	1	1	0	0
1	0	1	1		0	0	0	1	1	0
1	1	0	0		1	1	0	0	0	0
1	1	0	1		0	1	0	0	1	0
1	1	1	0		0	1	1	0	0	0
1	1	1	1		0	0	0	0	0	0

Appendix D

Input Voltage Identifier Mealy State Machine VHDL Code

```
-- mealy_phase_choser

library ieee;
use ieee.std_logic_1164.all;

entity mealy_input_voltage_identifier is
    port (U1,U2,U3,U4: in std_logic;
        D: in std_logic;
        V1in,V2in,V3in: in std_logic;
        V1,V2,V3: out std_logic);
end mealy_input_voltage_identifier;

architecture behave of mealy_input_voltage_identifier is
    signal in_stat: std_logic_vector (7 downto 0);
    signal VSup_Stat: std_logic_vector (2 downto 0);
begin


    -- Combine X,Y,Z
inmix: process (U1,U2,U3,U4,D,V1in,V2in,V3in)
begin
        in_stat(0) <= V3in;
```

```
        in_stat(1) <= V2in;
        in_stat(2) <= V1in;
        in_stat(3) <= D;
        in_stat(4) <= U4;
        in_stat(5) <= U2;
        in_stat(6) <= U1;
        in_stat(7) <= U3;
end process inmix;


    -- Mealy output definition using Q & reg_stat data
outputs: process (in_stat)
    begin
        case in_stat is
                when "00000000" => VSup_Stat <= "000";
when "00000001" => VSup_Stat <= "000";
when "00000010" => VSup_Stat <= "000";
when "00000011" => VSup_Stat <= "000";
when "00000100" => VSup_Stat <= "000";
when "00000101" => VSup_Stat <= "000";
when "00000110" => VSup_Stat <= "000";
when "00000111" => VSup_Stat <= "000";
when "00001000" => VSup_Stat <= "000";
when "00001001" => VSup_Stat <= "000";
when "00001010" => VSup_Stat <= "000";
when "00001011" => VSup_Stat <= "000";
when "00001100" => VSup_Stat <= "000";
when "00001101" => VSup_Stat <= "000";
when "00001110" => VSup_Stat <= "000";
when "00001111" => VSup_Stat <= "000";
when "00010000" => VSup_Stat <= "000";
when "00010001" => VSup_Stat <= "000";
when "00010010" => VSup_Stat <= "011";
when "00010011" => VSup_Stat <= "001";
when "00010100" => VSup_Stat <= "110";
when "00010101" => VSup_Stat <= "100";
when "00010110" => VSup_Stat <= "010";
when "00010111" => VSup_Stat <= "010";
when "00011000" => VSup_Stat <= "000";
when "00011001" => VSup_Stat <= "001";
when "00011010" => VSup_Stat <= "010";
when "00011011" => VSup_Stat <= "011";
when "00011100" => VSup_Stat <= "100";
```

```
when "00011101" => VSup_Stat <= "101";
when "00011110" => VSup_Stat <= "110";
when "00011111" => VSup_Stat <= "010";
when "00100000" => VSup_Stat <= "010";
when "00100001" => VSup_Stat <= "010";
when "00100010" => VSup_Stat <= "010";
when "00100011" => VSup_Stat <= "010";
when "00100100" => VSup_Stat <= "010";
when "00100101" => VSup_Stat <= "010";
when "00100110" => VSup_Stat <= "010";
when "00100111" => VSup_Stat <= "010";
when "00101000" => VSup_Stat <= "010";
when "00101001" => VSup_Stat <= "010";
when "00101010" => VSup_Stat <= "010";
when "00101011" => VSup_Stat <= "010";
when "00101100" => VSup_Stat <= "010";
when "00101101" => VSup_Stat <= "010";
when "00101110" => VSup_Stat <= "010";
when "00101111" => VSup_Stat <= "010";
when "00110000" => VSup_Stat <= "000";
when "00110001" => VSup_Stat <= "001";
when "00110010" => VSup_Stat <= "010";
when "00110011" => VSup_Stat <= "011";
when "00110100" => VSup_Stat <= "100";
when "00110101" => VSup_Stat <= "101";
when "00110110" => VSup_Stat <= "110";
when "00110111" => VSup_Stat <= "010";
when "00111000" => VSup_Stat <= "000";
when "00111001" => VSup_Stat <= "001";
when "00111010" => VSup_Stat <= "010";
when "00111011" => VSup_Stat <= "011";
when "00111100" => VSup_Stat <= "100";
when "00111101" => VSup_Stat <= "101";
when "00111110" => VSup_Stat <= "110";
when "00111111" => VSup_Stat <= "010";
when "01000000" => VSup_Stat <= "010";
when "01000001" => VSup_Stat <= "010";
when "01000010" => VSup_Stat <= "010";
when "01000011" => VSup_Stat <= "010";
when "01000100" => VSup_Stat <= "010";
when "01000101" => VSup_Stat <= "010";
when "01000110" => VSup_Stat <= "010";
when "01000111" => VSup_Stat <= "010";
```

```
when "01001000" => VSup_Stat <= "010";
when "01001001" => VSup_Stat <= "010";
when "01001010" => VSup_Stat <= "010";
when "01001011" => VSup_Stat <= "010";
when "01001100" => VSup_Stat <= "010";
when "01001101" => VSup_Stat <= "010";
when "01001110" => VSup_Stat <= "010";
when "01001111" => VSup_Stat <= "010";
when "01010000" => VSup_Stat <= "010";
when "01010001" => VSup_Stat <= "010";
when "01010010" => VSup_Stat <= "010";
when "01010011" => VSup_Stat <= "010";
when "01010100" => VSup_Stat <= "010";
when "01010101" => VSup_Stat <= "010";
when "01010110" => VSup_Stat <= "010";
when "01010111" => VSup_Stat <= "010";
when "01011000" => VSup_Stat <= "010";
when "01011001" => VSup_Stat <= "010";
when "01011010" => VSup_Stat <= "010";
when "01011011" => VSup_Stat <= "010";
when "01011100" => VSup_Stat <= "010";
when "01011101" => VSup_Stat <= "010";
when "01011110" => VSup_Stat <= "010";
when "01011111" => VSup_Stat <= "010";
when "01100000" => VSup_Stat <= "010";
when "01100001" => VSup_Stat <= "010";
when "01100010" => VSup_Stat <= "010";
when "01100011" => VSup_Stat <= "010";
when "01100100" => VSup_Stat <= "010";
when "01100101" => VSup_Stat <= "010";
when "01100110" => VSup_Stat <= "010";
when "01100111" => VSup_Stat <= "010";
when "01101000" => VSup_Stat <= "010";
when "01101001" => VSup_Stat <= "010";
when "01101010" => VSup_Stat <= "010";
when "01101011" => VSup_Stat <= "010";
when "01101100" => VSup_Stat <= "010";
when "01101101" => VSup_Stat <= "010";
when "01101110" => VSup_Stat <= "010";
when "01101111" => VSup_Stat <= "010";
when "01110000" => VSup_Stat <= "000";
when "01110001" => VSup_Stat <= "001";
when "01110010" => VSup_Stat <= "010";
```

```
when "01110011" => VSup_Stat <= "011";
when "01110100" => VSup_Stat <= "100";
when "01110101" => VSup_Stat <= "101";
when "01110110" => VSup_Stat <= "110";
when "01110111" => VSup_Stat <= "010";
when "01111000" => VSup_Stat <= "001";
when "01111001" => VSup_Stat <= "011";
when "01111010" => VSup_Stat <= "110";
when "01111011" => VSup_Stat <= "010";
when "01111100" => VSup_Stat <= "101";
when "01111101" => VSup_Stat <= "101";
when "01111110" => VSup_Stat <= "100";
when "01111111" => VSup_Stat <= "010";
when "10000000" => VSup_Stat <= "010";
when "10000001" => VSup_Stat <= "010";
when "10000010" => VSup_Stat <= "010";
when "10000011" => VSup_Stat <= "010";
when "10000100" => VSup_Stat <= "010";
when "10000101" => VSup_Stat <= "010";
when "10000110" => VSup_Stat <= "010";
when "10000111" => VSup_Stat <= "010";
when "10001000" => VSup_Stat <= "010";
when "10001001" => VSup_Stat <= "010";
when "10001010" => VSup_Stat <= "010";
when "10001011" => VSup_Stat <= "010";
when "10001100" => VSup_Stat <= "010";
when "10001101" => VSup_Stat <= "010";
when "10001110" => VSup_Stat <= "010";
when "10001111" => VSup_Stat <= "010";
when "10010000" => VSup_Stat <= "010";
when "10010001" => VSup_Stat <= "010";
when "10010010" => VSup_Stat <= "010";
when "10010011" => VSup_Stat <= "010";
when "10010100" => VSup_Stat <= "010";
when "10010101" => VSup_Stat <= "010";
when "10010110" => VSup_Stat <= "010";
when "10010111" => VSup_Stat <= "010";
when "10011000" => VSup_Stat <= "010";
when "10011001" => VSup_Stat <= "010";
when "10011010" => VSup_Stat <= "010";
when "10011011" => VSup_Stat <= "010";
when "10011100" => VSup_Stat <= "010";
when "10011101" => VSup_Stat <= "010";
```

```
when "10011110" => VSup_Stat <= "010";
when "10011111" => VSup_Stat <= "010";
when "10100000" => VSup_Stat <= "010";
when "10100001" => VSup_Stat <= "010";
when "10100010" => VSup_Stat <= "010";
when "10100011" => VSup_Stat <= "010";
when "10100100" => VSup_Stat <= "010";
when "10100101" => VSup_Stat <= "010";
when "10100110" => VSup_Stat <= "010";
when "10100111" => VSup_Stat <= "010";
when "10101000" => VSup_Stat <= "010";
when "10101001" => VSup_Stat <= "010";
when "10101010" => VSup_Stat <= "010";
when "10101011" => VSup_Stat <= "010";
when "10101100" => VSup_Stat <= "010";
when "10101101" => VSup_Stat <= "010";
when "10101110" => VSup_Stat <= "010";
when "10101111" => VSup_Stat <= "010";
when "10110000" => VSup_Stat <= "010";
when "10110001" => VSup_Stat <= "010";
when "10110010" => VSup_Stat <= "010";
when "10110011" => VSup_Stat <= "010";
when "10110100" => VSup_Stat <= "010";
when "10110101" => VSup_Stat <= "010";
when "10110110" => VSup_Stat <= "010";
when "10110111" => VSup_Stat <= "010";
when "10111000" => VSup_Stat <= "010";
when "10111001" => VSup_Stat <= "010";
when "10111010" => VSup_Stat <= "010";
when "10111011" => VSup_Stat <= "010";
when "10111100" => VSup_Stat <= "010";
when "10111101" => VSup_Stat <= "010";
when "10111110" => VSup_Stat <= "010";
when "10111111" => VSup_Stat <= "010";
when "11000000" => VSup_Stat <= "010";
when "11000001" => VSup_Stat <= "010";
when "11000010" => VSup_Stat <= "010";
when "11000011" => VSup_Stat <= "010";
when "11000100" => VSup_Stat <= "010";
when "11000101" => VSup_Stat <= "010";
when "11000110" => VSup_Stat <= "010";
when "11000111" => VSup_Stat <= "010";
when "11001000" => VSup_Stat <= "010";
```

```
when "11001001" => VSup_Stat <= "010";
when "11001010" => VSup_Stat <= "010";
when "11001011" => VSup_Stat <= "010";
when "11001100" => VSup_Stat <= "010";
when "11001101" => VSup_Stat <= "010";
when "11001110" => VSup_Stat <= "010";
when "11001111" => VSup_Stat <= "010";
when "11010000" => VSup_Stat <= "010";
when "11010001" => VSup_Stat <= "010";
when "11010010" => VSup_Stat <= "010";
when "11010011" => VSup_Stat <= "010";
when "11010100" => VSup_Stat <= "010";
when "11010101" => VSup_Stat <= "010";
when "11010110" => VSup_Stat <= "010";
when "11010111" => VSup_Stat <= "010";
when "11011000" => VSup_Stat <= "010";
when "11011001" => VSup_Stat <= "010";
when "11011010" => VSup_Stat <= "010";
when "11011011" => VSup_Stat <= "010";
when "11011100" => VSup_Stat <= "010";
when "11011101" => VSup_Stat <= "010";
when "11011110" => VSup_Stat <= "010";
when "11011111" => VSup_Stat <= "010";
when "11100000" => VSup_Stat <= "010";
when "11100001" => VSup_Stat <= "010";
when "11100010" => VSup_Stat <= "010";
when "11100011" => VSup_Stat <= "010";
when "11100100" => VSup_Stat <= "010";
when "11100101" => VSup_Stat <= "010";
when "11100110" => VSup_Stat <= "010";
when "11100111" => VSup_Stat <= "010";
when "11101000" => VSup_Stat <= "010";
when "11101001" => VSup_Stat <= "010";
when "11101010" => VSup_Stat <= "010";
when "11101011" => VSup_Stat <= "010";
when "11101100" => VSup_Stat <= "010";
when "11101101" => VSup_Stat <= "010";
when "11101110" => VSup_Stat <= "010";
when "11101111" => VSup_Stat <= "010";
when "11110000" => VSup_Stat <= "101";
when "11110001" => VSup_Stat <= "101";
when "11110010" => VSup_Stat <= "101";
when "11110011" => VSup_Stat <= "101";
```

```
when "11110100" => VSup_Stat <= "101";
when "11110101" => VSup_Stat <= "101";
when "11110110" => VSup_Stat <= "101";
when "11110111" => VSup_Stat <= "010";
when "11111000" => VSup_Stat <= "101";
when "11111001" => VSup_Stat <= "101";
when "11111010" => VSup_Stat <= "101";
when "11111011" => VSup_Stat <= "101";
when "11111100" => VSup_Stat <= "101";
when "11111101" => VSup_Stat <= "101";
when "11111110" => VSup_Stat <= "101";
when "11111111" => VSup_Stat <= "010";

                    when others => VSup_Stat <= "000";
        end case;
end process outputs;

    --Seperate switch_stat
outsep: process (VSup_Stat)
    begin
        V1 <= VSup_Stat(2);
        V2 <= VSup_Stat(1);
        V3 <= VSup_Stat(0);
end process outsep;

end behave;
```

Appendix E

5-Phase SSMC Photos

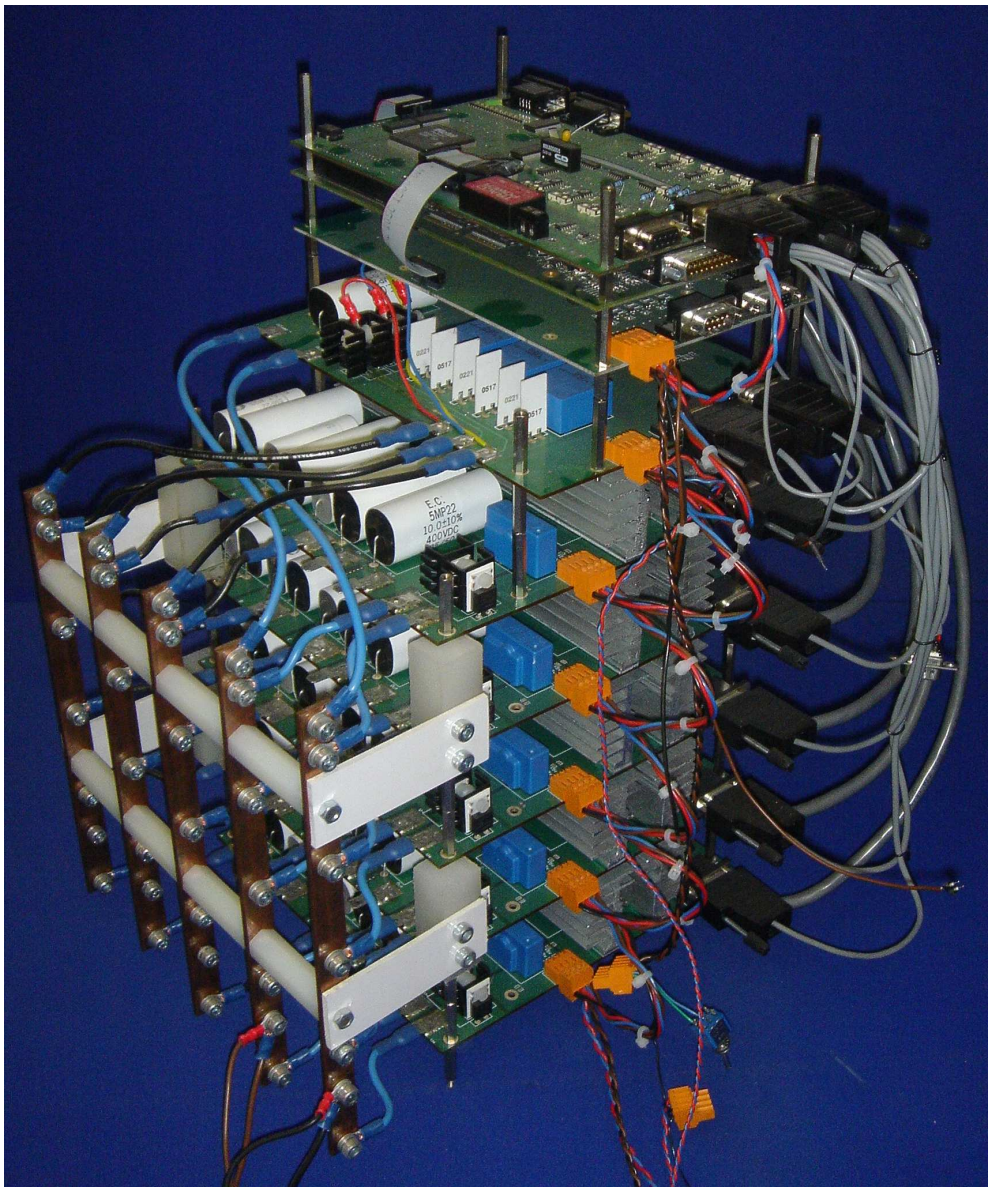

Figure E.1: SSMC Front.

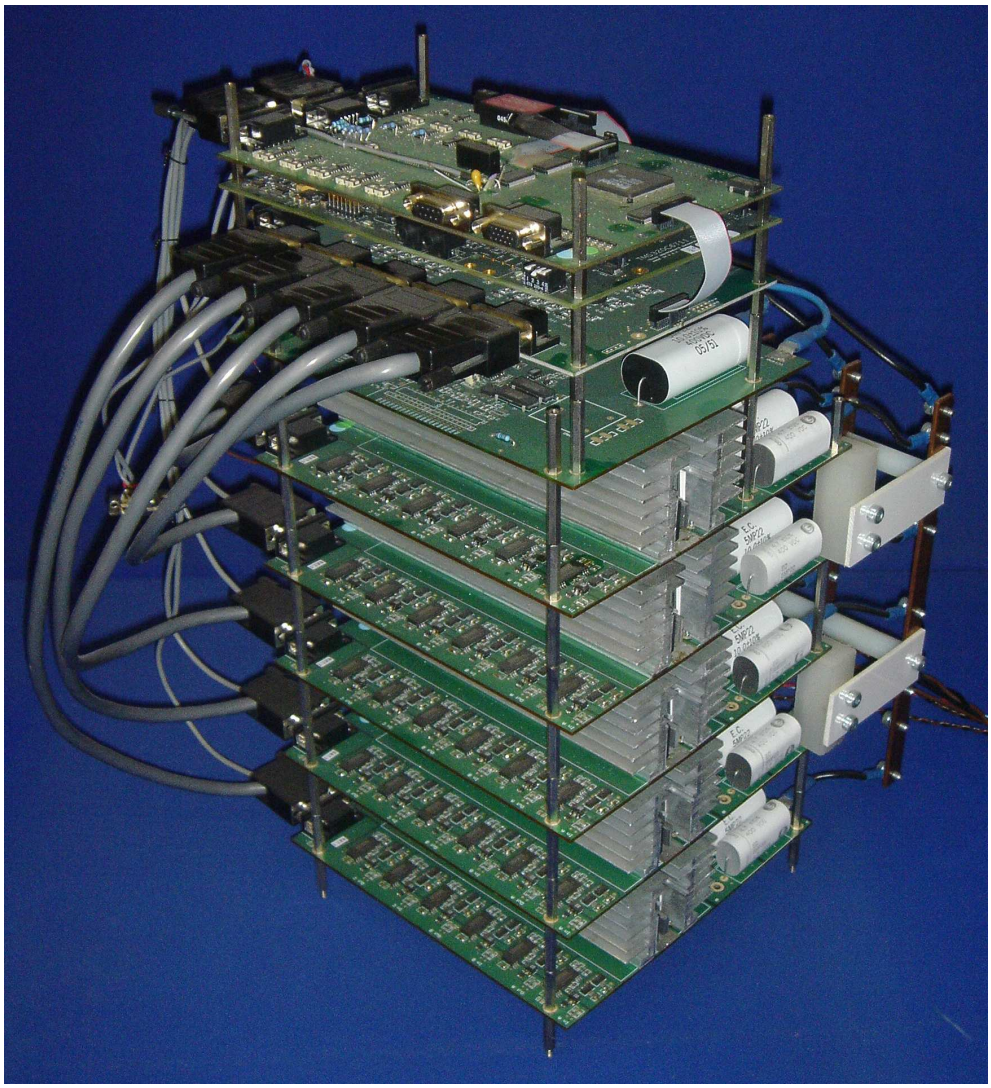

Figure E.2: SSMC Back.

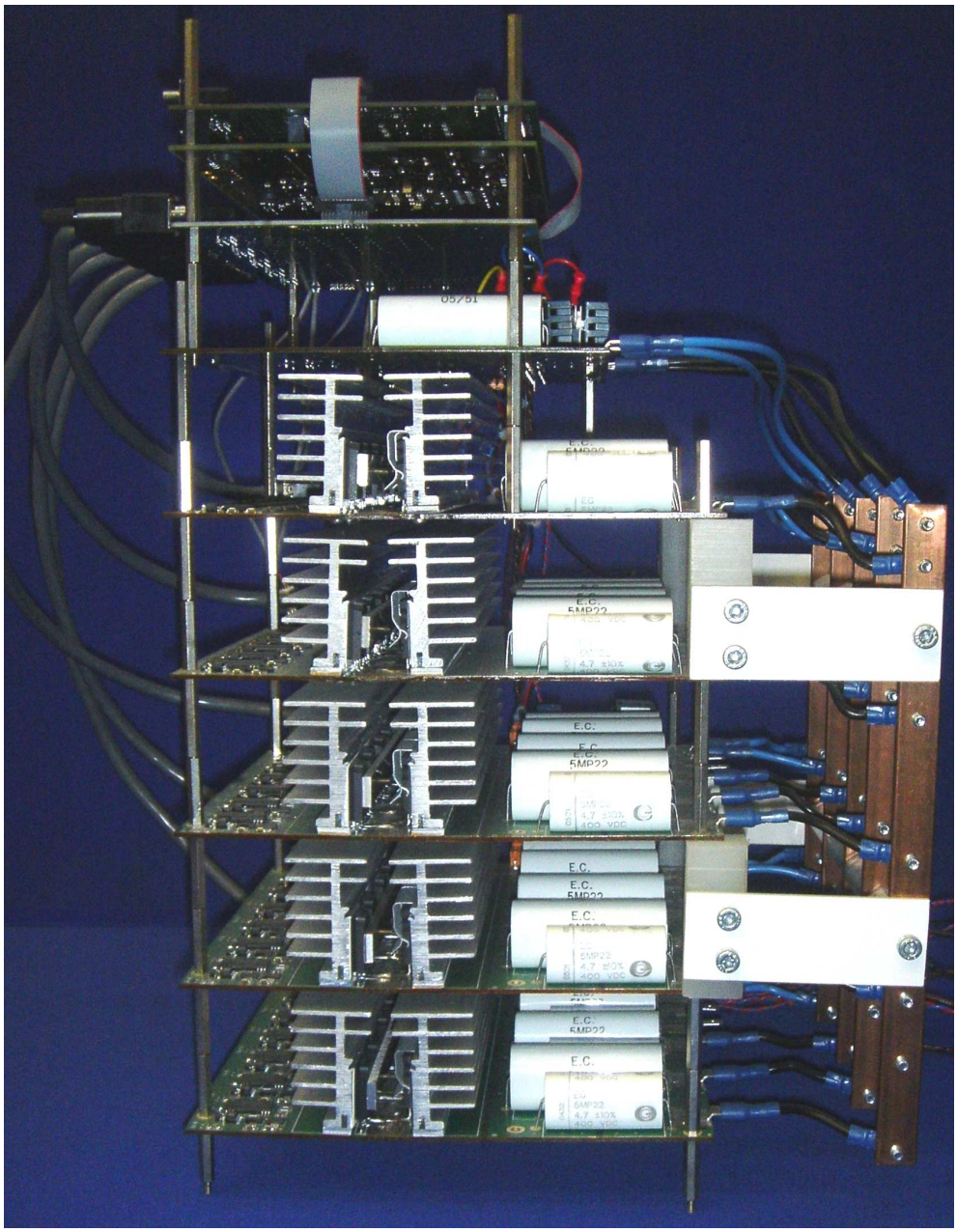

Figure E.3: SSMC End.

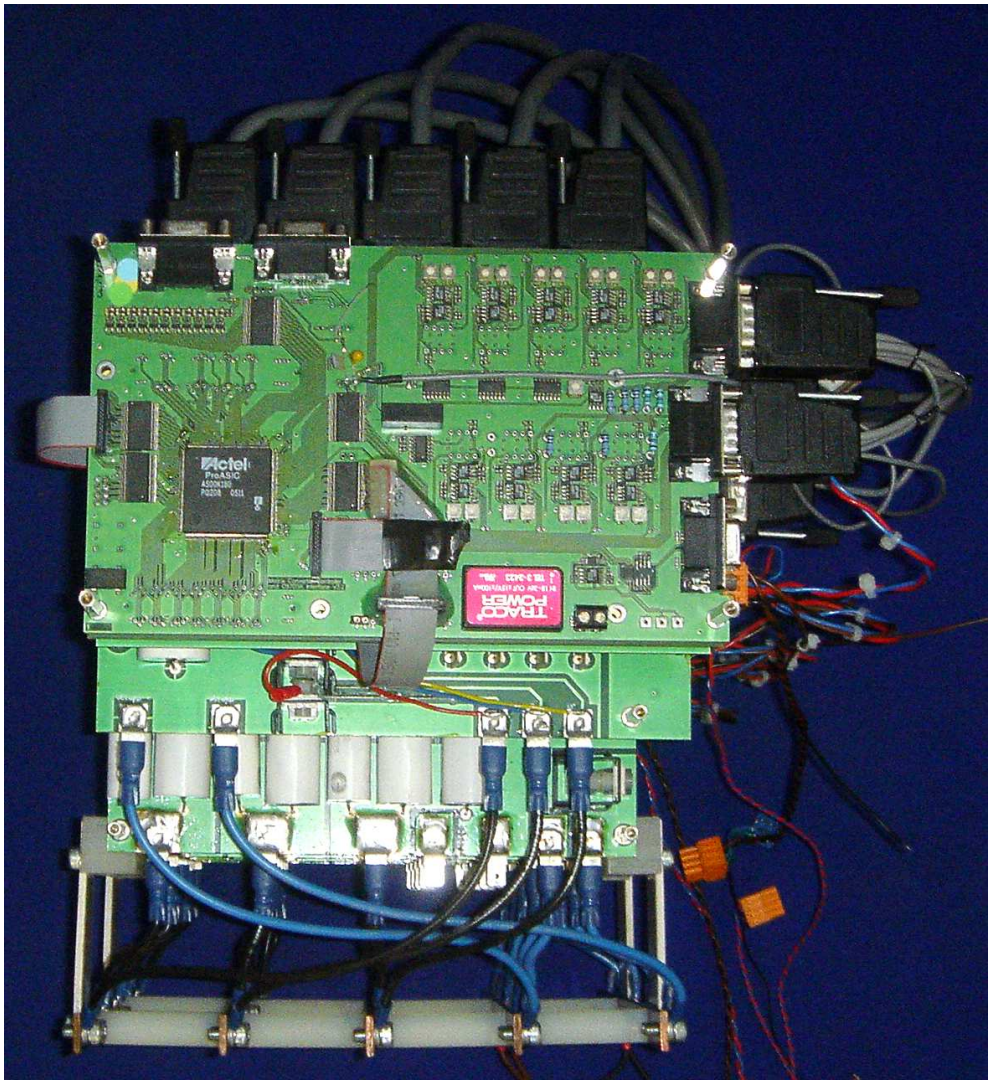

Figure E.4: SSMC Top.

Appendix F

Matrix PCB Layers & Photos

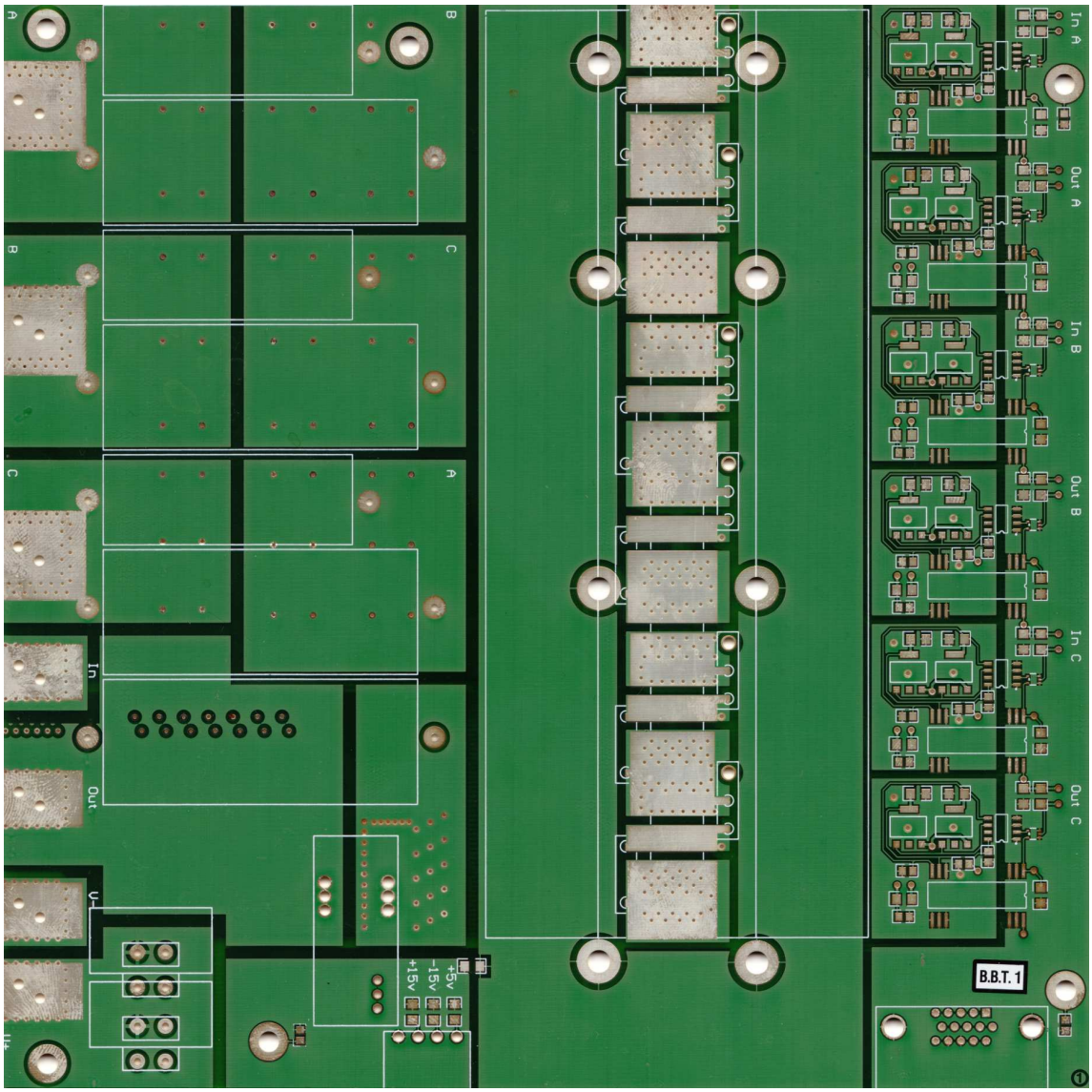

Figure F.1: Matrix PCB Photo - Top.

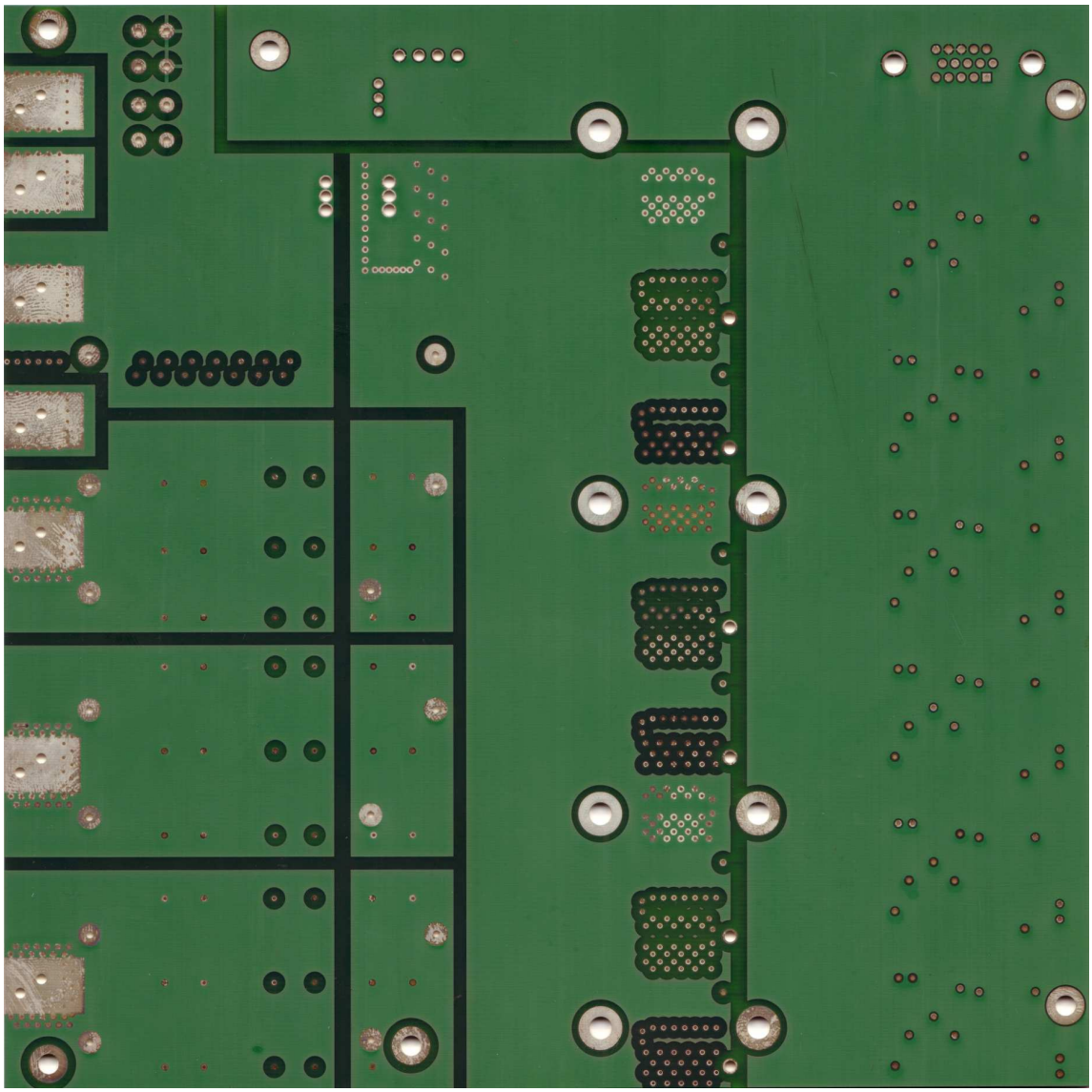

Figure F.2: Matrix PCB Photo - Bottom.

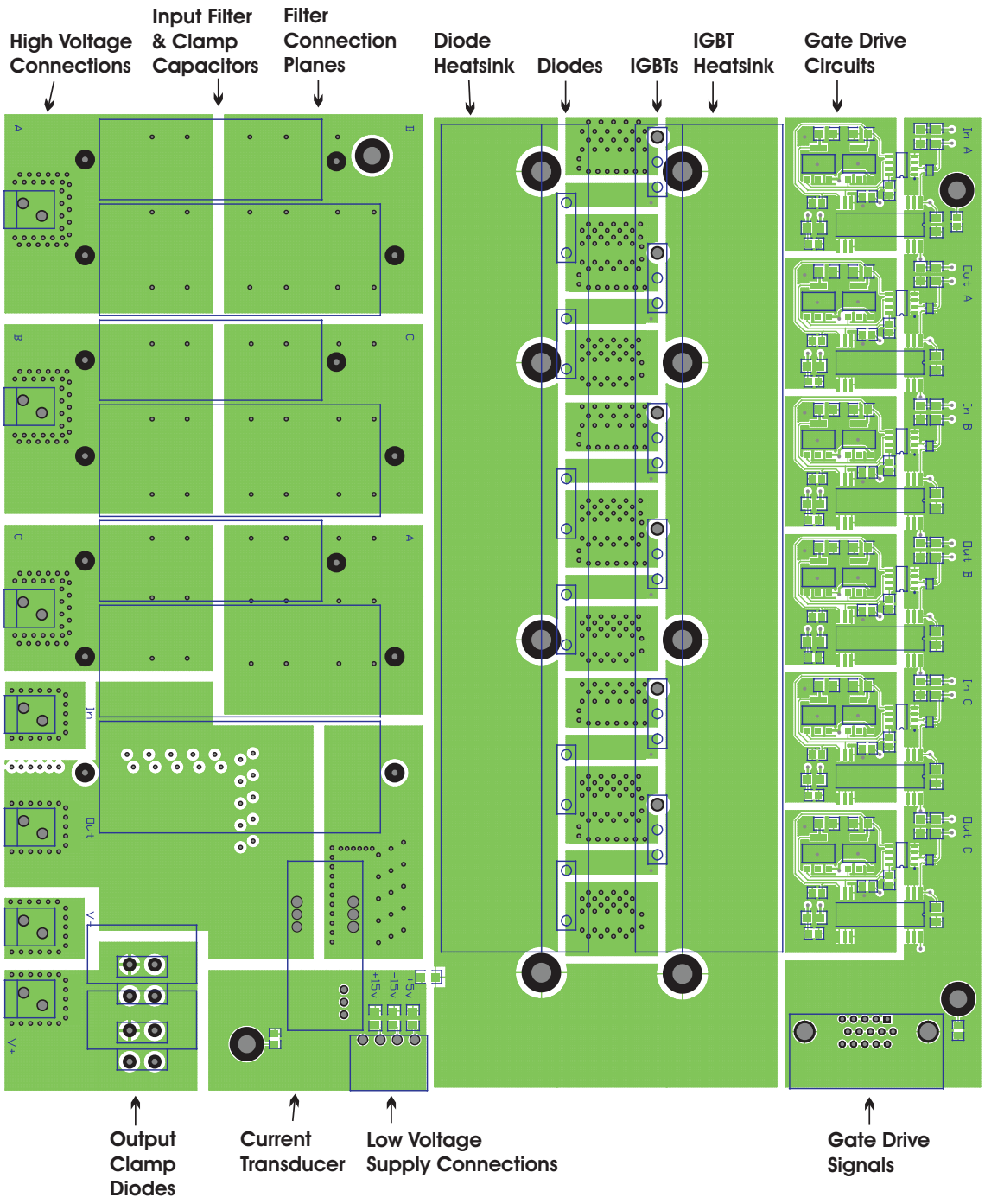

Figure F.3: Matrix PCB - Top Layer.

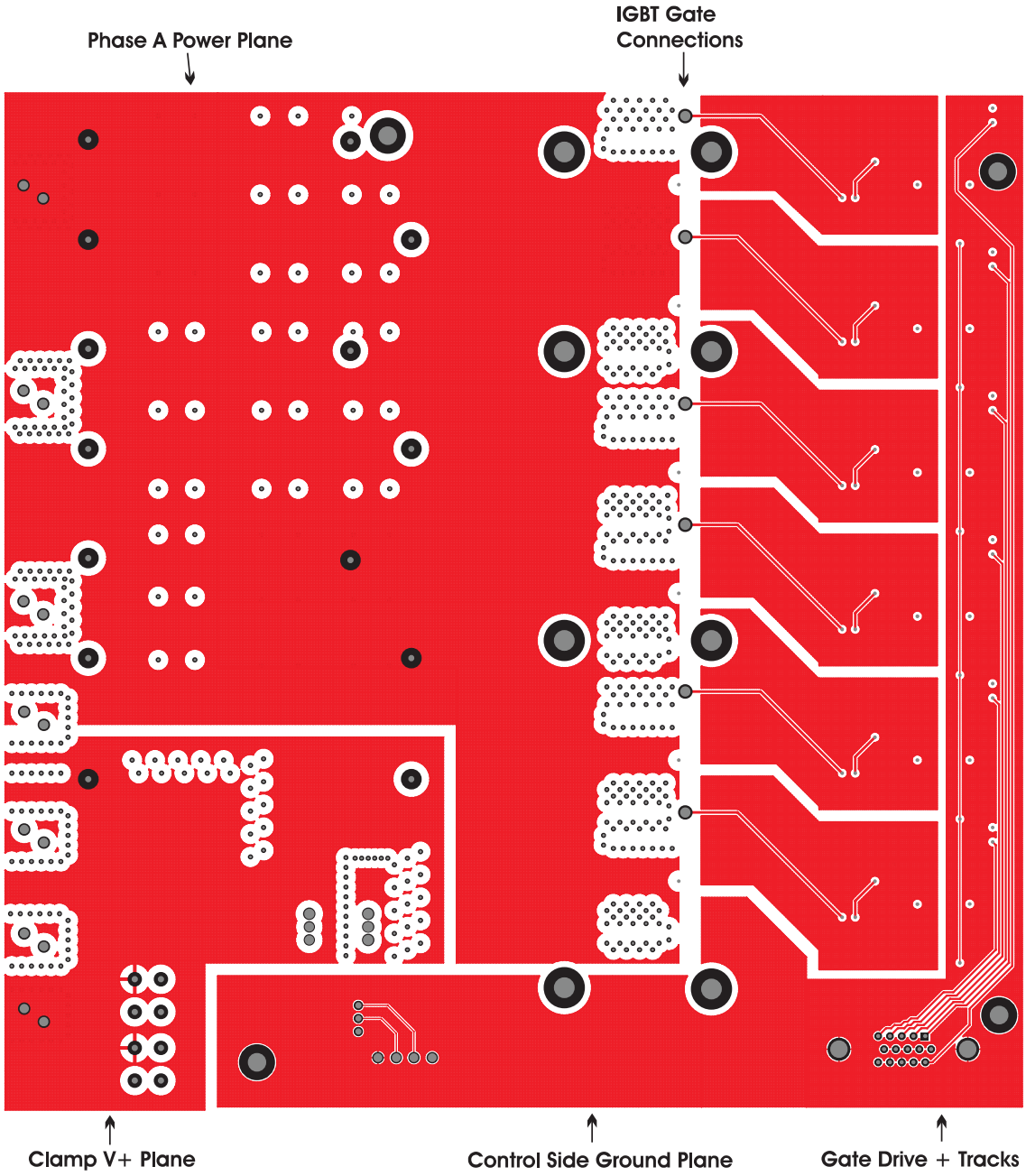

Figure F.4: Matrix PCB - Mid Layer 1.

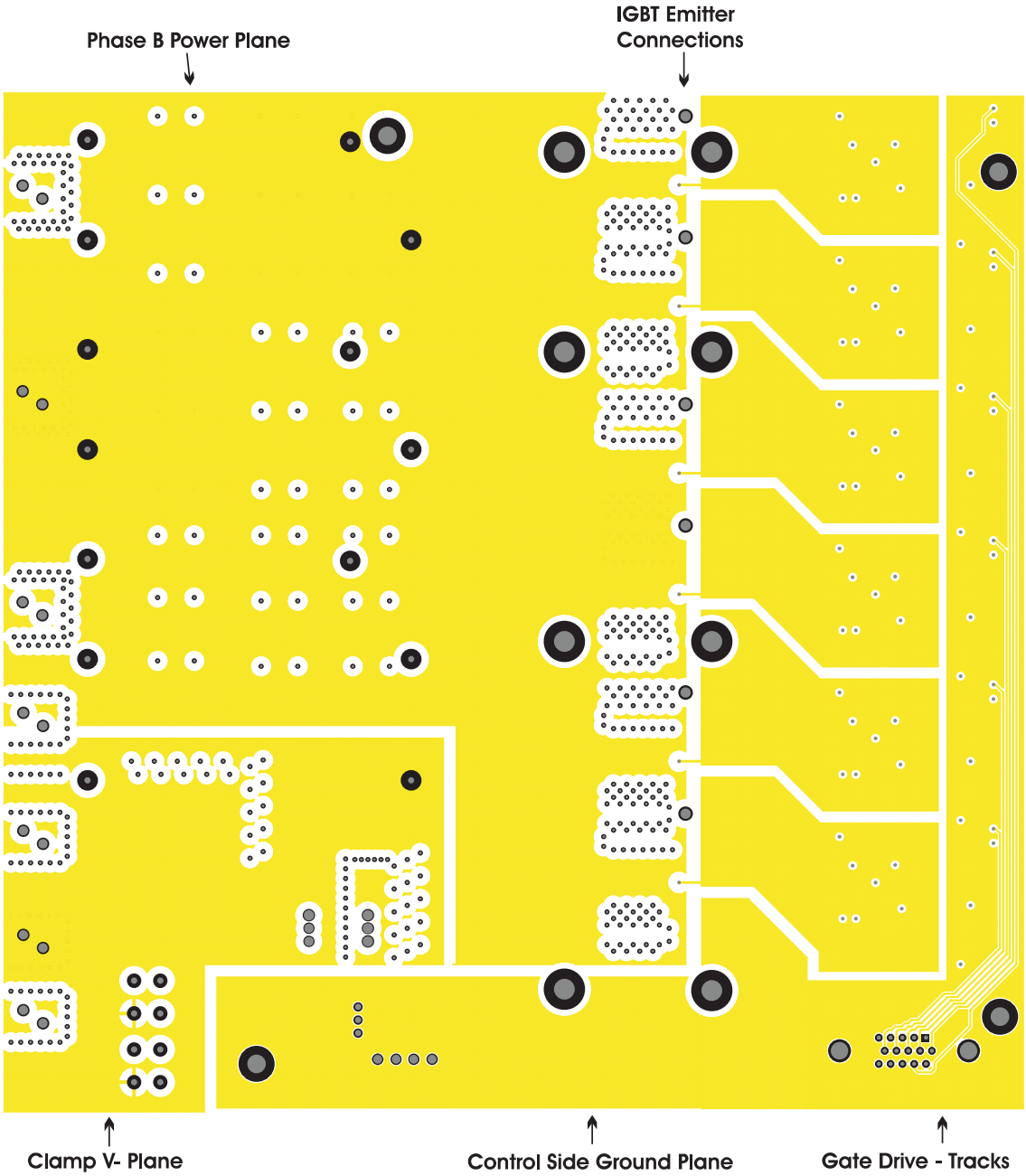

Figure F.5: Matrix PCB - Mid Layer 2.

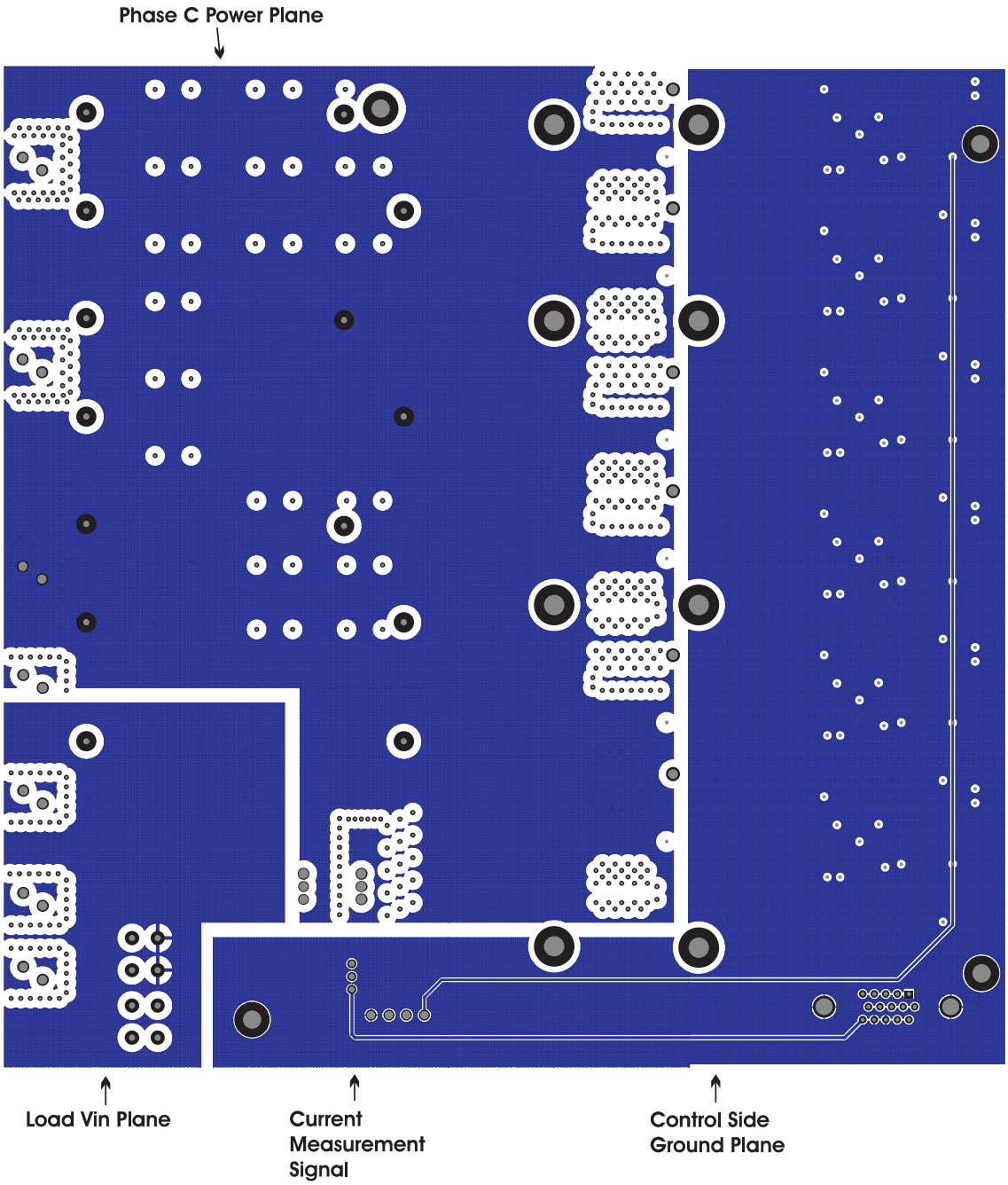

Figure F.6: Matrix PCB - Mid Layer 3.

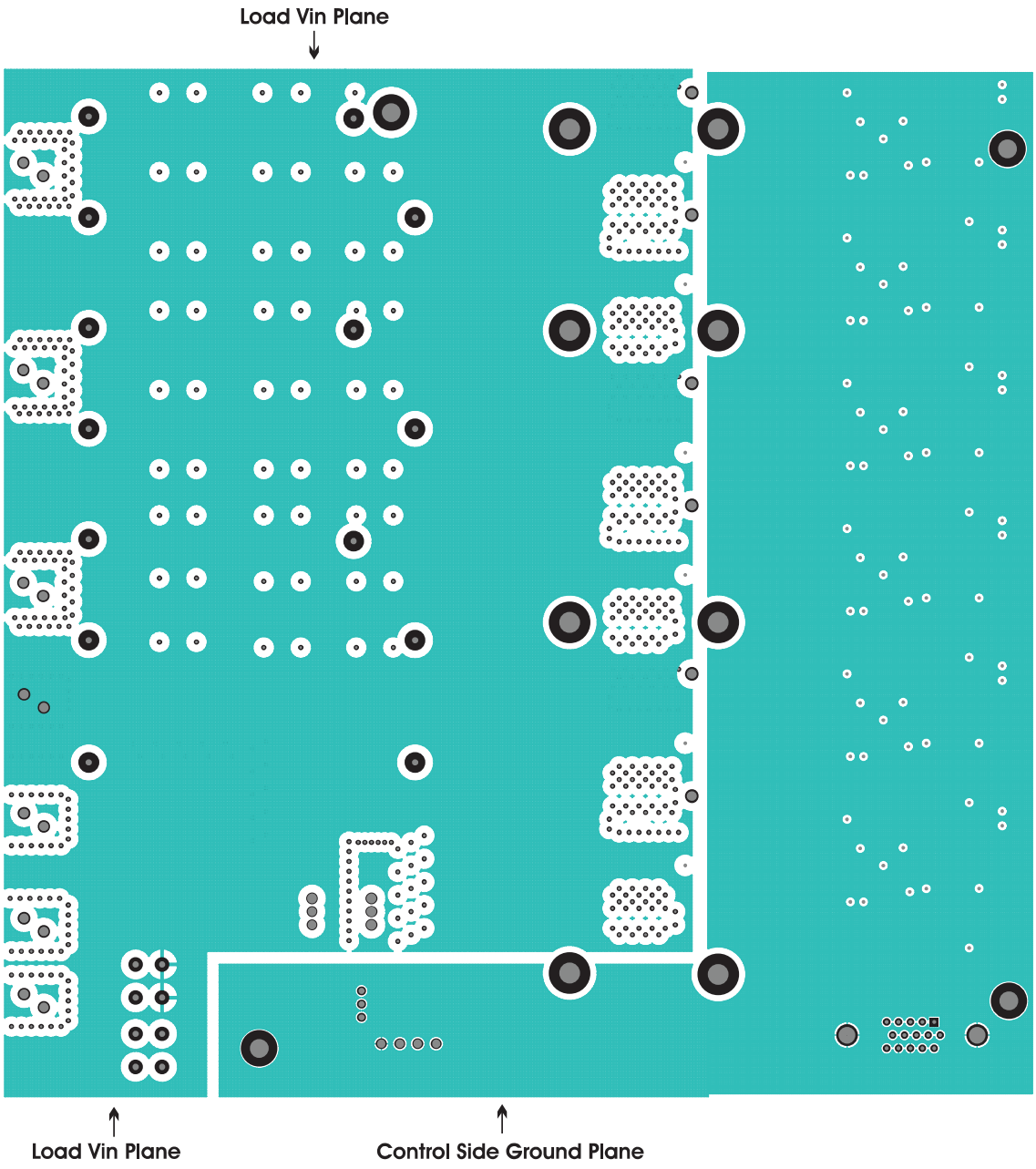

Figure F.7: Matrix PCB - Mid Layer 4.

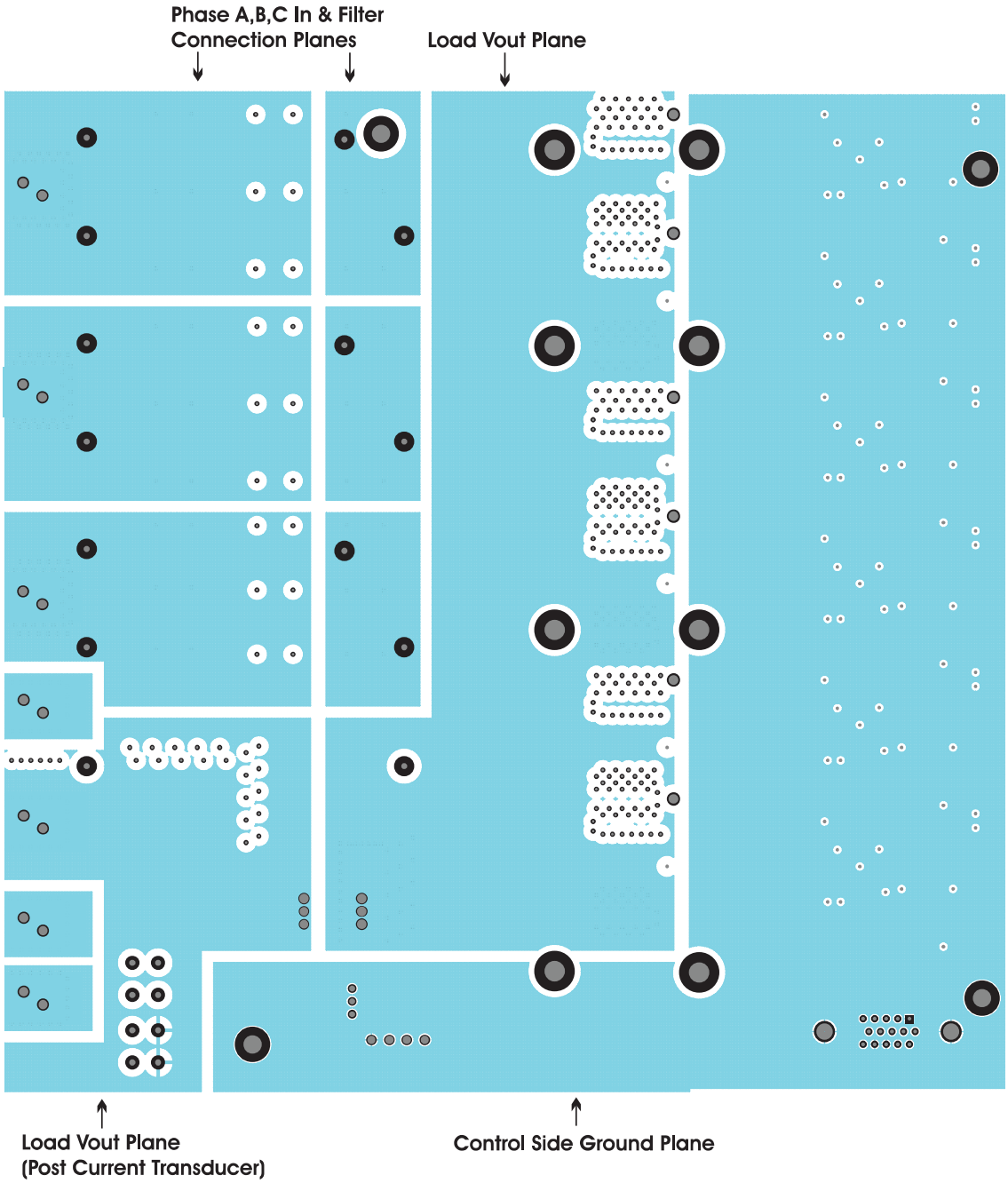

Figure F.8: Matrix PCB - Bottom Layer.

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